An Approach for Improving Routability of 3-Dimensional Maze Routing

Pawut Satitsuksanch

A Master Thesis
Presented to
Department of Computer Science
Faculty of Science and Technology
Assumption University

In Partial Fulfillment
of the Requirements for the
Master Degree of Science
in Computer Science

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Abstract

This thesis presents a modified maze routing technique, which is based on Lee-Moore maze routing algorithm on 3-dimensional layout space. The proposed technique is used to improve the routability of 3-dimensional maze routing. The process includes identifying the problem of using maze routing in 3-dimensional layout space and testing with the proposed technique. The experimental result shows the improvement of routability. The new technique is general enough to apply with other models.
Chapter 1

Introduction

The 3-dimensional layout generation in the field of VLSI is driven by the technology of 3-dimensional IC [1,2]. The 3-dimensional layout generation is a challenging problem in design automation. It has been known that even simplified 2-dimensional layout generation problems are very complex optimization problems. In general, existing layout generation systems are roughly decomposed into two phases, which are placement and routing. Although placement and routing are closely related and interdependent, they have been traditionally separately solved because of their computational complexities. Both placement and routing problem are NP complete; hence a large number of heuristics exist for solving problems, which vary in their runtime requirements and qualities of layout produced.
Within the field of 3-dimensional layout generation in VLSI design, some approaches have been proposed for 3-dimensional placement such as in [3,4,5] and some approaches have been proposed for 3-dimensional routing such as in [5, 6].

Even in routing phase, it is sometimes decomposed into small sub-problems, which are global routing and detailed routing because of the increasing complexities wiring in ICs. A global router performs coarse routing; it performs assignment of nets to a subset of routing areas. A detailed router does the exact routing of the nets.

Some forms of 3-dimensional global routing techniques are proposed in [5]. The main strategy of one from the proposed techniques is the expanding surface of 3-dimensional modules to cover as much routing space as possible without overlapping with another then the routing space around a module is split into six 3-dimensional switchboxes. After getting the routing space, which is the set of adjacency switchboxes, the proposed global routing strategy is applied. This technique is claimed that it is applicable of the global approach to evaluate routability of the proposed placement.

In [5] have not yet explicitly answered the detailed routing problems because the 3-dimensional detailed routing has not been performed there.

The layout generation process will not finish without completing all interconnections, which are taken care of detailed router. There exists an old and well-known but still up-to-date algorithm for detailed routing, which is Lee-Moore maze algorithm [7,8]. The main attributes of this algorithm are very general which can apply with many routing problems and it guarantees finding path if one exists. The original algorithm has been extended by many authors to include a number of features such as
multiple layers and multiple-pin nets [9,10]. Many coding techniques have been proposed to improve the performance of Lee-Moore maze routing algorithm [9,10,11].

By the nature, Lee-Moore maze routing algorithm routes one path at a time therefore the previously routed nets may block the other unrouted nets. The rip-up and reroute algorithm [10,12,13] is used to solve this kind of problem. However using rip-up and reroute algorithm does not guarantee the 100% of routability.

From the preliminary study, The problem of using 3-dimensional detailed routing based on Lee-Moore maze routing technique is indicated. The developed general 3-dimensional detailed routing is proposed based on the Lee-Moore maze routing algorithm and its extensions, which are multi-layers and multiple-pin nets. This proposed technique is aim at maximizing the routing completion before employed the rip-up and reroute technique.

In Chapter 2, the relevant concepts are reviewed. Chapter 3 presents the 3-dimensional layout model, which consists of 3-dimensional layout space, modules, and routing space. In Chapter 4, the general problems are identified and preliminary study result is included. Chapter 5 presents the snake hole problem, proposed technique and experiment result. The conclusion is in Chapter 6.
Chapter 2

Literature Reviews

This chapter is devoted for the relevant concepts, which are closely related to this research work. Lee-Moore maze routing algorithm and its extensions is reviewed here. 3-dimensional integrated circuit and 3-dimensional layout generation are also summarized in this chapter.

2.1 Lee-Moore Maze Routing Algorithm and its Extensions

Lee-Moore maze routing algorithm is the most widely used technique for detailed general purpose wires routing [7,8]. It guarantees to find a path for a net if one exists and the path determined will be of minimum length.

It is the most classic, but still up-to-date, algorithm for detailed routing. Many available research works can prove for the existing and widely used of this algorithm [14,
Lee’s algorithm for maze routing is a three phase algorithm[7,8,15]. These phases are \textit{wavefront expansion}, \textit{path recovery}, and \textit{sweeping}. In the first phase, \textit{wavefront expansion}, a breadth first search beginning at $s$ is performed. Cells that are one unit from $s$ are labeled, then those 2 units from $s$ are labeled, then those 3 units from $s$ are labeled, and so on. This labeling continues until the target cell $t$ is reached. Blocked cells are not labeled during front wave expansion. Figure 1(b) shows the effect of the \textit{wavefront expansion} phase on the example of figure 1(a). If the wavefront reaches the target cell $t$, then the \textit{path recovery} phase is entered. This is a trace back from $t$ to $s$ (see Figure 1(c)). Now the wire path has been identified. Before the next wire can be routed, this wire path must be blocked and all other labeled cells cleared. This is done in the \textit{sweeping} phase. Figure 1(d) shows the configuration after \textit{sweeping}.
2.2 Multi-Layer Interconnection and Multi-Pin Nets, the variations of Lee-Moore maze routing algorithm

A straightforward way for routing on a three-dimensional grid is to consider a cellular array consisting of unit cubes as shown in Figure 2, where three-layer case is illustrated. As before a pair of source cell and target cell is given. To find the desired path using Lee-Moore maze routing algorithm, we follow the same front wave expansion phase except that all adjacent non-blocked cell including those accessible from above or below layer must be labeled at each step (see Figure 2)
The Lee-Moore maze routing algorithm can be extended for connecting multiple points instead of a pair of points. The aim of the extension is to construct a Steiner tree of small length to connect all points. The “multiple sink, single source” algorithm is used to handle $k$-point nets where $k > 2$. For example, a case with 4 terminals $(k = 4)$, $A$, $B$, $C$, and $D$, which have to be interconnected in a net is shown in Figure 3(a). A pair $A$ and $B$ of the interconnections in the net is selected as initiator points and a connection is established between them by the traditional way. All the grid cells along the paths between them ($A$ and $B$) are then marked as the target cells ($t(s)$) in Figure 3(b). A remaining point in the net is selected as a new source, in this case $C$ is selected. A wavefront is then initiated from the source cell $C$ (in Figure 3(b)). The wavefront is then initiated from the new source cell and will terminate when meet any target cell. A new path is recovered after the path recovery and sweeping phase (in Fig 3(c)). All the cells in the path $A$-$B$-$C$ are again marked as target cells $t(s)$. The last terminal $D$ in this net is marked as source cell $s$ (in Fig 3(d)). Wavefront, path recovery, and sweeping phase are entered. The interconnections of this net is completed because all of the 4 terminals $A$, $B$, $C$, and $D$ are already connected and formed a net of routed terminals (in Figure 3(e)).
This algorithm for routing multiple-pin is guaranteed to find a tree if one exists but it may not be a tree of minimum length.

Figure 3(a) 4 unconnected terminals

Figure 3(b) Initiated path is marked as target cells t(s) and terminal C is marked as source cell. Then wavefront expand from s

Figure 3(c) New path from the A-B-C interconnection

Figure 3(d) Terminal D is marked as source cell s and path A-B-C is marked as target cells t(s).

Figure 3(e) Completed multiple terminal net.

Figure 3 Illustration of 4 terminals interconnection
2.3 3-Dimensional Integrated Circuit

The following definition of the three-dimensional integrated circuit is provided with the courtesy of R&D Association for Future Electron Devices (FED).

A three-dimensional integrated circuit is a vertically interconnected multilayered device having a different function in each layer. An illustration is in Figure 4. This device features in high-density integration and high-speed parallel signal processing. Incorporation of different functions within the layers increases the possibility of carrying out various complicated functions not possible in conventional two-dimensional ICs. Silicon-On-Insulator (SOI) techniques, laser and electron-beam annealing, lateral solid phase epitaxy, techniques involving low-temperature processing and ultra-thin SOI devices are examples of developments directly resulting from this research. Refractory metal wiring technique and superheteroepitaxial growth of GaAs directly on SOI, are also products of this project. These techniques will contribute to realizing high-density 3-D (three-dimensional) memory and logic ICs, ultra fast parallel pattern recognition ICs, and other parallel sensor ICs.

Figure 4 Illustration of 3-D Integrated Circuit
2.4 3-Dimensional layout generation

Like the layout generation in 2-dimensional circuit system, the 3-dimensional layout generation is generally separated in two phases. The first one is the arrangement of two-dimensional or three-dimensional electronic components of the circuit in finite 3-dimensional layout space, which is known as 3-dimensional placement. The second phase, which will be performed after the first phase, is 3-dimensional routing, which is the process of interconnection among such components according to the information from the placement and circuit description.

There are some proposed systems for 3-dimensional placement such as [3,4,5]. For the first two proposed system[3,4], the multiple layered placement of 2-dimentional modules is considered but for the last one from example[5], the author have proposed the model of the placement of 3-dimensional modules in the 3-dimensional continuous layout space together with 3-dimensional global routing for analyzing the routability of the placement.

Some researches emphasize on 3-dimensional routing problem such as [6, 14]. The three-dimensional routing technique, which is the extension form of line search algorithm, is implemented on multi-layer ceramic printed circuit boards in [6]. The general-purpose tool called VYUHA, for detailed routing is presented in [14]. The authors of [14] have claimed that the multiple layers and multiple pin problems, which arise in 3-dimensional chips, can be easily handled using their tool.

Some CAD tools for automated 3-dimensional layout generation are also available in the market. True-3D technology[19] is an example of the CAD product based on 3-dimension layout generation.
Chapter 3

The 3-Dimensional Layout Model

In this chapter, the physical aspects of the model for 3-dimensional structure that describe the 3-dimensional layout space, 3-dimensional modules, and 3-dimensional routing space are defined. Some constraints, which projected on the model, are also stated in this chapter.

The major constraints imposed on the dimension of nets to be wired are characterized by two values; a minimum width \( w \) and a minimum clearance \( c \), which must be maintained between wires. It is assumed for standardization that these two values are fixed throughout all the nets, and then combined into a single center-to-center constraint \( \Delta = w + c \). This leads to uniform rectangular grid, having an incremental spacing of \( \Delta \). Then by requiring that all nets are routed following the lines of this grid, the width and clearance constraints will be satisfied automatically.

This research work does not attempt to address the question of floorplanning or automatic cell placement. There are, however, three restrictions placed on the module
placement: The module must be rectangular, oriented orthogonally, and placed a finite and non-zero distance apart.

By following these constraints, the 3-D layout space, routing space and modules can be specified as the following.

3.1 3-Dimensional Layout Space

The 3-D layout space is simply the 3-D cellular array, which is defined by $X, Y, Z$ where these variables are the maximum range of each dimension. The triple $(x,y,z)$ is an element of the Cartesian product of these three variable, $(x,y,z) \in X \times Y \times Z$, corresponds to a cell in layout space.

3.2 3-Dimensional Modules

Module description

- Module’s size, designated by three integer parameters, $l_m, w_m, h_m$ representing length, width, and height of the module respectively.

- Module is also a 3-dimensional cellular array where the triple $(u_m, v_m, w_m)$ corresponds to a cell in module $m$.

- The module’s position, designated by three variable $x_m, y_m, z_m$ which are defined in the layout space and associated with the module originate $(u_m, v_m, w_m) = (0,0,0)$.

- A pin $p_{mn}$ is assumed to be located on a module’s surface of the module. Its location is defined by a triple $(u_{pmn}, v_{pmn}, w_{pmn})$, so the exact pin $p_{mn}$ location in layout space is $(x_m + u_{pmn}, y_m + v_{pmn}, z_m + w_{pmn})$. 


3.3 3-Dimensional Routing Space

The 3-D routing space is the free cells in layout space, which are not occupied by any module or previously routed path(s).
Chapter 4

Towards the Improved Routability in 3-Dimensional Layout Space

In this chapter, the general 3-dimensional routing problem is stated. The extended Lee-Moore routing techniques, which are multiple layers and multiple pins routing technique, are tested on the given 3-dimensional model. The preliminary study is on applying the existing extended Lee-Moore maze routing techniques on the 3-dimensional layout model. The result from this preliminary study shows an unacceptable routability therefore the routability should be improved by the modified extended technique.
4.1 General 3-Dimensional Routing Problem

The problem concerns the routability of the terminals on 3-dimensional modules that represented physically 3-dimensional sub-circuits. The main objective is to complete as many connections of the nets as possible with in the fixed routing space.

The problem may be formally stated as the following.

Given:
- Rectangular 3-dimensional layout space where modules will be placed.
- A set of rectangularly approximated modules with fixed sizes and fixed pins positioned on module surfaces.
- A net list specifying which pins are to be connected.
- A placement of 3-dimensional modules in a given 3-dimensional layout.

Find:
- A design-rule correct detailed routing technique with the routing completion and the minimum total interconnection length.

It is inevitable that the shortest interconnection criteria of maze routing algorithm needs to be relaxed to some degree in order to allow the routing completion to be improved.
4.2 Preliminary Study

Some forms of specified 3-dimension placement are tested with the traditional extended Lee-Moore techniques, which are multiple layers and multiple pins net.

The traditional extended Lee-Moore techniques is tested on 15 different 3-dimensional placement. In general, there are 3 sets of the module placement and within each set of the module placement, it consists of 5-difference interconnections. The experiment result is shown in Table 1.

```
<table>
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<th>Placement</th>
<th># of modules</th>
<th>Size of modules</th>
<th># of terminals per module</th>
<th>Total terminals</th>
<th># of nets</th>
<th>% of nets completions</th>
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Table 1 Preliminary experiment results

4.3 Deriving Problem from the Preliminary Study

Form the preliminary study, percent of nets completion is not acceptable. After the investigation, we can identify the main cause of this problem. The main cause of this
problem is that the unrouted terminals are blocked by the paths of routed terminal on the same plane of the same module. Example case is illustrated in 2-dimensional grid cells in Figure 5. Net $A$ is the interconnection of terminal $a$ on module $X$ and terminal $c$ on module $Y$ and net $B$ is the interconnection of terminal $b$ on module $X$ and terminal $d$ on module $Y$.

Figure 5 Illustration of the blockage, net $B$ is blocked by the routed path of net $A$.

Reordering of the routed net may solve this kind of problem therefore rip-up and reroute technique may be applicable in increasing the routability. Rip-up and reroute technique also has some drawback, which is rip-up and reroute technique has to perform after the detailed routing finished unsuccessfully and detailed router has to routed the uncompleted nets again and again.

From the problems stated above, this will be more applicable if we can maximize the routability by relaxing the shortest path criteria to some certain degree before applied with rip-up and reroute technique.
Chapter 5

Proposed Technique and Experiment

The main problem deriving from the preliminary study is the unrouted terminals are blocked by the previously routed terminals, which locate on the same plane of the same module. The author calls this kind of problem as snake hole problem by mimicking the nature of the snake hole. The proposed technique to solve this kind of problem is stated in this chapter. The result of using the proposed technique is compared with the traditional Lee-Moore maze routing technique with its extension. The experiment results show the improvement of routability and prove the applicable of this technique on this kind of problem.

5.1 Snake Hole Problem

By general, the snake hole is fit for a snake to pass through it and there is only one way for a snake to enter into or exit from the hole. Therefore, if there is any object
block the hole, snake cannot creep into or creep out from the hole. By this nature, the
snake hunter sometimes places the snake-trap at the gate of snake hole using the
limitation of the snake hole. If the hunter could not lie the snake-trap as close to the hole
as possible, the snake has many directions to creep away.

The deriving problem can be viewed as a snake hole problem as well because of
the same limitation. A terminal is placed on the surface of the module, therefore there is
only one direction for connecting the terminal to the routing space except the terminals
which place at the corner or the edge of the module.

Let degree of connectivity is defined as the number of routing direction from a
cell to routing space. The degree of connectivity of the terminal on the module surface is
3 whenever the terminal is on the corner of the module defined formally as the triple

$$(u_{pmn},v_{pmn},w_{pmn}) \in \{(l_{g_{m-1}})\times(1,wd_{m-1})\times(1,ht_{m-1})\}.$$ 

The degree of connectivity of the terminal on the module surface is equal 2 whenever the terminal is on the edge of the
module and not on the corner of the module. It is equal to 1, if it is neither on the edge nor
on the corner of the module.

5.2 The Proposed Technique

The objective of the solution to solve snake hole problem is preventing the snake
hole from blocking and increasing the possible direction for a snake to enter into or exit
from its hole. Therefore the proposed technique to solve snake hole problem on 3-
dimensional maze routing is reserving the cell which is adjacent to the terminal in order
to avoid blocking caused by the other previously routed net and increase the possible
routing directions. This can increase the degree of connectivity of the terminal on the module surface to 5 in case that this terminal is not adjacent to any other terminals.

The critical routing cell is defined as a free cell in routing space and it is adjacent to the terminal.

The algorithm to locate the critical routing cell is listed below:

Algorithm for locate the critical routing cell

For each terminal cell \((x,y,z)\).

Begin

If \((x+1,y,z)\) is a free cell in routing space then

The critical routing cell = \((x+1,y,z)\);

Exit;

If \((x,y+1,z)\) is a free cell in routing space then

The critical routing cell = \((x,y+1,z)\);

Exit;

If \((x,y,z+1)\) is a free cell in routing space then

The critical routing cell = \((x,y,z+1)\);

Exit;

If \((x-1,y,z)\) is a free cell in routing space then

The critical routing cell = \((x-1,y,z)\);

Exit;

If \((x,y-1,z)\) is a free cell in routing space then

The critical routing cell = \((x,y-1,z)\);

Exit;

If \((x,y,z-1)\) is a free cell in routing space then

The critical routing cell = \((x,y,z-1)\);

Exit;

End
The algorithm for solving snake hole problem in 3-dimensional maze routing is stated below:

**Algorithm for solving snake hole problem in 3-dimensional maze routing**

1. **Modify the routing space by following:**
   
   *For any critical routing cell, reserve it by mark it as a special blocked cell.*

2. **For each associated pair of terminal and reserved critical routing cell, initiate the path between them.**

3. **Apply Lee-Moore maze routing technique on the modified layout placement by:**

   *For each net, the reserved critical routing cells associated to their terminals are routed instead of the terminal themselves.*

These two algorithms will not affect the runtime of Lee-Moore maze routing technique.

### 5.3 Experiments and Discussion

The comparison between traditional Lee-Moore maze routing technique and its extensions and the modified technique based on the same set of layout placement from the preliminary study is given in Table 2. Percent of nets completion from Table 2 shows a lot improvement of routability when applying with the proposed technique.

Table 3 shows the summarized comparison between two techniques on the various kind of layout placements. Each set is summarized from 5 difference net lists of the same kind of modules and module locations. All of the experiments is performed on 40x40x40 layout space. From the experiment results show in Table 3, it is obvious that
the low percent of nets completion from applying traditional Lee-Moore maze routing technique with its extensions does not come from the net congestion problem. For example, in experiment set#1, same 16 modules is placed loosely in the layout space and percent of routing space is 93.75, the result of using traditional Lee-Moore technique still be poor. This low routability can be indicated the existence of snake hole problem on 3-dimensional maze routing. Therefore the proposed technique can solve this problem.

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Table 2 Comparison between traditional Lee-Moore technique and proposed technique using the preliminary experiment set

The two main attributes of the proposed technique are preventing the terminal from blocking by the previously routed path and increasing possible routing direction by increasing degree of connectivity of the terminal. It is noted here that there exist cases
where the proposed technique cannot increase degree of connectivity of the terminal on the module surface, which is when a terminal is surrounded by other terminals in all four directions.

The improvement of the routability after applying with the proposed technique can show its application on this kind of problem.

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Table 3 Comparison between traditional Lee-Moore technique and proposed technique using various kind of layout placements
Chapter 6

Conclusion and Future Research

Lee-Moore maze routing technique and its extension, which are multiple layers and multiple pins nets, is tested on the 3-dimensional layout. The result of the test is the poor routability. The investigation identifies the cause of poor routability problem to be the blockage of the previously routed nets. This problem is viewed as the snake hole problem. The rip-up and reroute technique can be applied to solve at the expense of computation time on this problem. Therefore a new modified technique is proposed to maximize the routability by relaxing the shortest path criteria.

The two main attributes of the proposed technique are reserving the critical routing cell thereby increasing the routing directions. From experimental results, the proposed technique shows the improvement of routability of 3-dimensional maze routing.

For further study, the multiple reserving critical routing cell will be considered. Instead of reserving one critical routing cell per terminal, the increasing number of...
critical routing cells per terminal will be observed in order to increase the degree of connectivity of a terminal on a module surface. Further experiment result may show improvement of routability in 3-dimensional maze routing compared with the technique proposed in this thesis.
References


Biographical Sketch

Pawut Satitsuksanoh was born in Bangkok, Thailand, on May 2, 1972. He had secondary education from Suankularb Vithayalai College in Bangkok, Thailand. He received the B.S. degree in Computer Science from Assumption University, Bangkok, Thailand, in 1995. After his graduation, he had worked with Internet KSC for a period of time.