Design and Implement Battery Energy Storage System

by

Wutthikorn Threevithayanon

Faculty of Engineering
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Design and Implement Battery Energy Storage System

A Thesis

Submitted to the Faculty of Engineering

By

Wutthikorn Threevithayanon

In partial fulfillment of the requirements

For the degree of

Master of Engineering in Power Electronics

Advisor: Dr. Seshanna Panthala

Assumption University

Bangkok, Thailand

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Abstract

The thesis deals with the design, construction and testing of a small Battery Energy Storage System (BESS) rated for 1.2kW power level. The principal objective of this project is to develop appropriate converter technology indigenously. The BESS developed consists of a 3-phase pwm based IGBT converter capable of bidirectional power and reactive power transfer between the battery system and electric grid. The converter control is done using two numbers of Texas Instruments Digital Signal Processor TMS320F241.In particular the Battery energy storage system is tested in the following modes:

1.As a stand alone 3-phase –380volt –50Hz a.c generator capable of supplying power to an isolated load with proper voltage and frequency control.

2. In synchronized mode operating stably in parallel with the existing 3-phase electric grid supply. In this mode the BESS is tested for active and reactive power flow in either direction. Power and reactive power levels can be controlled from a computer by sending the required commands to one of the DSP through serial communication.

3. After synchronising the BESS with the electric grid, it is made to operate in power levelling mode that is the power drawn from the grid is kept at a fixed level and the excess demand by the load connected is met by the BESS.

Acknowledgements

"We stand on the shoulders of those who come before"

I would like to thank my advisor, Dr. Seshanna Panthala, for all of his advices and motivation throughout the completion of this thesis. I would like to thank Asst. Prof. Dr. Kittiphan Techakitiroj for his enormous help in DSP controller design both hardware and software. I would like to thank Dr. Sudhiporn Patumtaewapibal, Dean of Faculty of Engineering for his own funding and lit the idea of the project. Futhermore, I would like to thank Dr. Sanjiva Rao Bhaganagarupu, Director of Power Electronics Program, Dr. Thiraphong Charoenkhunwiwat and all Faculty members of Power Electronics for their support. Also, I would like to thank A. Rungsri Wongvitavas and her staffs, DSP lab staffs, all of my friends for their help. Finally I would like to thank my Dad, my Mom and my family who never give up on me.

Table of contents

List of Figures

List of Tables

List of Symbols

Symbols

a	=	Transformer Ratio
B_L	=	Blanking time Ratio
C_f	=	Filter Capacitor
E	=	Inverter voltage
Eff	=	Efficiency of the converter
$f_{1desire}$	=	Desired waveform frequency
$f_{switching}$	=	Switching frequency
I	=	Current flow between two source
Irms	=	RMS value of line current
L_f	=	Filter inductor
M_a	=	Modulation Index
M_f	=	Frequency modulation index
P_{dc}	=	DC Power input to converter
P_O	=	Real Power output of inverter
$P_{out\ 3\ ph}$,P_{out}	=	Power output of converter 3 phase
Q_O	=	Reactive Power output of inverter
r	=	Internal resistance of inverter (measuring)
R_f	=	Filter Resistor
V_{batt},V_{dc}	=	Battery voltage or DC link voltage
V_{CE}	=	Saturated voltage across IGBT during on period
$V_{desired}$	=	Amplitude of the desire waveform
V_{in}	=	Input of filter voltage (PWM)

$V_{L\text{-}Lcalc}$	=	Line to Line voltage calculate (RMS)
V_{out}	=	Output of filter voltage
V_{rms}	=	RMS phase voltage
V_{tri}	=	Amplitude of triangular waveform
V_S	=	Grid voltage (RMS) / phase
Z_T	=	Impedance between inverter and electric grid ($R+jX_L$)
δ	=	Angle between V_S with E
φ	=	Power factor angle
θ	=	Impedance angle of Z_T

CHAPTER 1.

Introduction

1.1 What is a Battery Energy Storage System?

BESS-Battery Energy Storage System consists of a static solid state controlled converter capable of bidirectional power and reactive power transfer between a Battery Bank and A.C Power source such as an electric grid. Fig.1.1 depicts the BESS in its most frequently used environment . The main component systems of the BESS as can be seen from the figure are ;

(a) Battery Bank consisting of number of cells connected in series to provide the required voltage and ampere-hour capacity.

(b) Converter system consisting of 3-phase power module in bridge form, gate driver system, a microcontroller for controlling the gate driver.

(c) Sensing the system parameters and a communication means such as RS232 for interaction between the controller and the local computer.

(d) Industrial load and the utility forms the environment for the BESS to interact.

1.2 What are the application areas of BESS ?

(a) To meet the peak demand of an industrial system for short periods in terms of power and reactive power thus relieving the utility from transporting the peak

demand and saving the industry also from paying extra charges. This function of BESS is normally called load leveling.

(b) To feed critical loads when grid supply fails –thus acting as standby emergency power source.

(c) To provide voltage regulation at the load terminals by supplying / consuming reactive volt-amps from the electric grid.

(d) To balance the load from the grid point of view if the industrial load is unbalanced by providing power selectively to each phase of the three phase load. This function of the BESS is called load balancing .

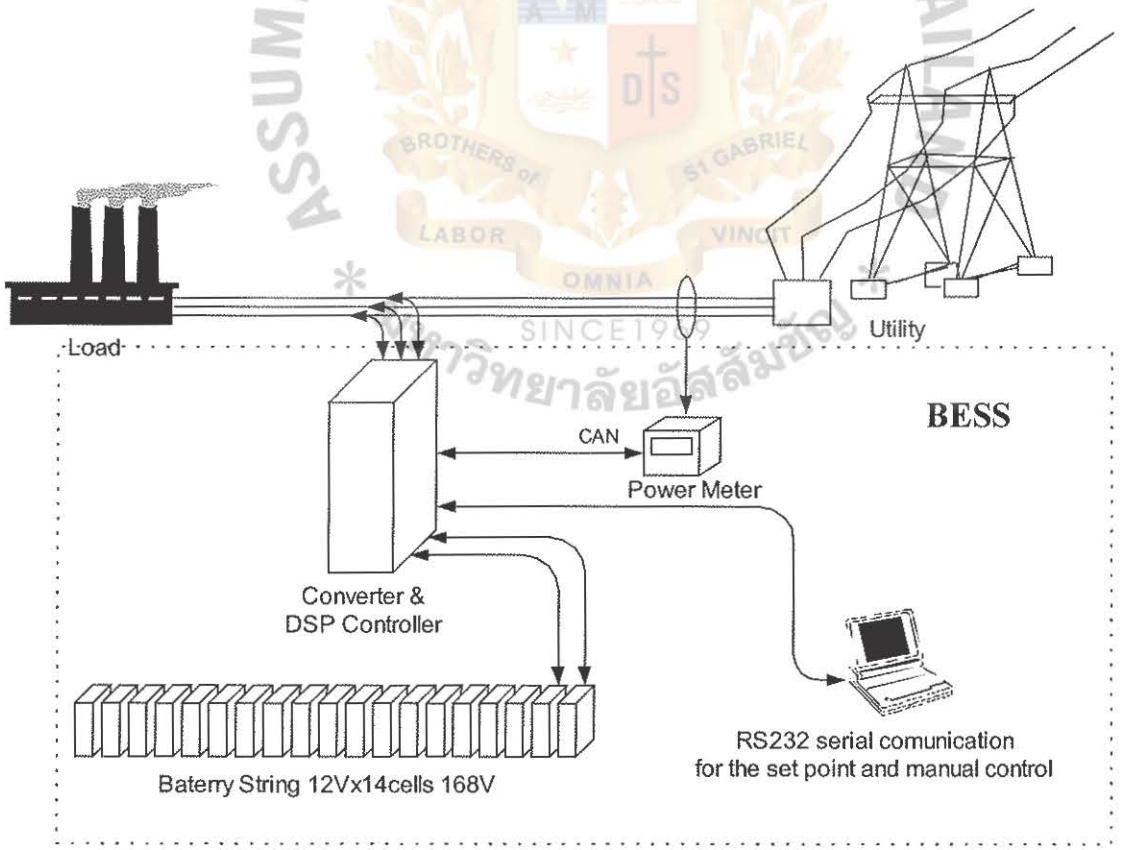

Figure1.1 BESS and its environment

In all the above areas of application the BESS reverts to charging mode and draws power from the electric grid to replenish the energy in the batteries. This happens when the industrial load is light or below normal.

The other potential areas of application of BESS are

(a) To convert the solar energy from the photo-voltaic arrays / wind energy (see figure 1.2) into three phase a.c at 50Hz and feed the power into the electric grid . In this mode of operation the photo-voltaic arrays / wind generator feed energy into the batteries which is converted into 3-phase a.c at 50Hz and fed into the power grid. This application may assume importance in future.

(b) To mitigate the harmonic currents generated by industrial nonlinear loads. This function is the active harmonic filter function in which case the battery is eliminated but a capacitor takes its place as a voltage source. No net energy transfer is involved. This is a sophisticated function.

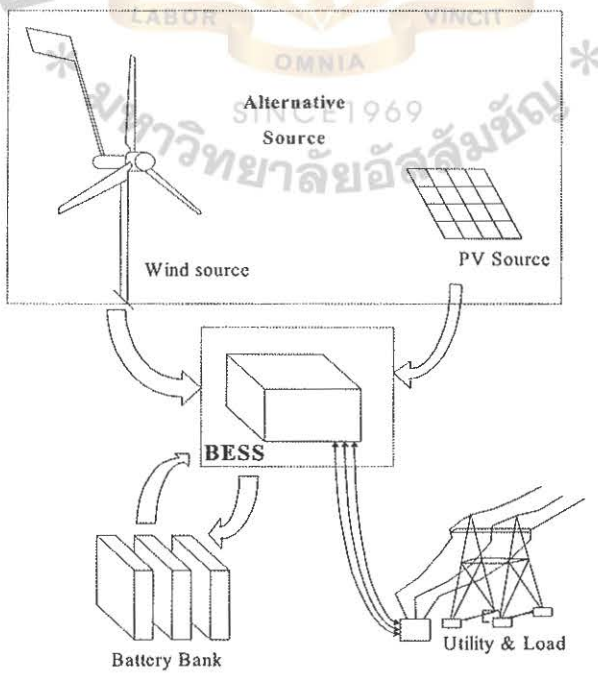

Figure 1.2 BESS with renew energy source

1.3 Details of some of the large scale BESS in operation worldwide

The many desirable features of BESS for dynamic control of power systems have been recognised and power utility companies have started installing BESS for power quality improvement. Some of the BESS installations already in operation in the world are given below:

(a) Chino site- 10MW/ 51.2MWh for load leveling[1],[2]

(b) Princeton site- 5MW/5MWh for peak shaving and area regulation[2]

(c) Puerto Rico site – 20MW/ 10MWh for frequency regulation[2],[3]

The biggest BESS installation ever constructed is currently (2002)being built by Golden Valley Electric Corporation. In order to have an idea of the magnitude of this installation the following statistics are given:

Funding US$ 35Million

13,760 liquid electrolyte filled Ni-Cd cells will be used

Each battery weighs 165 pounds

Total BESS weight 1500 tons

Anticipated battery life 20-30 years

Power output 40MW for 15 minutes

Floor area occupied is equivalent to a soccer field

Target date for completion December 2003

Now construction work is in progress.

1.4 Origin and Scope of the present work

The projects listed above are large scale ones and are meant for use in electric grid systems. Since BESS can easily interface with renewable energy sources such as solar energy(photo voltaic arrays), wind energy and fuel cells through the d.c link, many countries are encouraging small scale BESS installations (1-5kW)for households and commercial establishments. Large number of such small BESS installations in individual households will add up to a large scale BESS system with a positive effect to the power generation, transmission and distribution system on a national scale. This fact has been recognised in countries like Japan, USA. and residential buildings are encouraged to have small BESS with PV cells or Fuel cells as renewable energy sources. Even in Thailand (Bangkok) EGAT is encouraging the installation of such systems by providing subsidy and the required equipment. A few experimental systems are in operation under EGAT scheme .It is recognised that the needed technology and operational experience is to be developed indigenously and the dissertation presented herein is an effort in that direction. Hence the main objective of the present work is to develop appropriate converter technology including the controller software and then design, construct and test the BESS to obtain hands on operating experience.

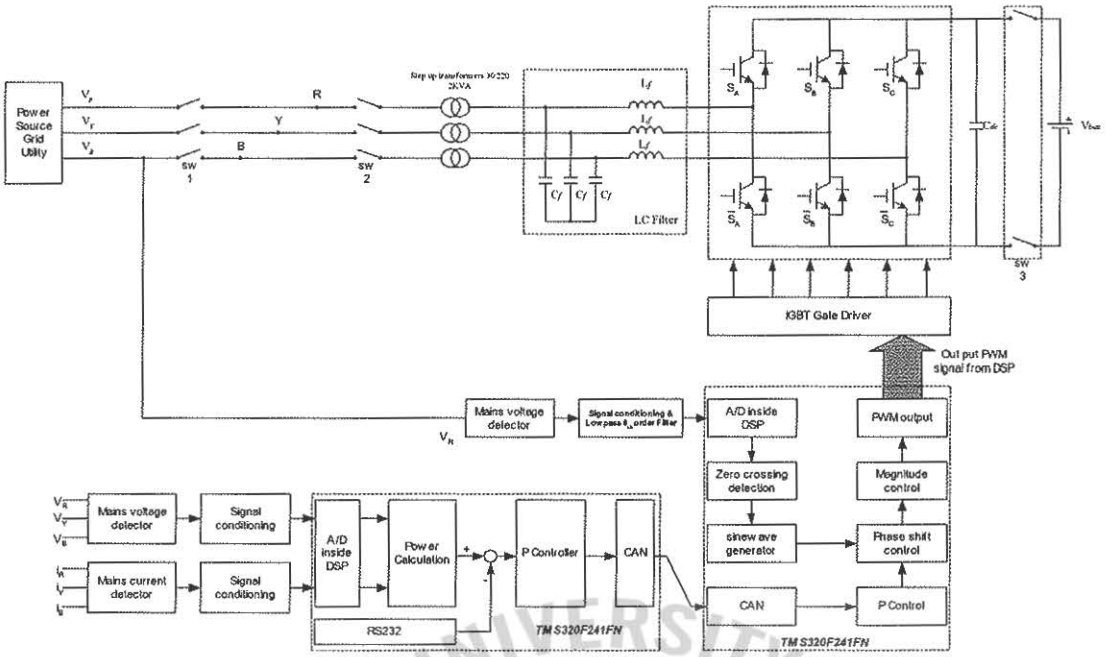

Figure 1.3 BESS system overview.

A block schematic of the system constructed is given in fig.1.3 . A brief description of the scheme is given below as a overview. The system consists of (a) Battery string- V_{batt} (b) 3-phase IGBT converter module (c) Gate driver (d) Two TI DSPs-TI 320F241N for controlling the inverter gate driver (e) Current and Voltage sensors (f) L-C filter for suppressing PWM generated harmonics (g) A step up transformer and associated contactors for connection to electric grid. A photograph of the BESS unit constructed is shown in fig.1.4. The IGBT module is switched at 10kHz using a PWM scheme to generate 3-phase ac output. An L-C filter is used to suppress the pwm generated harmonics so that the filtered output is sinusoidal at 50Hz. The d.c link voltage used is 168volts. A step up transformer is used to bring the converter voltage to 380volt line to line. At the heart of the system lie the two DSPs which are programmed to control the converter. The converter system is capable of operation on a stand alone basis feeding its own load or can operate in parallel with the power system after synchronization. In the later case the converter system is capable of bidirectional power and reactive power transfer between Battery system and the

electric power grid. In what follows more detailed descriptions are given in the subsequent chapters along with test results.

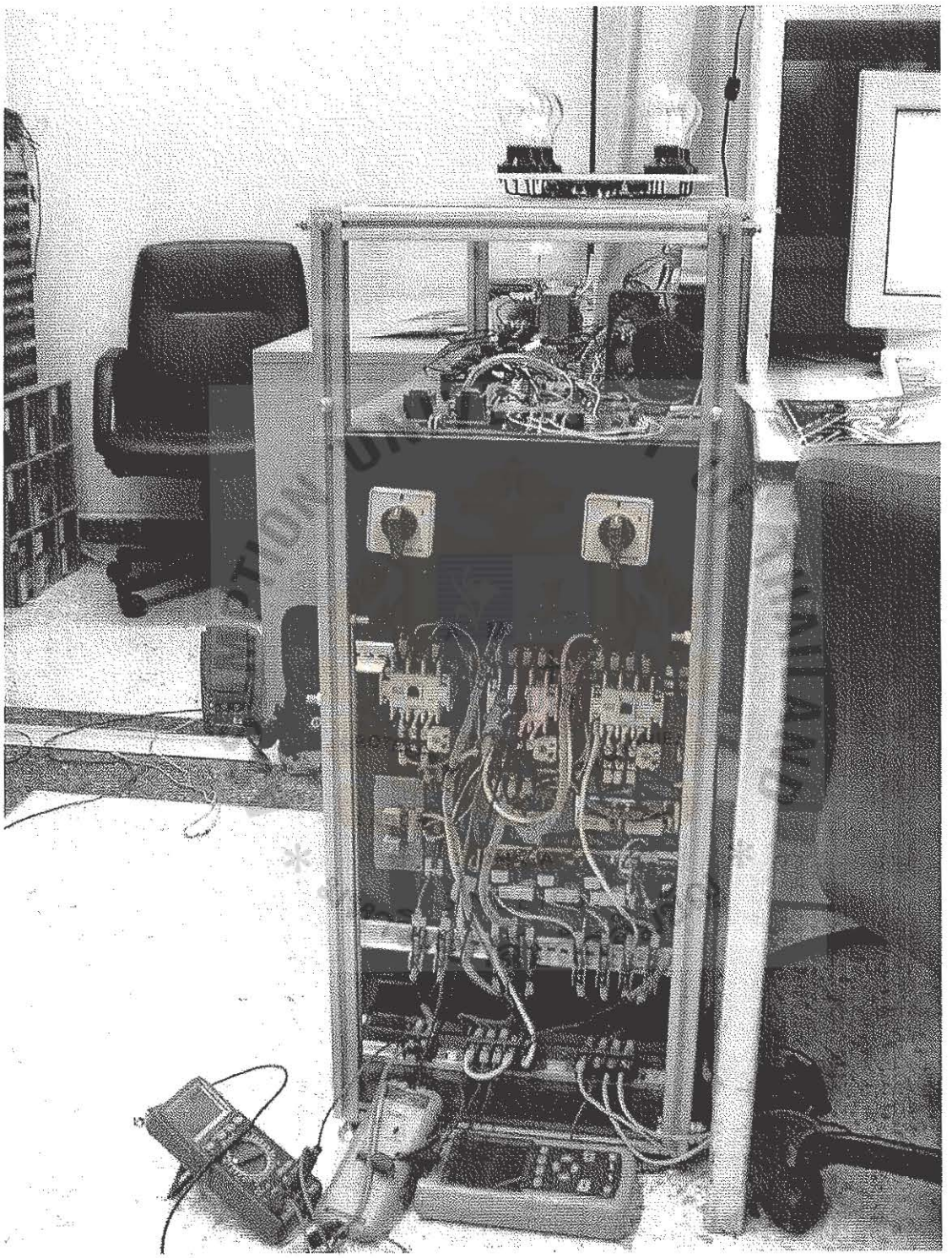

Figure 1.4 BESS unit Constructed

CHAPTER 2.

Principles of Operation of Battery Energy Storage System

2.1 Converting D.C to 3 Phase Sinusoidal A.C

2.1.1 Pulse Width Modulation Technique

In order to convert d.c voltage to a sinusoidally varying 3 phase a.c at 50 Hz, PWM technique is used to generate the required gating signals to the six IGBTs in the bridge form. The basic structure of the D.C to A.C converter used in this project is shown in the fig.2.1 below:

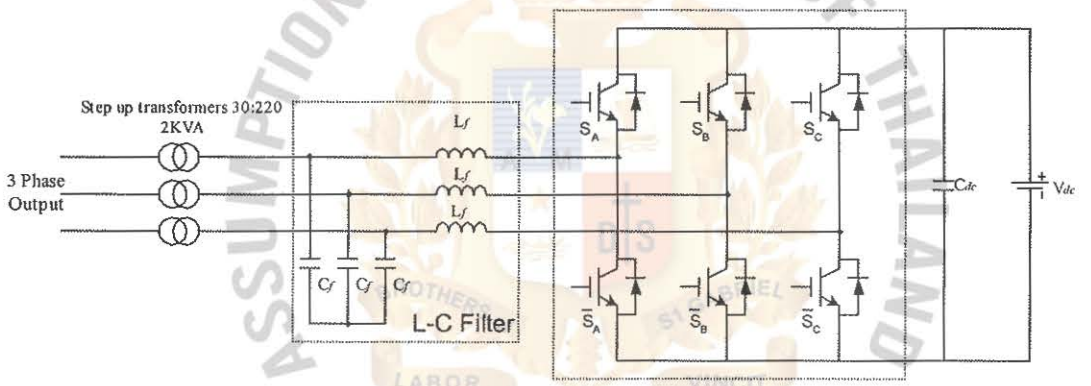

Figure 2.1 Structure of DC to AC Converter

The required gate drive signals are generated by comparing a reference sine wave at 50Hz with a triangular wave at the required switching frequency f_s.. In fig.2.2 is shown the 50Hz reference sine wave, the triangular wave at 1050Hz and the resulting PWM wave. The PWM wave will be used to switch the IGBTs which produce similar wave form at output but at higher voltage level. It can be seen that the average value of the PWM output is the desired reference sine wave. What is shown is for generating a single phase voltage from d.c. Similar schemes can be used by phase shifting the reference sine wave by 120 and 240 degrees electrical. In PWM switching we define Modulation index :

$$M_a = \frac{V_{reference}}{V_{tri}} \quad and \quad generally \quad 0 < M_a < 1 \qquad 2.1$$

Similarly the frequency modulation index is defined as

$$M_f = \frac{f_{switching}}{f_{1reference}} \qquad 2.2$$

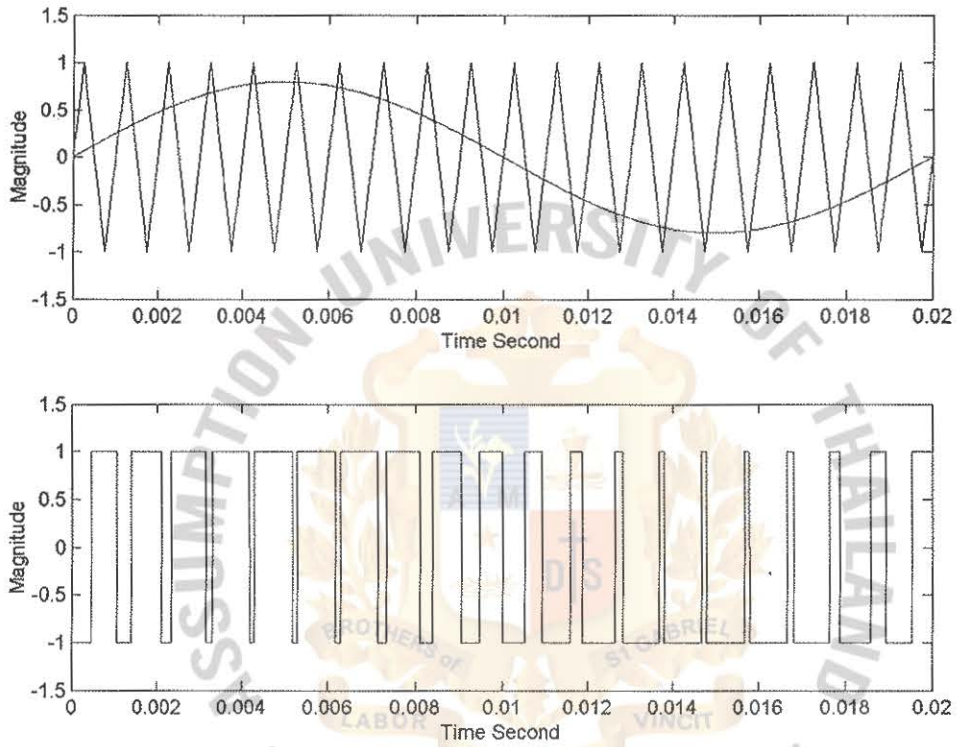

Figure 2.2 PWM Technique and switching waveform generated

Refer to fig.2.2 The waveforms are drawn for a modulation index M_a = 0.8 and M_f = 21 .The sine wave is the desired frequency at 50Hz and the triangular wave frequency is the switching frequency. The resulting pwm waveform is at switching frequency. The frequency spectrum is shown in the fig.2.3 and the dominant harmonic components are shown in table 2.1 for different modulation indices with M_f = 21. This table is adopted from Power Electronics by Ned Mohan.[4] It is stated in the reference that if M_f > 21 the amplitudes of the dominant components remain almost at the same values as given in the table 2.1

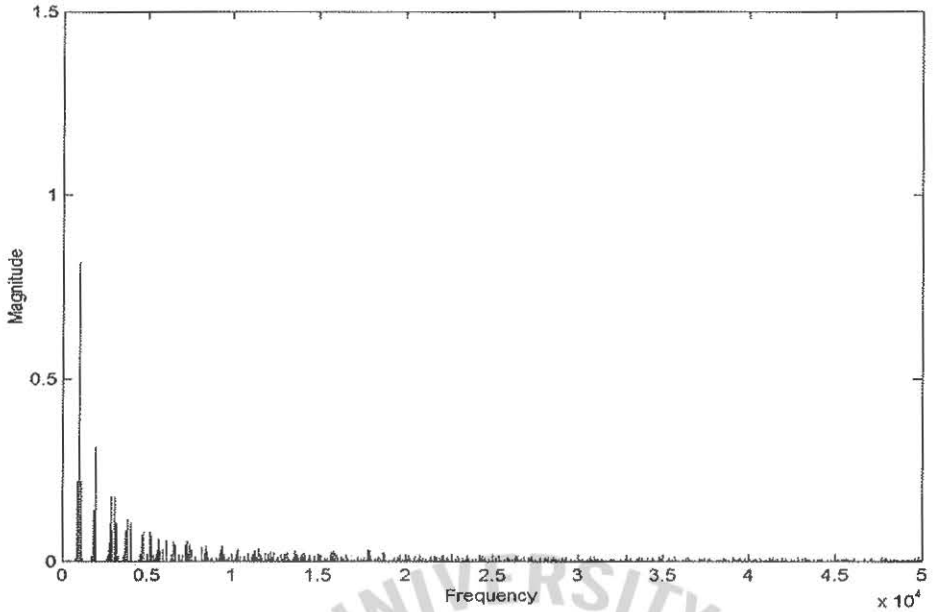

Figure 2.3 Frequency spectrum with $M_f = 21$ and $M_a = 0.8$

Table 2.1 Generalized Harmonics of PWM waveform at $M_f = 21$

M_a	0.2	0.4	0.6	0.8	1
M_f	1.2420	1.1506	1.0059	0.818	0.6009
$M_f \pm 2$	0.0155	0.0608	0.1311	0.2199	0.3180
$M_f \pm 4$	0.0000	0.0005	0.0025	0.0076	0.0178
$2M_f \pm 1$	0.1903	0.3260	0.3703	0.3143	0.1811
$2M_f \pm 3$	0.0033	0.0238	0.0707	0.1395	0.2123
$2M_f \pm 5$	0.0001	0.0005	0.0033	0.0128	0.0333
$3M_f$	0.3353	0.1233	0.0832	0.1706	0.1128
$3M_f \pm 2$	0.0436	0.1386	0.2035	0.1762	0.0620
$3M_f \pm 4$	0.0008	0.0116	0.0466	0.1044	0.1572
$3M_f \pm 6$	0.0001	0.0003	0.0035	0.0157	0.0437
$4M_f \pm 1$	0.1631	0.1571	0.0081	0.1052	0.0675
$4M_f \pm 3$	0.0119	0.0698	0.1323	0.1147	0.0093
$4M_f \pm 5$	0.0003	0.0064	0.0338	0.0842	0.1186
$4M_f \pm 7$	0.0000	0.0003	0.0033	0.0174	0.0502

Since switching frequency in our converter is at 10kHz, the frequency modulation index M_f = 200. The Matlab analysis has been used to find the amplitudes of the

dominant harmonics and are shown in the table 2.2. It can be seen that the amplitudes are almost same as given in the table 2.1 with Mf = 21. The frequency spectrum is shown in the figure 2.3. The dominant harmonic frequencies appearing in the output are obtained from the table are:

9.8 kHz, 9.9 kHz, 10 kHz, 10.1 kHz, 10.2 kHz, 19.75 kHz, 19.85 kHz,19.95 kHz, 20.05 kHz, 20.15 kHz, 20.25 kHz, 29.7 kHz, 29.8 kHz, 29.9 kHz, 30 kHz, 30.1 kHz, 30.2 kHz, 30.3 kHz, 39.65 kHz, 39.75 kHz, 39.85 kHz, 39.95 kHz, 40.05 kHz, 40.15 kHz, 40.25 kHz, 40.35 kHz. and so on.

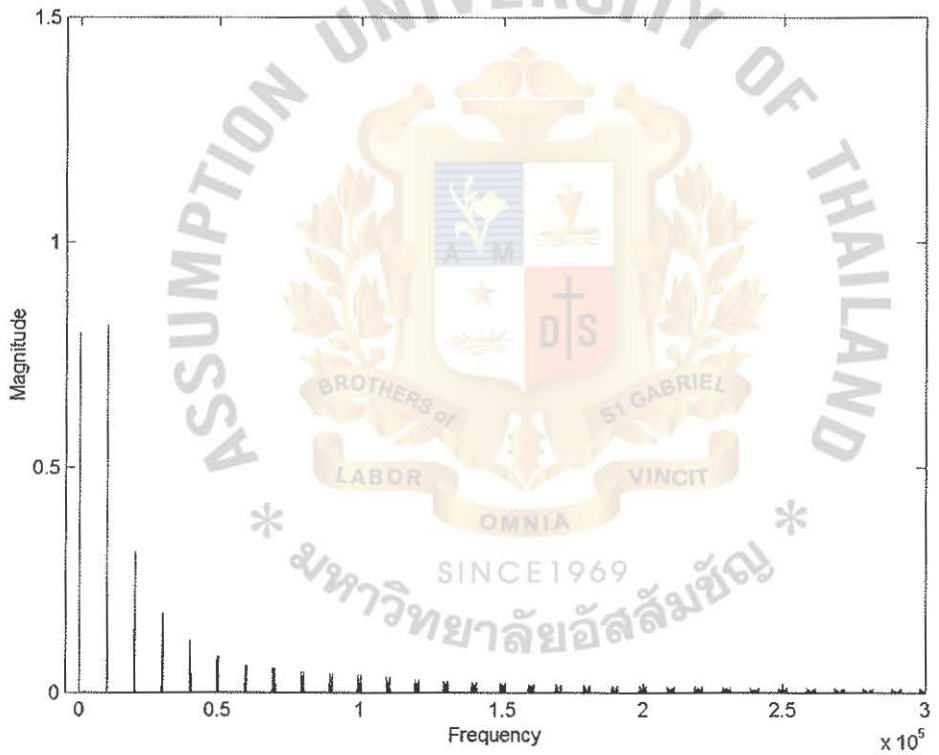

Figure 2.4 Frequency spectrum of PWM waveform at Ma is 0.8, f_s is 10kHz

Table 2.2 Generalized Harmonics of PWM waveform at $M_f = 200$

M_a	0.2	0.4	0.6	0.8	1
M_f	1.2421	1.1508	1.0059	0.8181	0.6009
$M_f \pm 2$	0.0153	0.0604	0.1311	0.2195	0.3177
$M_f \pm 4$	0.0001	0.007	0.0023	0.0077	0.0179
$2M_f \pm 1$	0.1902	0.3261	0.3702	0.3147	0.1814
$2M_f \pm 3$	0.0033	0.0236	0.0709	0.1393	0.2122
$2M_f \pm 5$	0.0002	0.0004	0.0032	0.0129	0.0333
$3M_f$	0.3354	0.1236	0.0832	0.1708	0.1129
$3M_f \pm 2$	0.0433	0.1383	0.2033	0.1764	0.0622
$3M_f \pm 4$	0.0010	0.0117	0.0468	0.1042	0.1571
$3M_f \pm 6$	0.0001	0.0003	0.0033	0.0157	0.0438
$4M_f \pm 1$	0.1631	0.1575	0.0082	0.1052	0.0677
$4M_f \pm 3$	0.0119	0.0694	0.1322	0.1149	0.0093
$4M_f \pm 5$	0.0001	0.0063	0.0340	0.0840	0.1186
$4M_f \pm 7$	0.0000	0.0001	0.0035	0.0175	0.0504

2.1.2 Harmonic Filter

In order to recover the sine wave at 50Hz from the PWM output from the IGBT bridge, it is necessary to filter out the harmonics at switching frequency as can be seen from the frequency spectrum. A low pass L-C filter is connected to the bridge output (Please see figure 2.1). The filter configuration is as shown below.

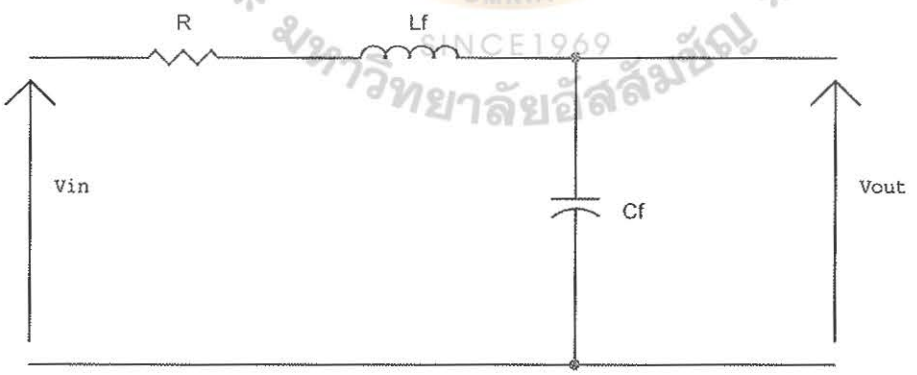

Figure 2.5 R L C filter circuit

The transfer function of the filter is given by

$$\frac{V_{out}}{V_{in}} = \frac{1}{S^2 L_f C_f + SRC_f + 1} \qquad 2.3$$

Then frequency response of the filter is as shown in figure 2.6

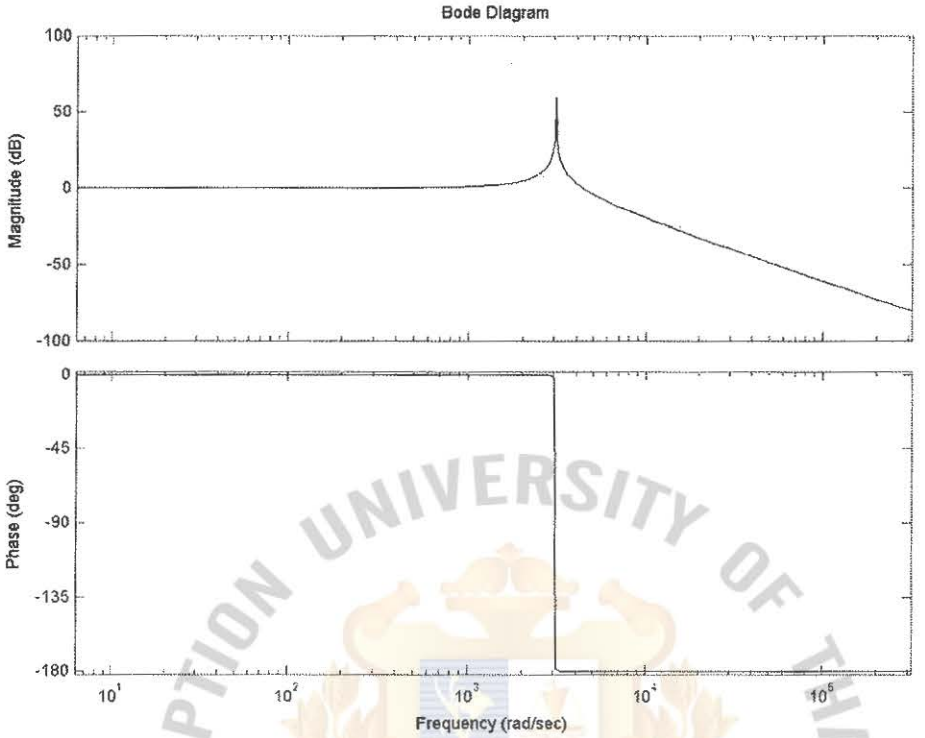

Figure 2.6 Frequency response of Filter circuit L = 2 mH, C = 1μF, R=0.3719Ω

The filter components are chosen such that the resonant frequency is 3050 rad/sec (485.4Hz). This frequency has to be away from the desired 50Hz so that the attenuation is low at 50Hz frequency and at the same time cut off the dominant harmonics (>10kHz). Attenuation 0.0926 dB, Phase shift 1.0107 deg at 50 Hz. Attenuation –52.5446dB , Phase shift -179.8301 deg at 10kHz..This shows that the 50Hz frequency component appears at the output with almost zero attenuation and phase shift whereas the 10kHz component is reduced to 0.23% (-52.5dB)of its input value. Other harmonics are reduced further down.

2.2 Steady State Performance Equations of BESS

The BESS can be regarded as a 3-phase 50Hz a.c source with bi-directional power and reactive power flow capability. On a single phase basis BESS can be thought of as a.c generator connected to a.c grid with an equivalent impedance interposed

between BESS and grid. Of course the BESS is to be synchronized to the electric grid in the usual way by making the amplitude, frequency and phase of BESS voltage same as that of electric grid. Figure 2.7 gives such an arrangement which will be used to develop the power and reactive power flow equations and the steady state operating chart for the BESS. The steady state vector diagram is also shown.

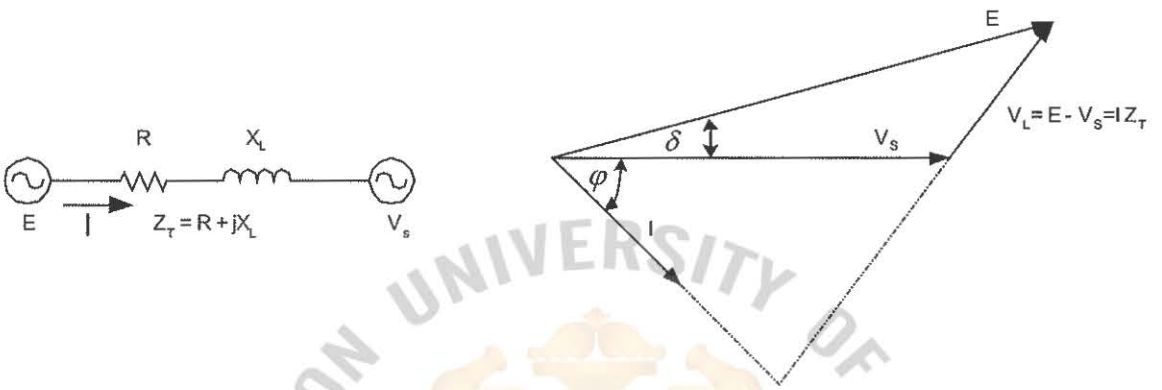

Figure 2.7 Equivalent circuit and vector diagram.

From Figure 2.7 E is inverter voltage, V_S is utility voltage and Z_T is the impedance between two source all on per phase basis. The impedance connecting the two sources is referred to the grid and is made up of the filter and the step up transformer (see figure 2.1) . It will be assumed in what follows that the supply voltage V_S forms infinite bus and the converter voltage magnitude E and its phase angle δ are variable and under control. Hence the resulting current is from the voltage difference between E and V_S divided by Z_T. Power flow can be controlled by three main parameters, first is the impedance between two sources Z_T, second is the amplitude of each source E or V_S, and third is the phase difference between two sources δ. In this case, V_S is fixed and it depends on the utility. The impedance Z_T is fixed and it depends on the converter characteristic, filter and step up transformer and thus the variables are only E and δ. The equations developed below are under steady state conditions.

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LABOR
VINCIT
OMNIA
SINCE1969
มหาวิทยาลัยอัสสัมชัญ

$$|E| = \sqrt{(V_S + IZ_T \cos(\theta - \varphi))^2 + (IZ_T \sin(\theta - \varphi))^2} \quad 2.15$$

$$\delta = \tan^{-1}\left[\frac{IZ_T \sin(\theta - \varphi)}{V_S + IZ_T \cos(\theta - \varphi)}\right] \quad 2.16$$

$$Z_T = \sqrt{R^2 + X_L^2} \quad 2.17$$

The equations developed above are standard equations encountered in the operation of a Synchronous Machine connected to an infinite bus. The BESS system can be regarded as a synchronous machine but static in nature.

The power and reactive power equations are plotted as a function of δ called load angle in the graphs shown in figure 2.8 . Grid Voltage and Inverter Voltage are fixed at 220V and Inductance value is 107.62mH, Resistance is 20 ohms and angle δ is varied from -180 to 180 degree.

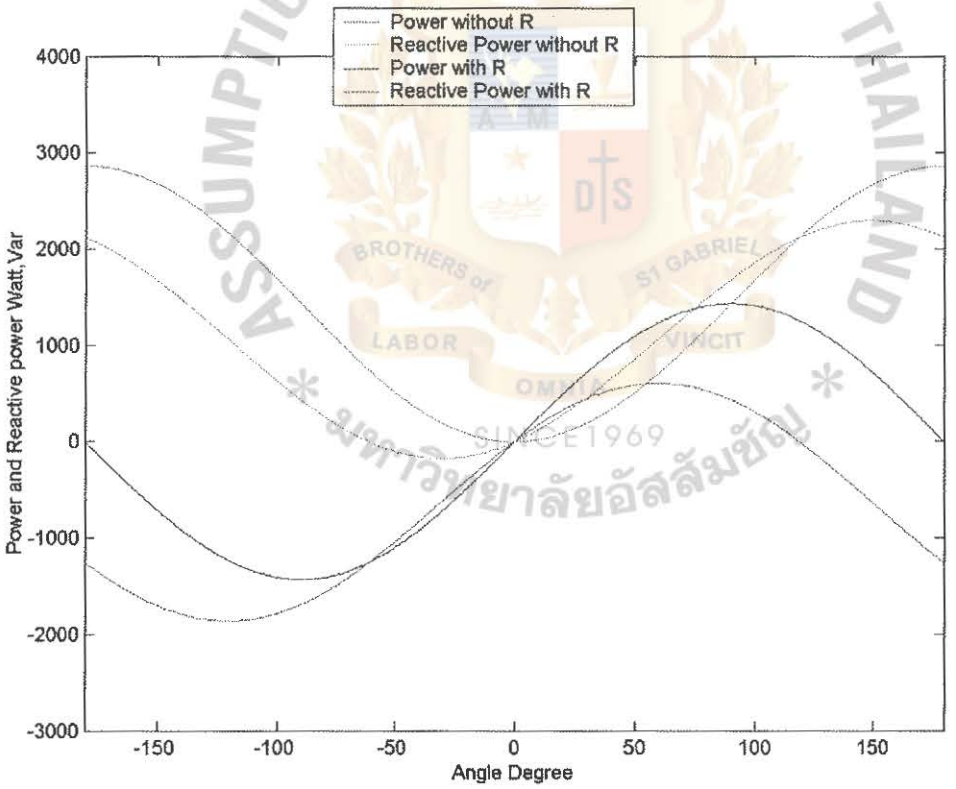

Figure 2.8 Power and Reactive Power plots.($V_S = E = 220V$)

From figure 2.8 power can be positive or negative and is controlled by adjusting the angle δ which means power can flow from BESS to grid or from grid to BESS. Same

applies to reactive power. Using the same equations but with different value of E the graph of power and reactive power are plotted in the figure 2.9. Grid Voltage is at 220V, Inverter Voltage is fixed at 340V and Inductance value is 107.62mH, Resistance is 20 ohms, angle δ vary from -180 to +180 degrees.

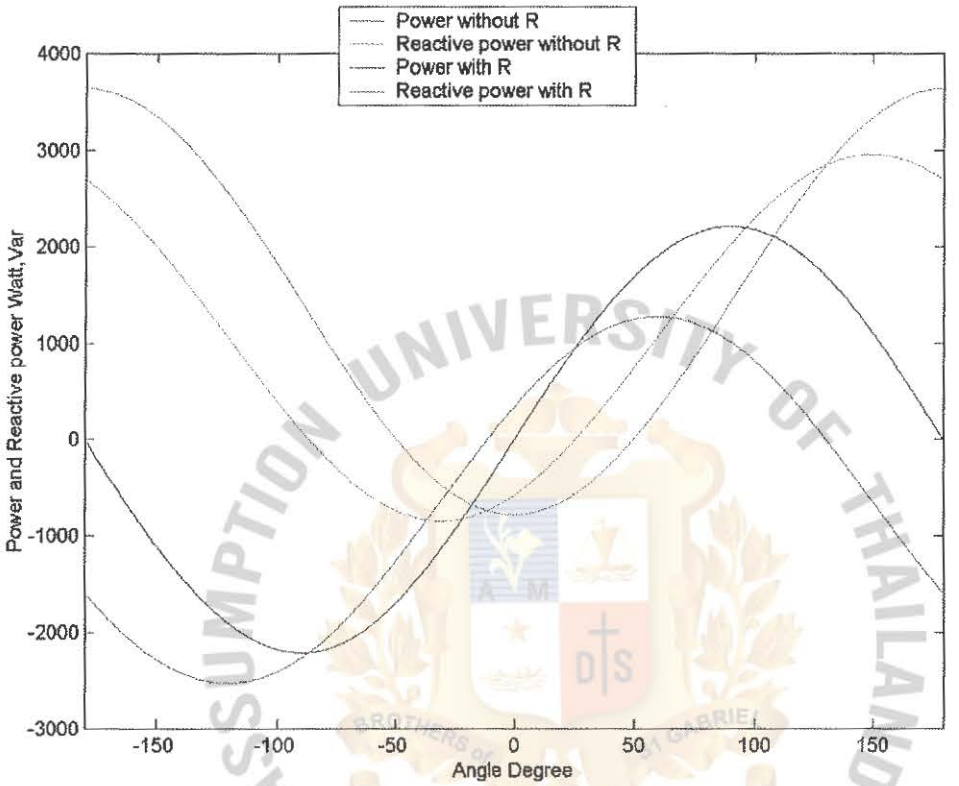

Figure 2.9 Power and Reactive Power plot (V_S = 220V, E = 340V)

From figure 2.9, increase in magnitude of E will have an effect to both power and reactive power. In case of power the maximum point of power transfer can get more than change phase only, a reactive curve can be positive and negative so that mean reactive power can be adjusted by increasing inverter voltage. Hence to meet the power transfer need we have to adjust both phase and magnitude of the internal voltage E of the converter. The maximum power transfer will happen at maximum of sinδ. However this is only a theoritical proposition as the current rating of the devices impose a practical limitation on the variation of the load angle δ .The power flow and reactive power flow are limited as shown in figure 2.10 as bound by the solid curve.

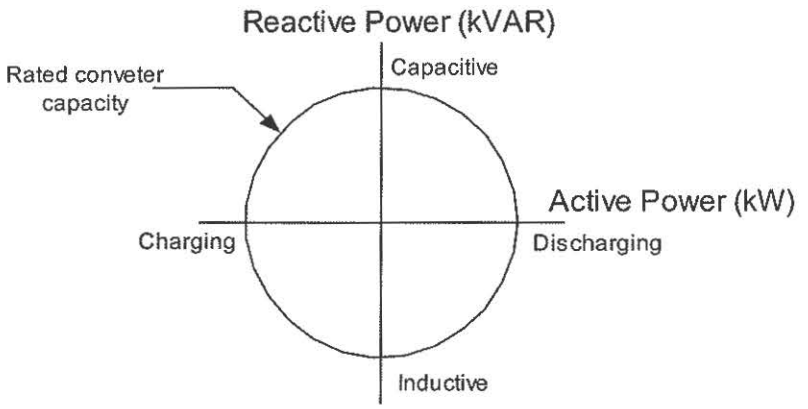

Figure 2.10 Active and Reactive Power Capability

Power and reactive power can be controlled in all four quadrants but not beyond the edge of the rated converter capacity which limit the variation in the value of angle δ and also on the amplitude of inverter voltage. The energy (kW.hr) is limited by the ampere-hour rating (A.hr) of a battery.

Figure 2.11 shows the vector diagram in which the current amplitude is kept constant but its phase angle φ is varied from 0-360 degrees thus making the converter to operate in all the four quadrants of the P-Q plane. The vector diagram will be used to calculate the magnitude and phase angle δ of the converter internal voltage E. The tip of E vector will trace a circle as the current phase goes through 0-360 deg. as shown in figure 2.11 .

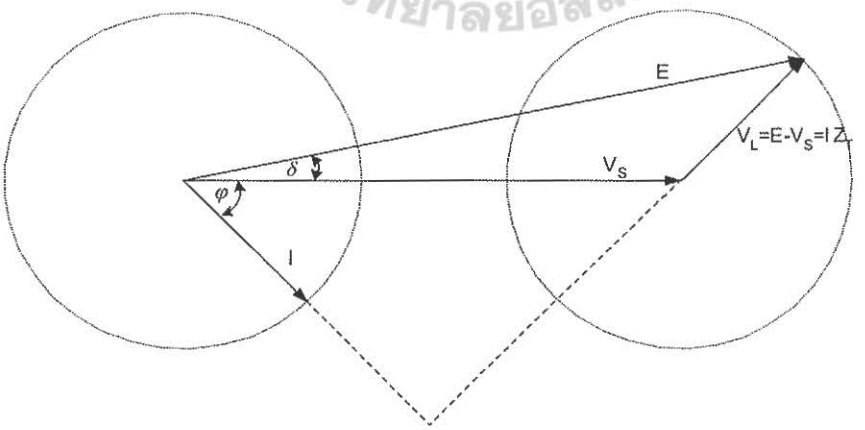

Figure 2.11 Phasor Diagram showing the effect of the power factor on E and δ

For a given current magnitude and power factor angle φ it is possible to find the magnitude and phase δ of the converter internal voltage E and the same is recorded in tables 2.3 and 2.4 The locus of the E vector is plotted in the figures 2.12 and 2.13 The equations used for this purpose are given below :

$$|E| = \sqrt{(V_S + IZ_T \cos(\theta - \varphi))^2 + (IZ_T \sin(\theta - \varphi))^2}$$

$$\delta = \tan^{-1}\left[\frac{IZ_T \sin(\theta - \varphi)}{V_S + IZ_T \cos(\theta - \varphi)}\right]$$

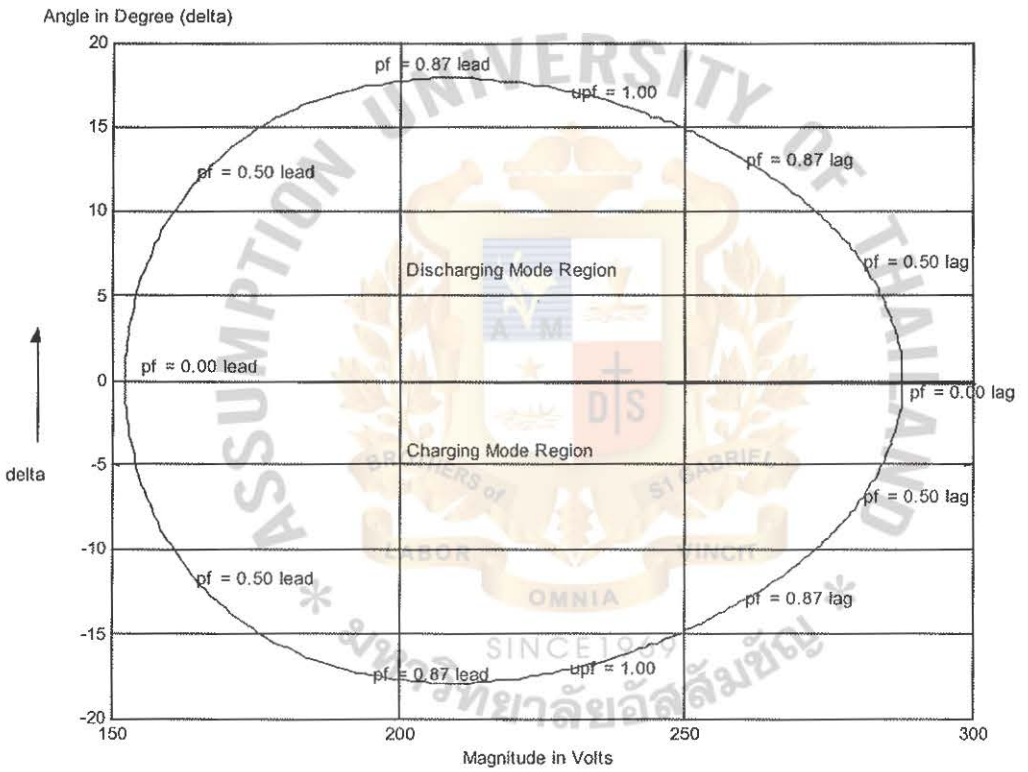

Figure 2.12. δ VS E, |I| is 2A, V_S is 220V, R is 0, L is 107.62 mH and ϕ is vary from 0 to 360 degree

If the load angle δ is negative that means the E vector lags the grid voltage vector V_S the BESS is in charging mode and receives power from the grid to charge the battery. The power factor of the current drawn depends on the magnitude of E . So charging can be done at leading or lagging power factors as can be seen from the fig.2.12 and 2.13.This has an implication for correcting the power factor of an industrial load and

affect the voltage control at the point of common coupling. Similarly for positive values of δ- that means E leading grid voltage V_S , the BESS will be in discharging mode thus supplying power with power factor leading or lagging.

Table 2.3 Value of ϕ, cos ϕ, |E| and δ for each point in figure 2.12

Φ	cosϕ	|E|	δ
0	1	230.157	17.0854
30	0.866	195.182	17.4593
60	0.5	164.942	11.8283
90	0	152.38	0
120	-0.5	164.942	-11.828
150	-0.866	195.182	-17.459
180	-1	230.157	-17.085
210	-0.866	260.478	-12.992
240	-0.5	280.605	-6.9203
270	0	287.62	0
300	0.5	280.605	6.9203
330	0.866	260.478	12.9922
360	1	230.157	17.0854

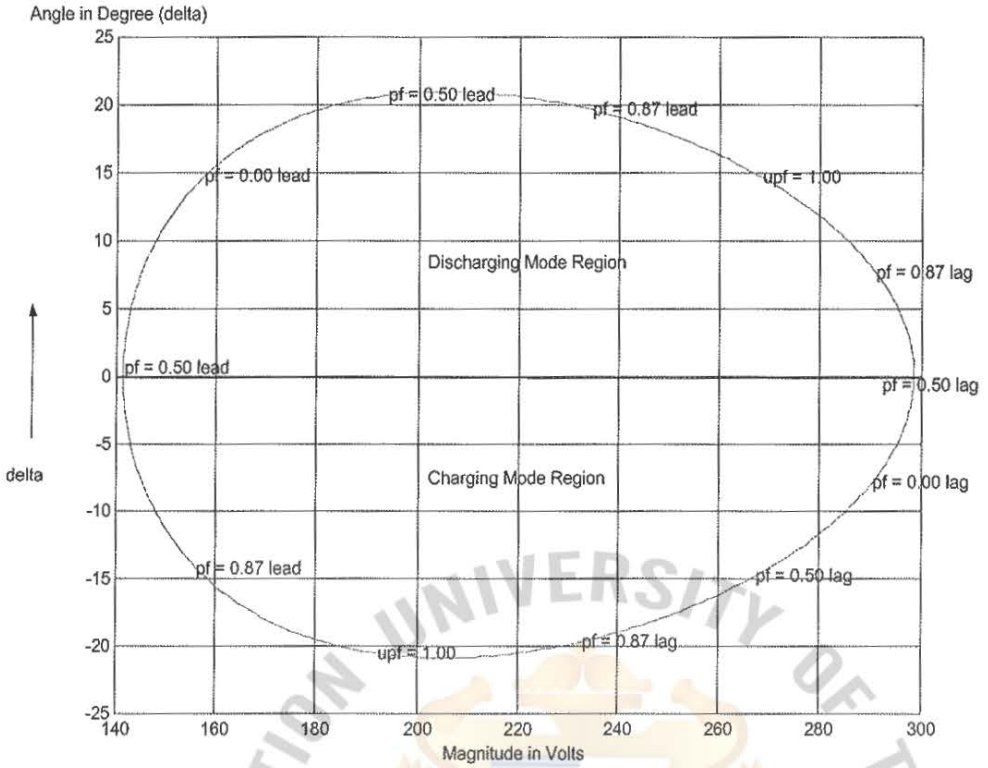

Figure 2.13 δ VS E, |I| is 2A, V_S is 220V, R is 20Ω, L is 107.62 mH and ϕ is vary from 0 to 360 degree

Table 2.4 Value of ϕ, cos ϕ, |E| and δ for each point in figure 2.13

Φ	cosϕ	|E|	δ
0	1	268.6492	14.5783
30	0.866	234.3889	19.5829
60	0.5	193.9223	20.6697
90	0	157.5429	14.7084
120	-0.5	141.4421	0.3367
150	-0.866	156.3779	-14.2755
180	-1	192.2821	-20.5894
210	-0.866	232.8233	-19.72
240	-0.5	267.4677	-14.8282
270	0	290.3878	-7.9175
300	0.5	298.5615	-0.1595
330	0.866	291.0168	7.6142
360	1	268.6492	14.5783

The Values of E and δ listed in the tables are important in the sense that they form an operating chart for the BESS. What is meant by this is that if we want to set the amount of current and power factor for the bess, then the required values of E and δ can be obtained from the tables. The BESS is controlled by a microcontroller-TI DSP TM320F241 which will be described later on. In order to set E and δ certain control words are to be fed to the controller and there is a set of control words corresponding to each value of E and δ.

CHAPTER 3

BESS System Description and Component Specification

3.1 System Overview and Modeling

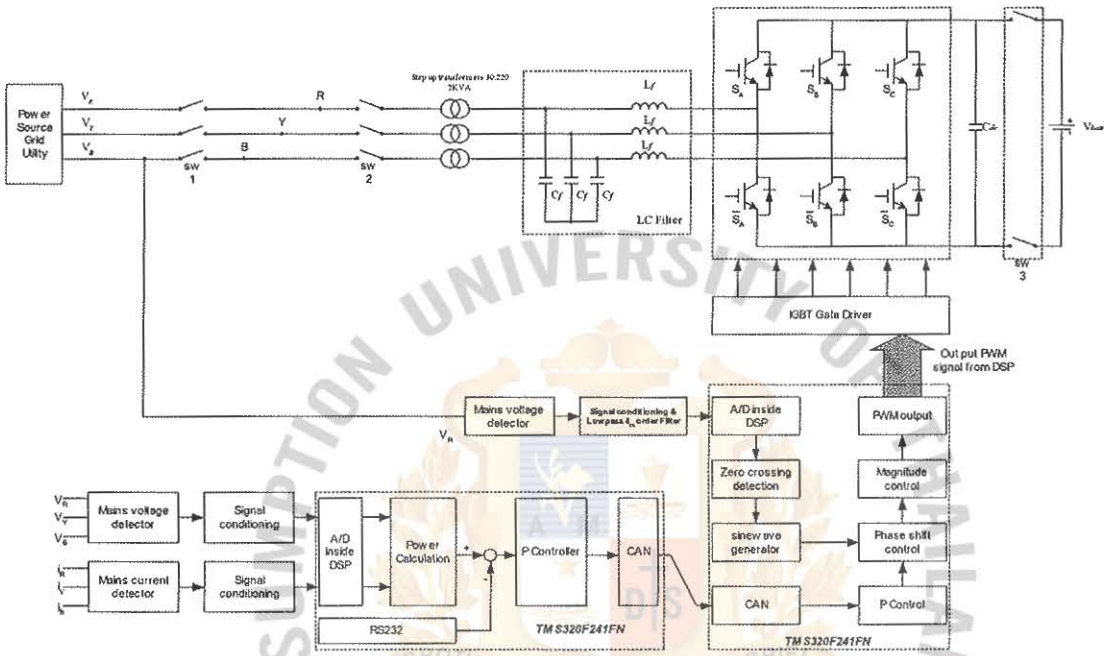

Figure 3.1 System overview

The main functional blocks of the BESS system constructed are shown in fig.3.1. The important blocks that constitute the system are:

1. Battery string (V_{batt})
2. Inverter bridge and gate driver
3. LC filter for harmonic filtering
4. Step Up transformer
5. Sensing and signal conditioning circuit
6. DSP controller for the power monitoring
7. DSP controller for inverter control

The details of each of these system blocks are described with their specifications

3.2 Description of system blocks and their specifications

Figure 3.2 Sealed Lead Acid Battery

3.2.1 Battery string

This is the battery bank consisting of 14 numbers of sealed lead acid batteries with a nominal voltage of 12 volts (see fig.1). The battery bank is the main energy storage system.

Specification :

12V -20AH

Standby use:13.50-13.80V

Initial current: Less than 6A

Each cell voltage is 12V -20 Ah hence the DC link voltage become 168V and can supply energy at 3360 watt for an hour. DC link will limit the maximum output voltage of the converter.

3.2.2 Inverter Bridge and gate driver

Switching module that is used here is the IGBT module " SKM 40 GD 123 D " from SEMIKRON.

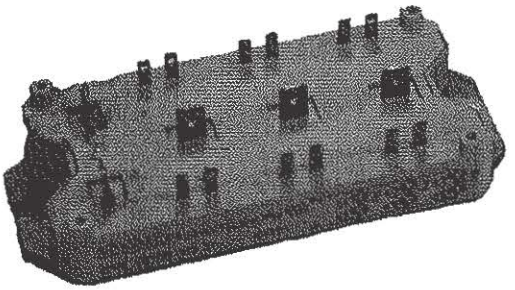

Figure 3.3 IGBTs Device

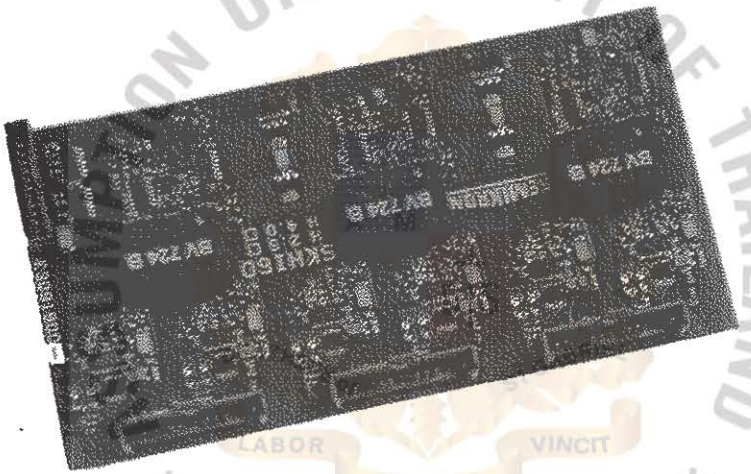

Figure 3.4 IGBTs Driver Board

It can stand a maximum current of 40A, V_{CE} rated at 1200V. The gate driver module is SKHI60- also from SEMIKRON. The D.C supply voltage 15V, Turn-on gate voltage is 15V, Turn-off output gate voltage is 0V, V_{CEsat} is 7V, Interlock dead time 3 usec. The detailed specification sheets from the manufacturer for the IGBT module and for the gate driver are given in the appendix.

We can get an idea of the rms value of the fundamental voltage on per phase basis from the equation:

$$V_{rms} = M_a \frac{V_{dc}}{2\sqrt{2}}$$

If the modulation index M_a is varied between 0.1 to 1, and V_{dc} from battery is 168V, then the range of output voltage V_{rms} possible per phase from the inverter become

$$V_{rms} = M_a \frac{V_{dc}}{2\sqrt{2}}$$

$$0.1 \le M_a \le 1$$
$$5.94V \le V_{rms} \le 59.4V$$

The actual voltage available at the terminals of the inverter will be less than this in practice due to finite drop in the devices and due to blanking time . This aspect will be considered in the testing phase of the inverter.

3.2.3 L C Filter :

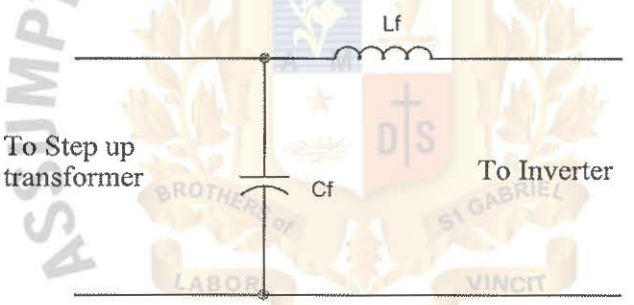

Figure 3.5 LC filter

Inductor value is 4 mH 15A. Two of inductor are connected in parallel to get 2mH pwer phase. The capacitor value is 1.5uF 400VAC.

3.2.4 Step Up Transformer Bank:

Since the output voltage available per phase from the inverter and filter combination is less than the electric supply voltage of 220 volts per phase, three single phase transformers connected in star/star are used as a transformer bank to step

up the voltage of the inverter to the supply level. The ratings of the transformers used and the equivalent circuit parameters are given below:

Transformer Specification

Single phase transformer

Ratio	:	30:220 (7.333)
Power	:	1kVA

From Open circuit and Short circuit test the parameter of transformer become

Megnetizing Inductance refer to LV	:	0.6006H
Leakage Inductance refer to LV	:	0.03mH
Resistance refer to LV	:	0.0238Ω
Leakage Inductance refer to HV	:	1.62mH
Resistance refer to HV	:	1.281Ω

3.2.5 Signal conditioning and filter circuits

(a) Voltage signal conditioning

The system must synchronize to the utility hence the controller need the phase information to adjust the phase change of output inverter and decide to close the synchronizing contactor. Phase information is sensed by the step-down transformer then pass the signal to the signal conditioning and noise filter circuit. Phase information will lag the real value for one cycle. The delay of the signal will be compensated by the program. Controller is DSP TMS320F241FN, it has A/D input resolution 10 bits, input vary from 0-5 V. But the V_{L-N} sensed by the transformer is AC voltage so it needs the signal conditioning circuit to offset the voltage up to 0-4 V to give to the input of noise filter cirucit as shown in figure 3.2

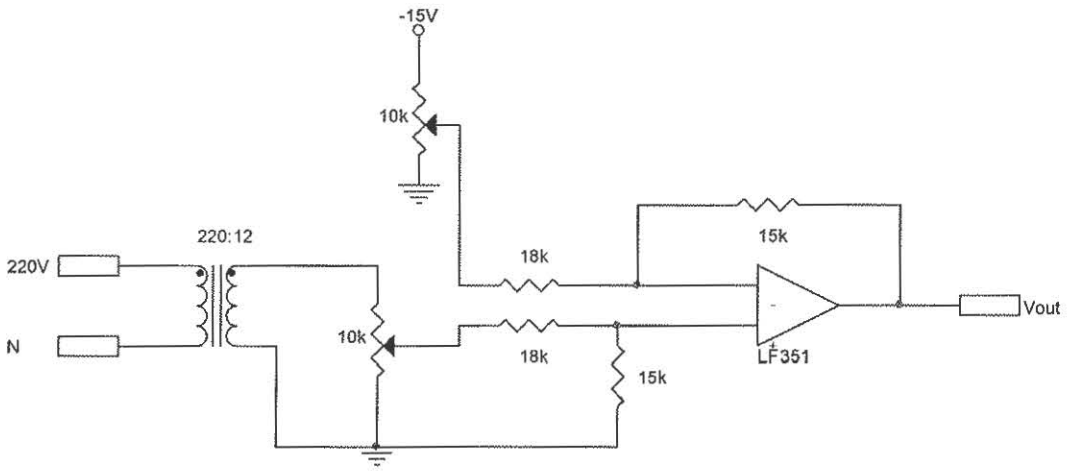

Figure 3.6 V_{AC} sensing and off set the signal

$$R_1 = R_2$$
$$R_3 = R_f$$
$$V_{out} \approx (V2 - V1)\frac{R_f}{R_1}$$
$$-15 < V1 < 0$$
$$-1.67 < V2 < 1.67$$
$$0 < V_{out} < 4$$
$$\frac{R_f}{R_1} = 1.2$$
$$R_1 = R_2 = 15k\Omega$$
$$R_f = R_3 = 15kx1.2 = 18k\Omega$$

Then Input and Output range of V_{AC} sensing-signal conditioning is become

$$-310V \le V_{in} \le 310V$$
$$0V \le V_{out} \le 4V$$

8^{th}-order, low pass , switched-capacitor filters (MAX 291) is use to filter the noise from output of the sensing and signal conditioning before give to the A/D of Controller which have a circuit in figure 3.3

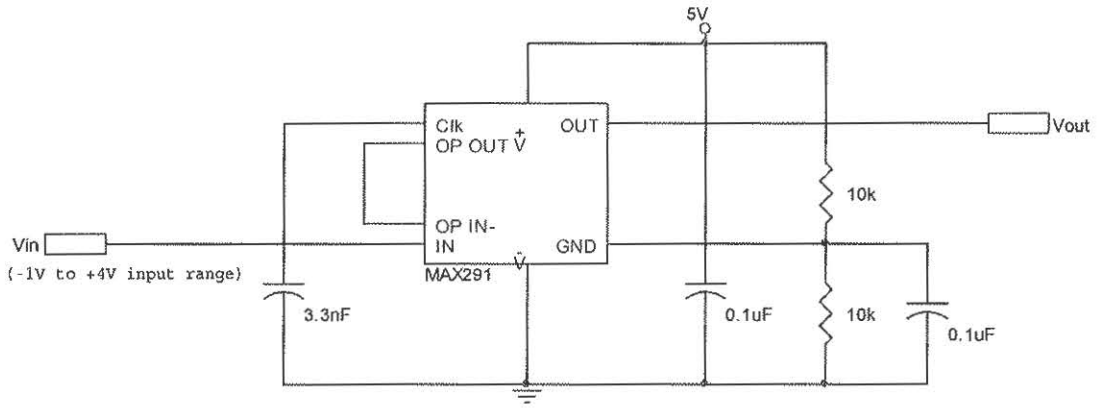

Figure 3.7 MAX291 8th order low pass filter

The application of MAX291 is 50Hz/60Hz Line-Noise Filtering which all detail such as cut-off frequency is provided in datasheet in the appendix. The Input and Output range of filter circuit become

$$-1V \le V_{in} \le 4V$$

$$0V \le V_{out} \le 5V$$

For the power monitoring part DSP TMS320F241FN is use to calculate the power and send the control signal to the phase change controller part. The V_{AC} sensing and current sensing are required the V_{AC} sensing and signal conditioning is use the same circuit as shown in fig. 3.3

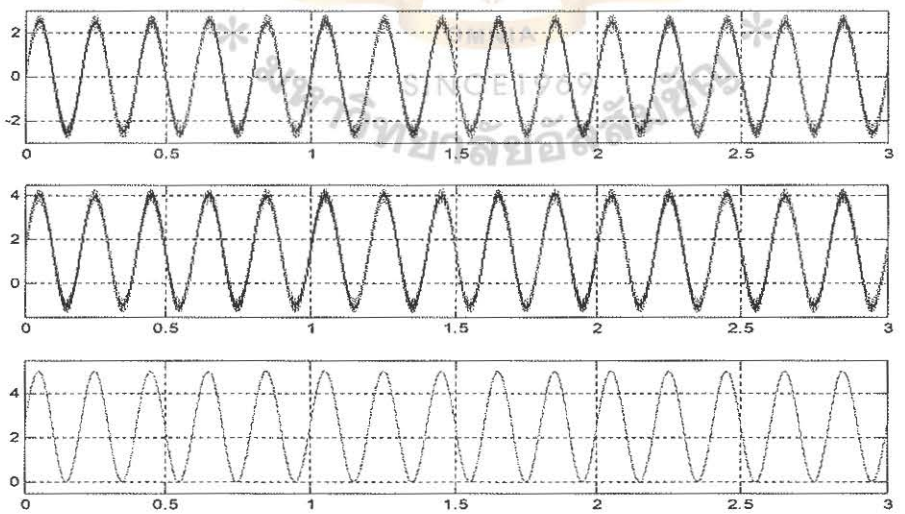

Figure 3.8 (a) input to signal from step down transformer, (b)off set a.c signal , and (c) output waveform after the filter.

(b). Current signal conditioning

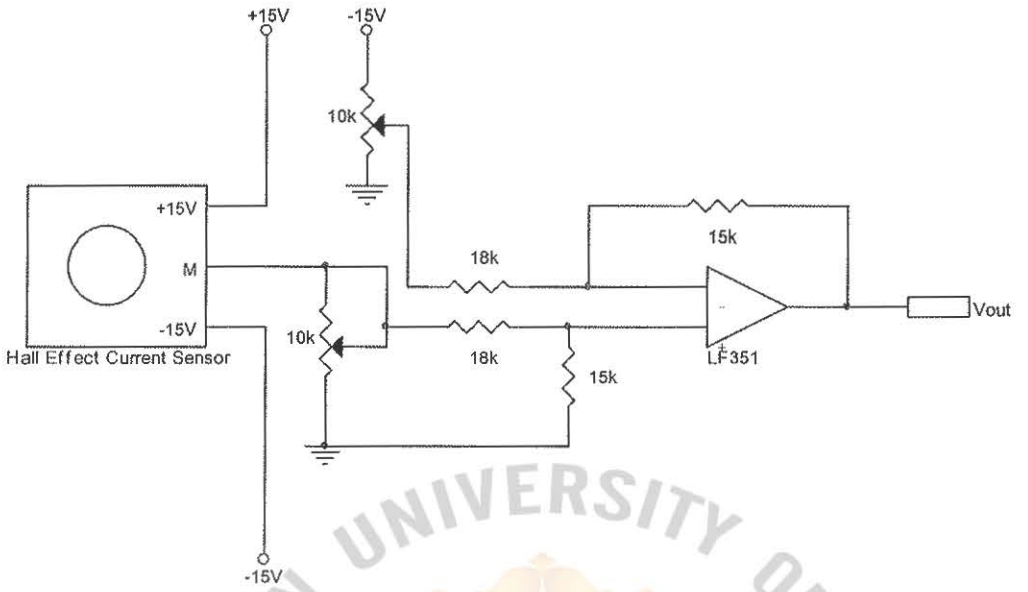

Figure 3.9 Current sensing and signal conditioning

For the current sensing and signal conditioning circuit is shown fig. 3.5 Current hall effect sensor (EL 50 P1) specification is 1A:1mA, maximum current is 50 Arms. The signal conditioning circuit is differential amplifier circuit. The Input and Output range of current sense and signal conditioning circuit become (The value of current is the magnitude of current when measure by current probe)

$$-7A \leq I_{in} \leq 7A$$

$$0V \leq V_{out} \leq 5V$$

3.2.6 DSP TMS320F241N

The DSP Controller has 8K words x 16 bits of flash EEPROM, Eight Compare PWM channels with dead band, Single 10-Bit Analog-to-Digital Converter (ADC) Module with 8 Multiplexed Input channels, Controller Area Network (CAN) Module, Serial Communications Interface (SCI). The crystal that is used for the CPU is 5MHz, however the inside DSP chip have a multiplier so the CPU will run at 20MHz or 20MIPS (Million Instruction per second).

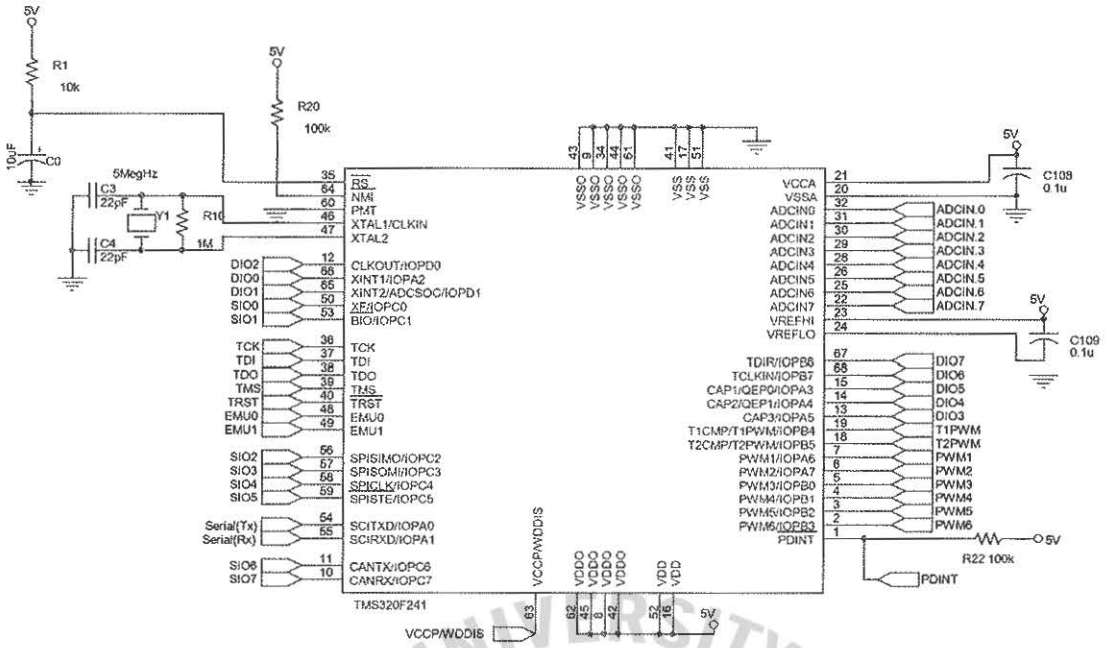

Figure 3.10 DSP circuit

The circuit in figure2 is the RS232 chip which use to connect the serial communication of DSP chip to computer.

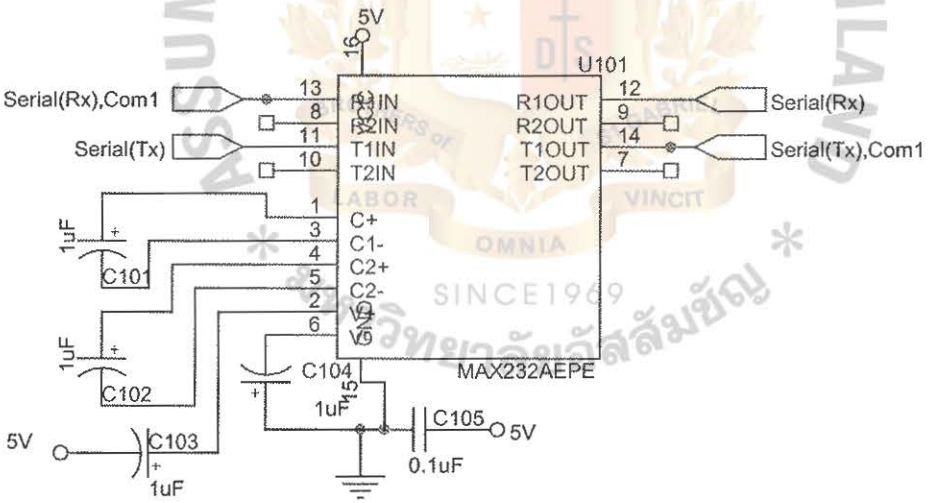

Figure 3.11 RS232 Connection

Dead-band provide by DSP can calculate by [xx]

Dead-band = Period x Dead-band Prescaler x CPU clock

Example:

DBT3-DBT0	= 0001 (Period)
DBTPS2-DBTPS)	= 001 (Prescaler) = 2
CPU clock	= 50 nsec.
Dead-band	= 1x2x50 nsec = 100 nsec

PWM Generator, the frequency of triangular is up to the counter. Because the Counter register is 16-bits hence the maximum count is 2^{16}. One count is one CPU cycle time hence the for the full time range of count is 2^{16} x 50nsec for an count up and 216 x 50nsec for an count down. Hence the frequency of the triangular become 2 x 2^{16} x 50nsec which is equal to 0.1 second. That mean if the counter is set to count in full length of 16-bits will give a triangular frequency at 10Hz. The way to increase the frequency of triangular is to reduce the number of count. However the resolution for the compare unit to compare with the input value to get pwm will decrease.

Example:

Count up	= 1024
Count down	= 1024
Time consume is	= 2x1024x50nsec
	= 102400nsec = 102.4usec
Triangular frequency	= 1/102.4usec = 9.7656kHz

The compare unit will compare the input value with the counter and if it equal will give one or zero (the one or zero output can be set by the control register) to the pwm output pin.

CHAPTER 4.

Performance Testing

In this chapter performance tests conducted on the constructed BESS system are described . In particular the following tests are conducted to evaluate the performance of the software and the hardware components of the system. The tests conducted are:

1.No Load or Open Circuit test

2. Load Test when BESS acting as an independent a.c source

3.Load Test when BESS acting in parallel with the electric grid

4. Transient Test when BESS acting in load leveling mode

4.1 No Load or Open circuit Test

In this test the BESS is run without any load connected to its output terminals. The purpose of this test is to obtain the open circuit characteristic which is the relation between the modulation index M_A and the rms terminal voltage measured as line-to-line voltage$V_{L\text{-}L}$. The measured and calculated values are tabulated in Table 4.1 and the open circuit characteristic is plotted in figure 4.1.

The basis for the formula used to calculate the line to line voltage is as follows: Under ideal conditions the fundamental rms phase voltage is given by

$V_{phase} = M_A\ V_{dc}\ /2^*\ \sqrt{2}$ but in practice this formula gives much higher calculated values as the blanking time between the two switches in the same leg of the inverter is not considered. Also there is a finite voltage drop V_{CESAT} across the IGBT switches which in turn reduces the available output voltage. Taking these factors into account the formula for the line to line voltage of the inverter becomes:

$$V_{L-Lcalc} = \frac{\sqrt{3}(V_{dc} - 2V_{CE})}{2\sqrt{2}} \times M_a B_L a$$

$V_{dc} = DC\ \ Link\ \ Voltage$

$V_{CE} = V_{sat}\ \ across\ \ IGBT$

$M_a = Modulation\ \ Index$

$B_L = Blankingtime\ \ Ratio$

$a = Transformer\ \ Ratio$

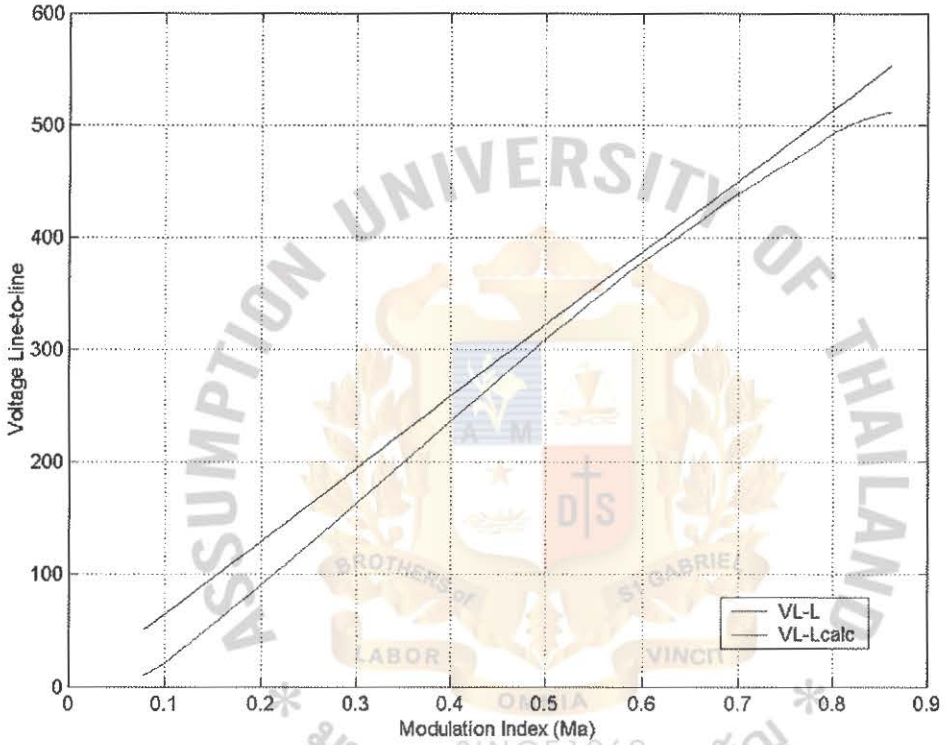

Figure 4.1 Open Circuit Characteristic with measured and calculated values

The modulation index can be set to 13 bit resolution in the DSP controller. Hence the calculated modulation index M_A = XXXX H / 1FFF H = XXXX D /8192 D and referring to the data sheet of the IGBT the saturation voltage V_{CESAT} = 3V Also the gate drive module provides a blanking time of 5usec at the rising and falling edges of the gate pulses. Refer to figure 4.2 for the details of the blanking time provided. Hence the blanking time ratio B_L =0.9 taking the switching frequency f_s =10kHz (100 usec period). The step up transformer turns ratio is 7.33 (refer to chap.3.2.4). The line

to line voltage is calculated using these parameters. With this formula the calculated and the measured line to line voltages are very close to each other as shown in the fig.4.1

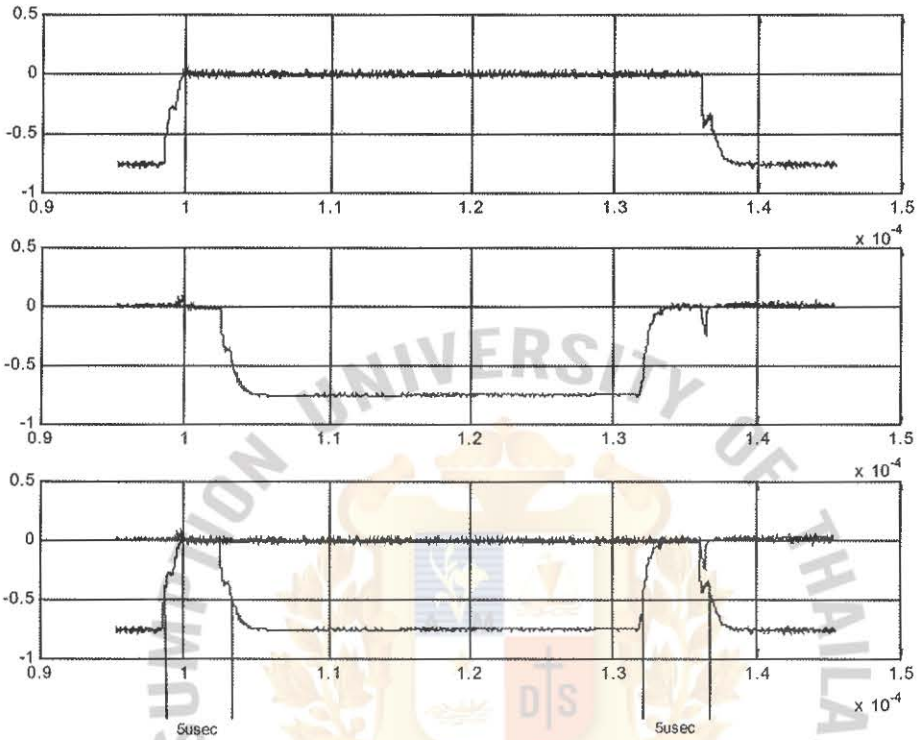

Figure4.2 Blanking Time (Dead time) about 5 usec for each rise edge and falling edge.

Table 4.1 No load test

DIGIT	VL-L	Vdc	ma	VL-Lcalc	Diff
650	10.25	166.45	0.0793	51.45	41.20
1160	50.20	166.44	0.1416	91.82	41.62
1620	89.60	166.38	0.1978	128.18	38.58
2100	131.30	166.29	0.2563	166.07	34.77
2560	172.00	166.18	0.3125	202.31	30.31
2990	210.50	166.03	0.3650	236.07	25.57
3410	248.10	165.90	0.4163	269.01	20.91
3800	282.80	165.76	0.4639	299.52	16.72
4230	320.80	165.62	0.5164	333.12	12.32
4610	352.70	165.50	0.5627	362.77	10.07
5010	384.00	165.35	0.6116	393.88	9.88
5400	413.90	165.21	0.6592	424.16	10.26
5800	443.50	165.07	0.7080	455.18	11.68
6210	469.80	164.92	0.7581	486.90	17.10
6600	495.50	164.76	0.8057	516.96	21.46
6700	500.30	164.73	0.8179	524.69	24.39
7020	511.00	164.64	0.8569	549.44	38.44

Table 4.2 and fig. 4.3 show the phase shift between utility gird voltage and inverter voltage by changing parameter input to controller.

Table4.2 Relationship between digit number in DSP with angle δ

Digit	Time	delta angle	E
-3650	2.64 E-03	47.52	lead
-3500	2.36 E-03	42.48	lead
-3000	1.76 E-03	31.68	lead
-2500	1.04 E-03	18.72	lead
-2000	4.00 E-04	7.20	lead
-1500	2.00 E-04	3.60	lead
-1000	-2.40 E-04	-4.32	lag
-500	-9.20 E-04	-16.56	lag
0	-1.72 E-03	-30.96	lag
500	-2.12 E-03	-38.16	lag
1000	-2.80 E-03	-50.40	lag
1500	-3.40 E-03	-61.20	lag

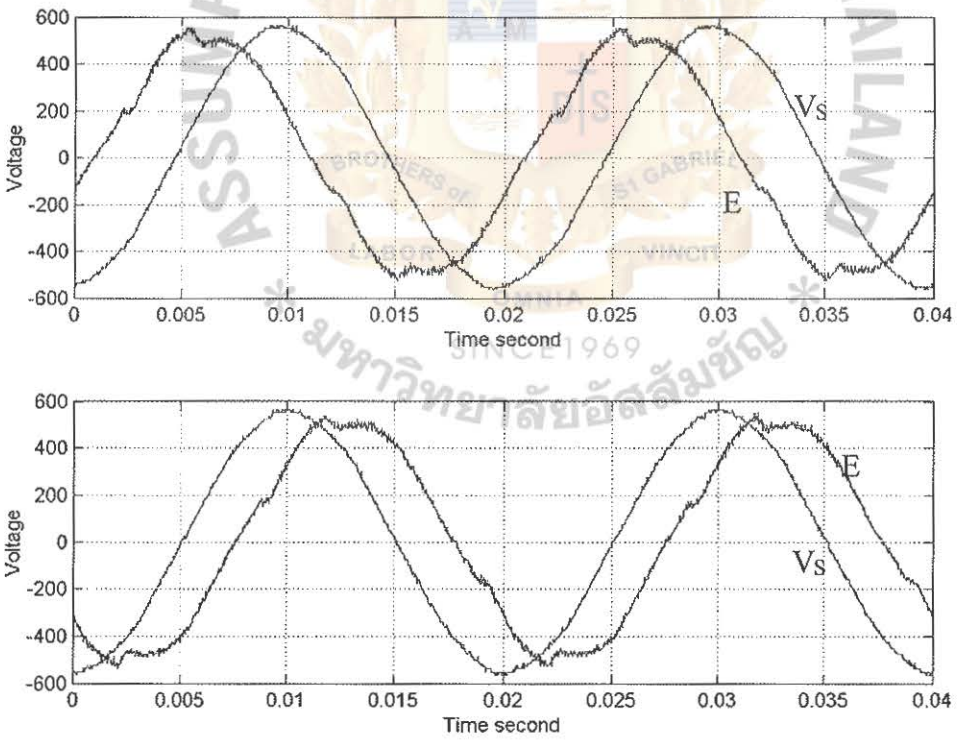

Figure 4.3. Waveform show phase change between E and V_S

The Line to Line voltage waveforms and their harmonic content are shown in the figures 4.4 to 4.8 for different modulation indices. These waveforms are taken after the low pass filter and at the high voltage terminals of the transformer.

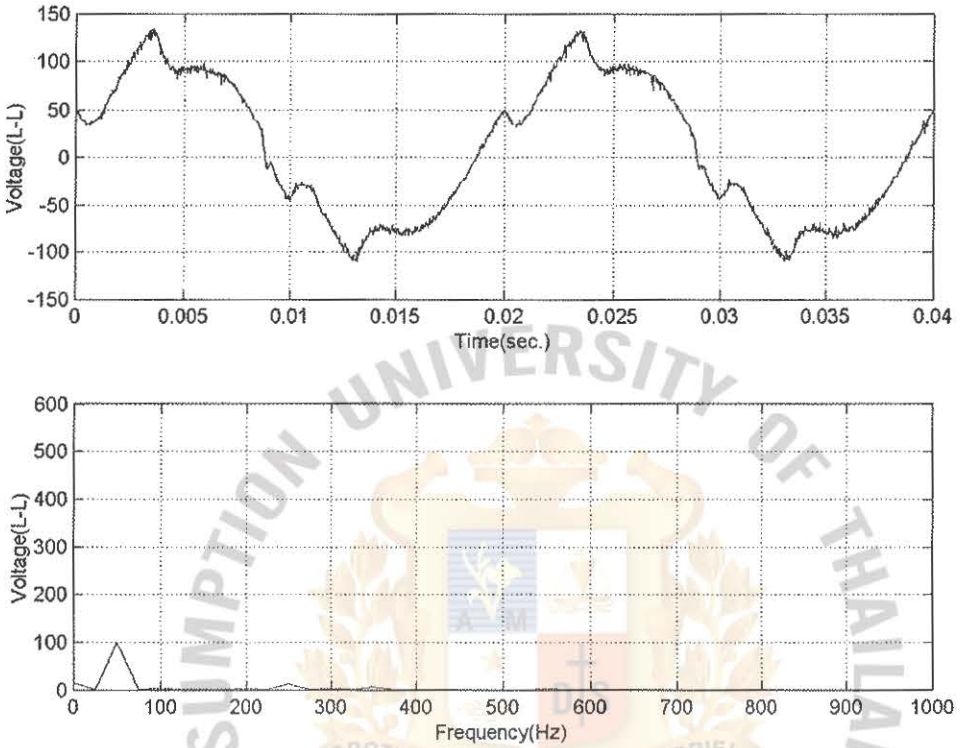

Figure 4.4 Waveform of no load line-line voltage with harmonic analysis

Condition : $M_a = 0.1742$, $V_{dc} = 165.75V$, $V_{rms} = 71.4V$ by Fluke meter

V_{rms} from Oscilloscope trace is 70.51V fundamental (50Hz) after harmonic analysis and THD is found to be 17.3780%. Small traces of 5^{th} and 7^{th} harmonic exist.

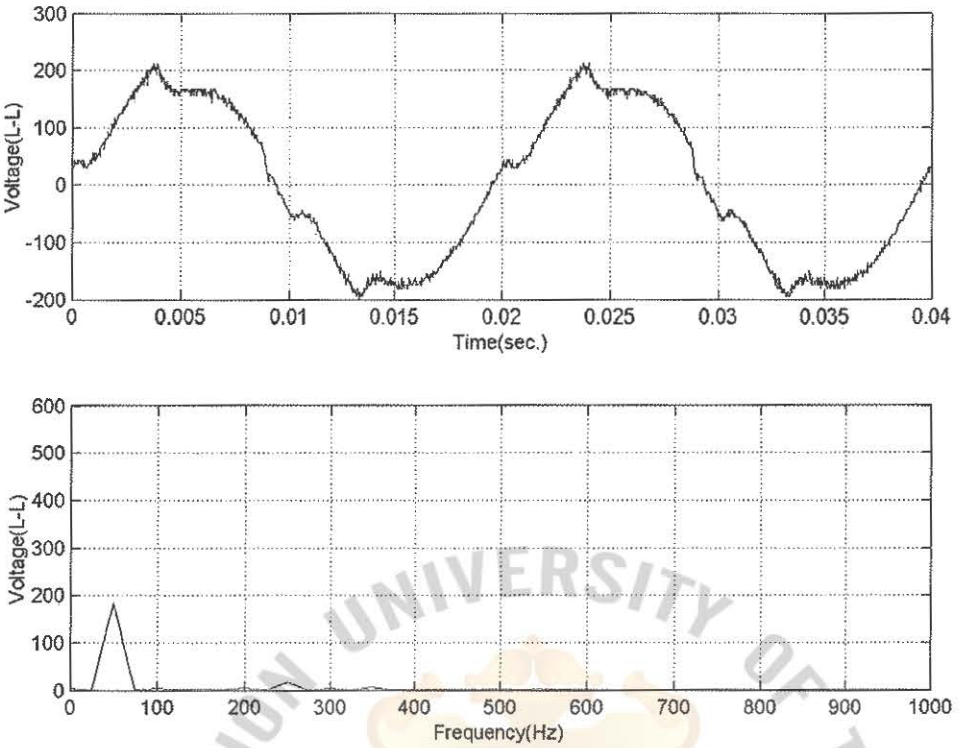

Figure 4.5 Waveform of no load line-line voltage with harmonic analysis

Condition : $M_a = 0.2593$, $V_{dc} = 165.75V$, $V_{rms} = 130.9V$ by Fluke meter

Calculate V_{rms} form Oscilloscope = 130.2194V fundamental (50Hz) of its harmonic analysis, THD = 11.8486%

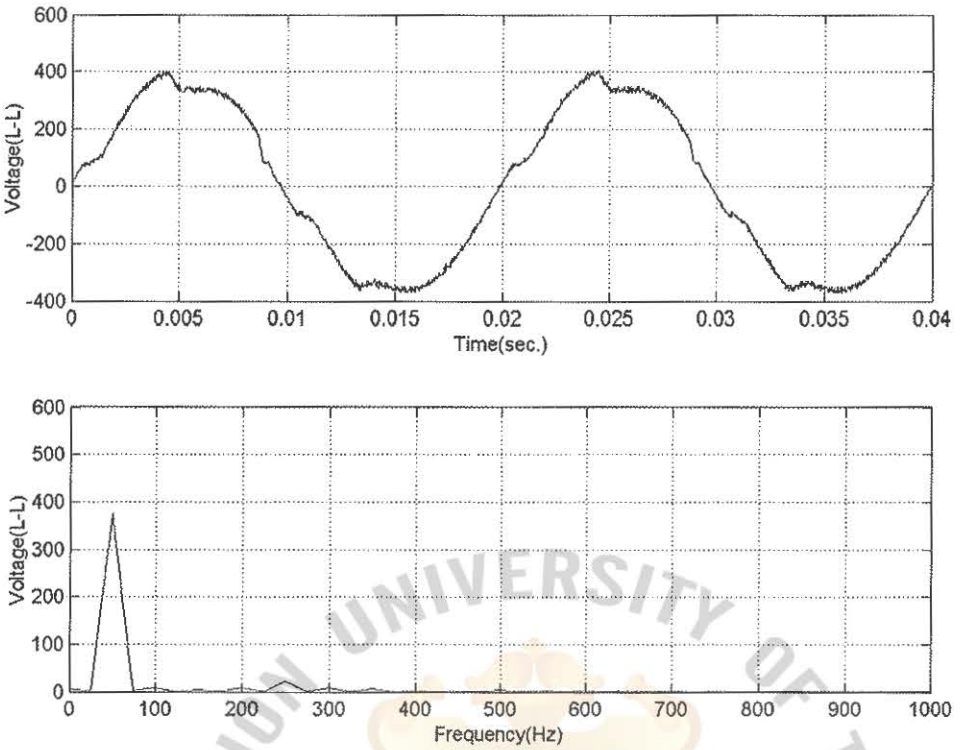

Figure 4.6 Waveform of no load line-line voltage with harmonic analysis

Condition : : $M_a = 0.4447$, $V_{dc} = 165.75V$, $V_{rms} = 265V$ by Fluke meter

Calculated V_{rms} from Waveform = 265.3573V fundamental (50Hz) after harmonic analysis, THD = 8.3495%

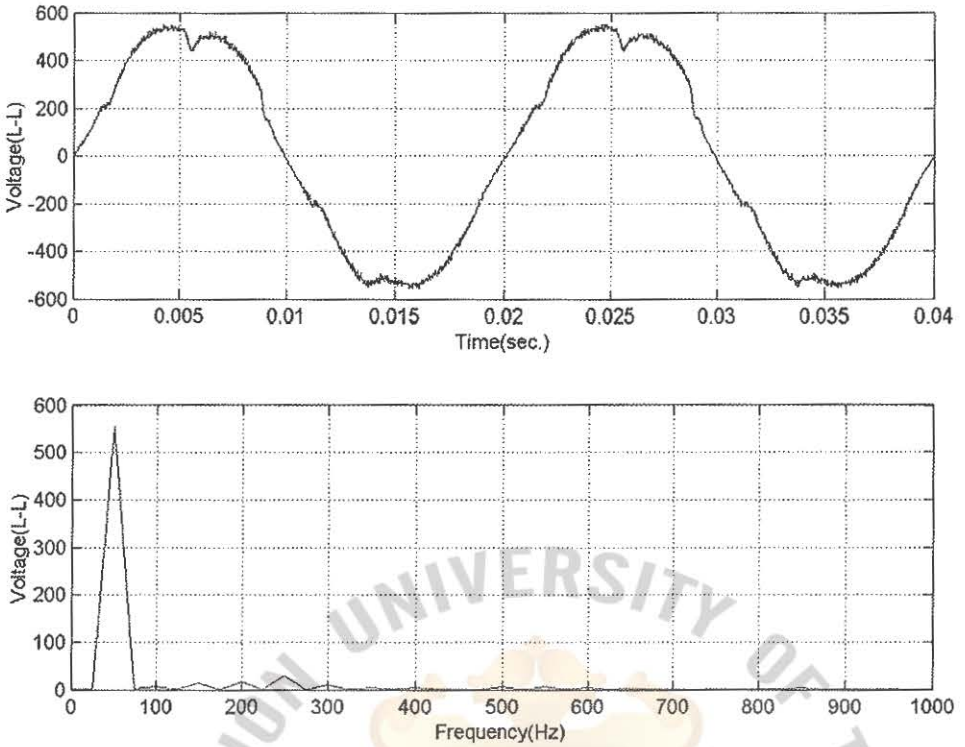

Figure 4.7 Waveform of no load line-line voltage with harmonic analysis

Condition : $M_a = 0.63$, $V_{dc} = 165.75V$, $V_{rms} = 392.1V$ by Fluke meter

Calculated V_{rms} from Oscilloscope = 391.9250V fundamental (50Hz) after harmonic analysis , THD = 7.8541%

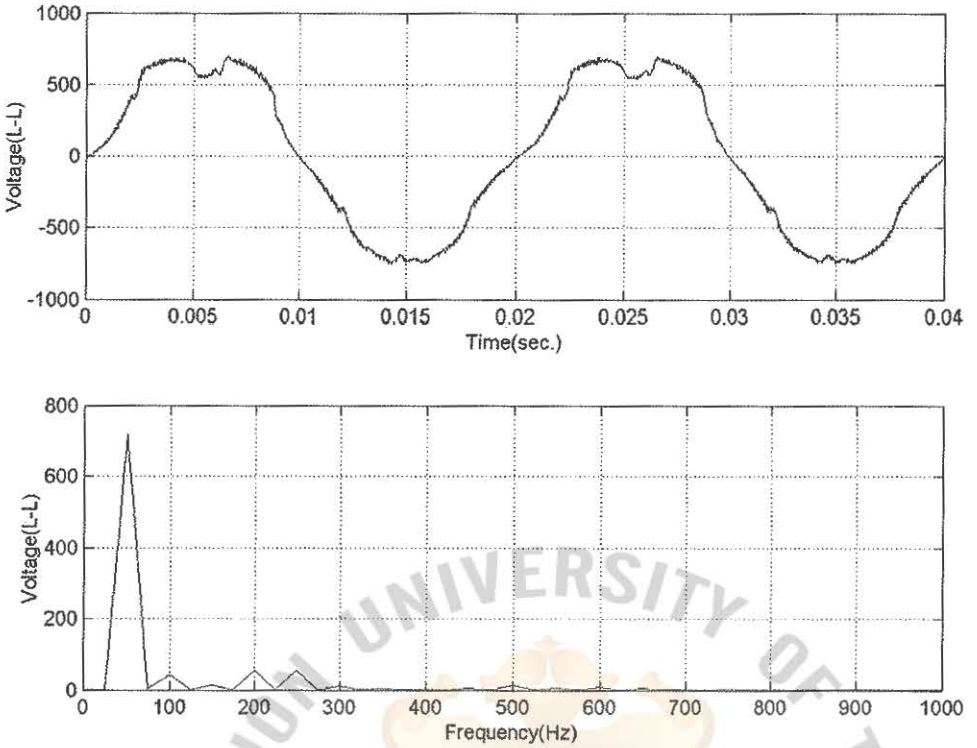

Figure 4.8 Waveform of no load line-line voltage with harmonic analysis

Condition : : $M_a = 0.8671$, $V_{dc} = 165.75V$, $V_{rms} = 510.9V$ by Fluke meter

Calculated V_{rms} from Oscilloscope = 508.2634V fundamental (50Hz) after harmonic analysis, THD = 13.4580%

4.2 Load Test (BESS as a standby generator)

4.2.1 without feedback

In this test the BESS is acting as an independent a.c source feeding its own load having no voltage regulator. The no load voltage is fixed by adjusting the modulation index and this modulation index is kept constant during the test. The results obtained for three modulation indices namely 0.439, 0.565 and 0.739 are shown in the table 4.3 and the load characteristics are plotted in fig.4.9 for resistive load . The load voltage droops with increasing power out put as with any a.c generator without a voltage regulator and in fact the BESS can be regarded as a static synchronous generator..

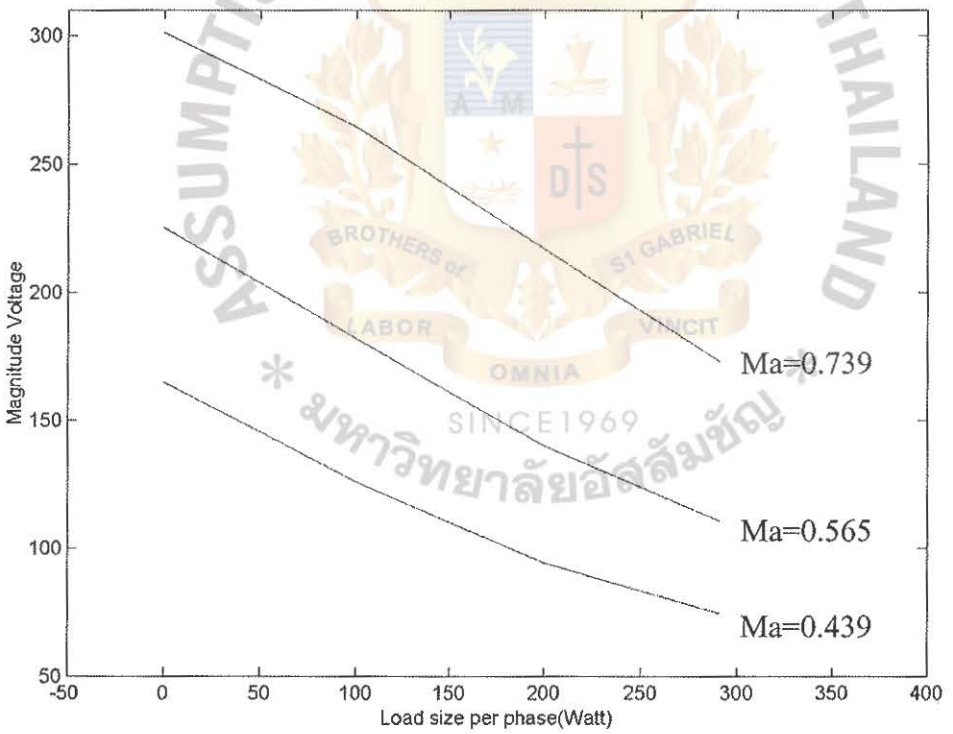

Figure 4.9 Load test at different M_a settings

Using the data in table 4.2 the efficiency of the inverter can be found by the following equation:

$$Eff = \frac{P_{out3ph}}{P_{dc}}$$

$$P_{out3ph} = 3 \times V_{rms} \times I_{rms}$$

$$P_{dc} = V_{dc} \times I_{dc}$$

The overall loss in the inverter system can be found as

$$Loss = P_{dc} - P_{out3ph}$$

From the loss it is possible to estimate the equivalent internal resistance of the system on per phase basis as:

$$r = \frac{P_{dc} - P_{out3ph}}{3 \times I_{rms}^2}$$

This equivalent resistance varies with load conditions as can be seen from the table 4.3 given below.

Table 4.3 Load test data

Ma	Vdc	idc	Vrms/phase	Irms	Pdc	Pout3ph	loss	eff	r
0.438859	166.5	0.298	164.6	0	49.617	0	49.617	0	
	165.8	1.17	125.8	0.347	193.986	130.9578	63.0282	0.675089	58.16121
	165.5	1.717	94.2	0.62	284.1635	175.212	108.9515	0.616589	31.49251
	164.8	1.993	72.6	0.838	328.4464	182.5164	145.93	0.555696	23.08947
0.564847	166.1	0.466	225.1	0	77.4026	0	77.4026	0	
	165.2	1.837	181.8	0.418	303.4724	227.9772	75.4952	0.751229	48.00918
	164.2	2.82	140	0.75	463.044	315	148.044	0.680281	29.24326
	164.1	3.363	107.5	1.023	551.8683	329.9175	221.9508	0.597819	23.56476
0.739007	165.6	0.771	300.9	0	127.6776	0	127.6776	0	
	165.4	2.912	264.5	0.489	481.6448	388.0215	93.6233	0.805618	43.50345
	163	4.555	216.8	0.893	742.465	580.8072	161.6578	0.782269	22.5243
	162.5	5.597	168.7	1.229	909.5125	621.9969	287.5156	0.683879	21.15023

From table 4.3 the efficiency of the inverter is shown to vary around 0.5 to 0.8.depending on the power output

4.2.2 Load Test with feedback

It can be seen that the terminal voltage of the inverter drops down as the load is increased because of its high equivalent internal impedance. In practice we need the terminal voltage to remain constant at the set value irrespective of the load connected. This is achieved by using negative feedback of the terminal voltage to the DSP controller which corrects the modulation index M_a . The load test results are shown in the fig.4.9 and fig.4.10 in the form of graph with and without feed back. It can be seen that with feedback the terminal voltage remains constant almost at the set value. In fact the terminal voltage changed from 380V to 374.5 V only from no load to full load.In order to acertain the effectiveness of the voltage controller, loads were suddenly and removed and the terminal voltage of the BESS were recorded in the form of oscillographic recordings as shown in figures 4.11-4.16. Whenever load is applied suddenly applied the voltage dips slightly and recovers to the set value within one or two cycles time as can be seen from the transient recordings mentioned above. Similarly when the load is removed, quickly the terminal voltage is recovered. This mode of operation of BESS is the Standby generator mode .

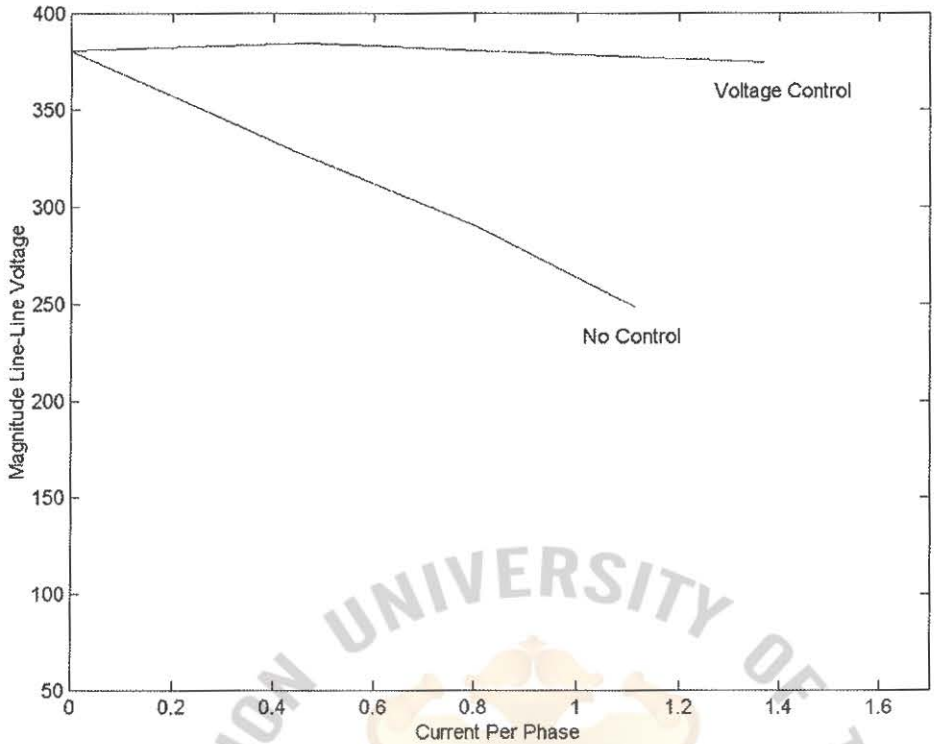

Figure 4.10 Control and no control voltage loop

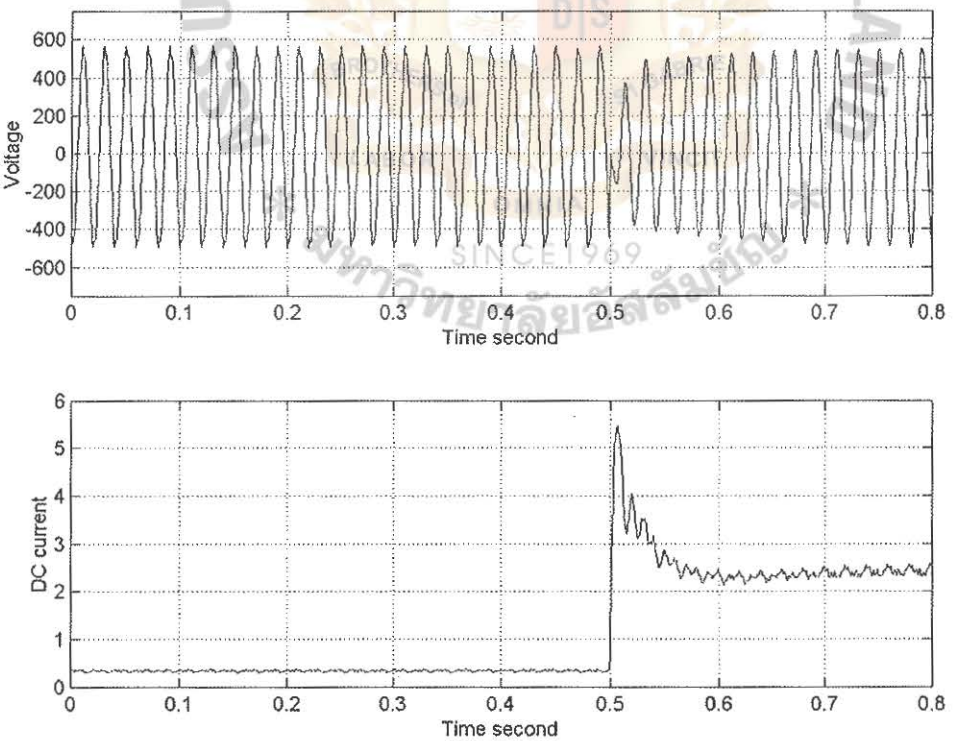

Figure 4.11 Transient response when load 300 watts is closed to the inverter.

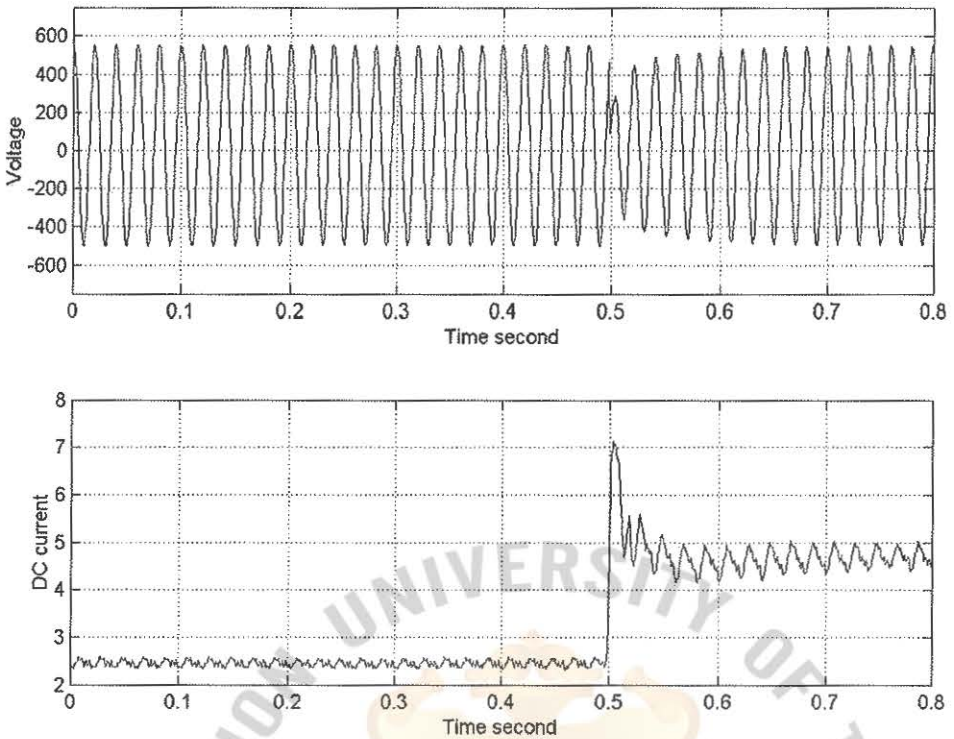

Figure 4.12 Transient response when add more 300 watts to the inverter.

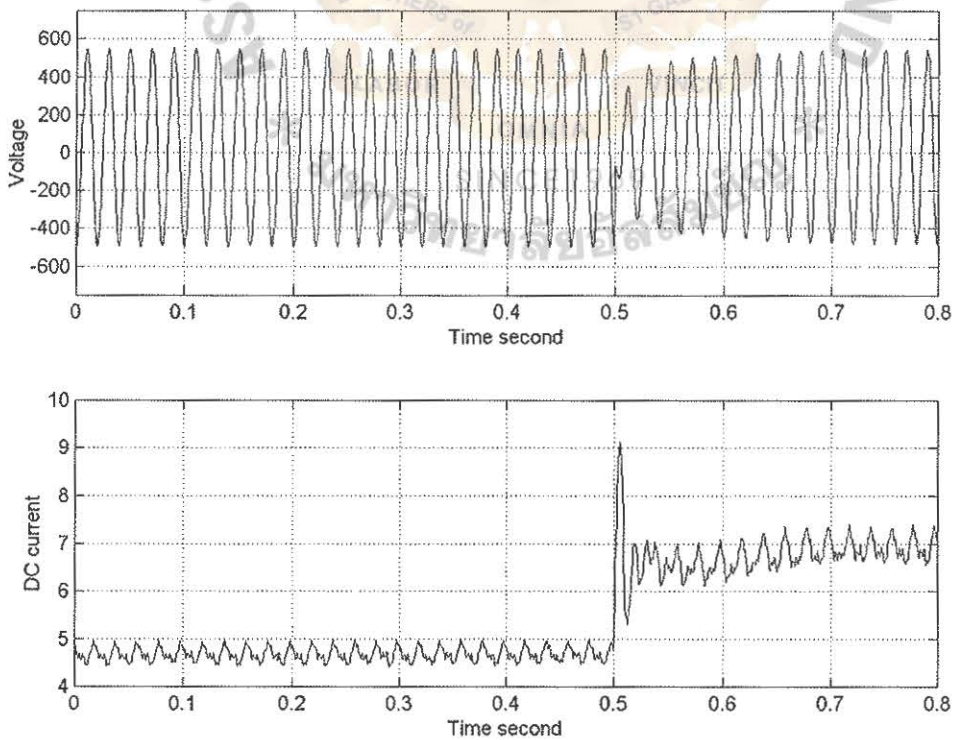

Figure 4.13Transient response when add another 300 watts load to the inverter

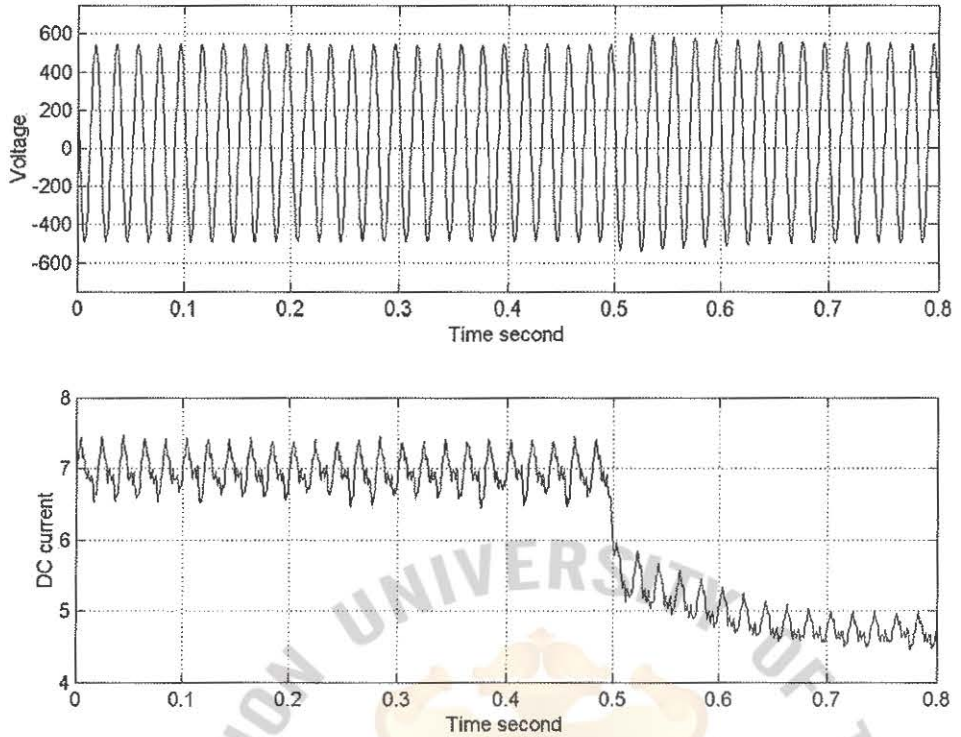

Figure 4.14 Transient response when load 300 watts is remove from inverter

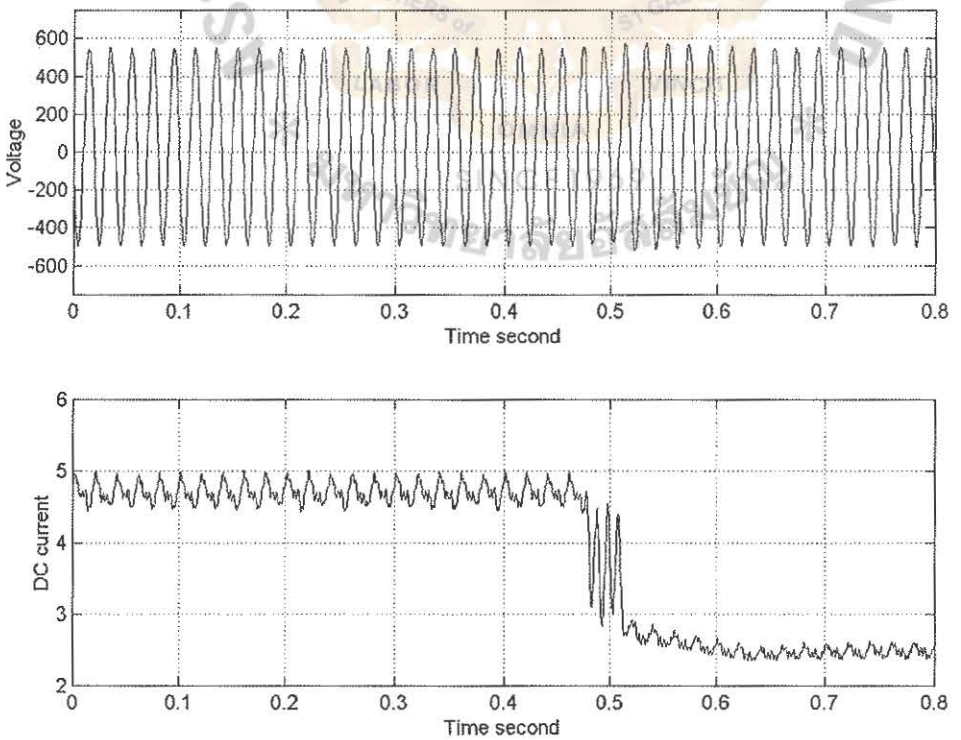

Figure 4.15 Transient response when load 300 watts is remove from inverter

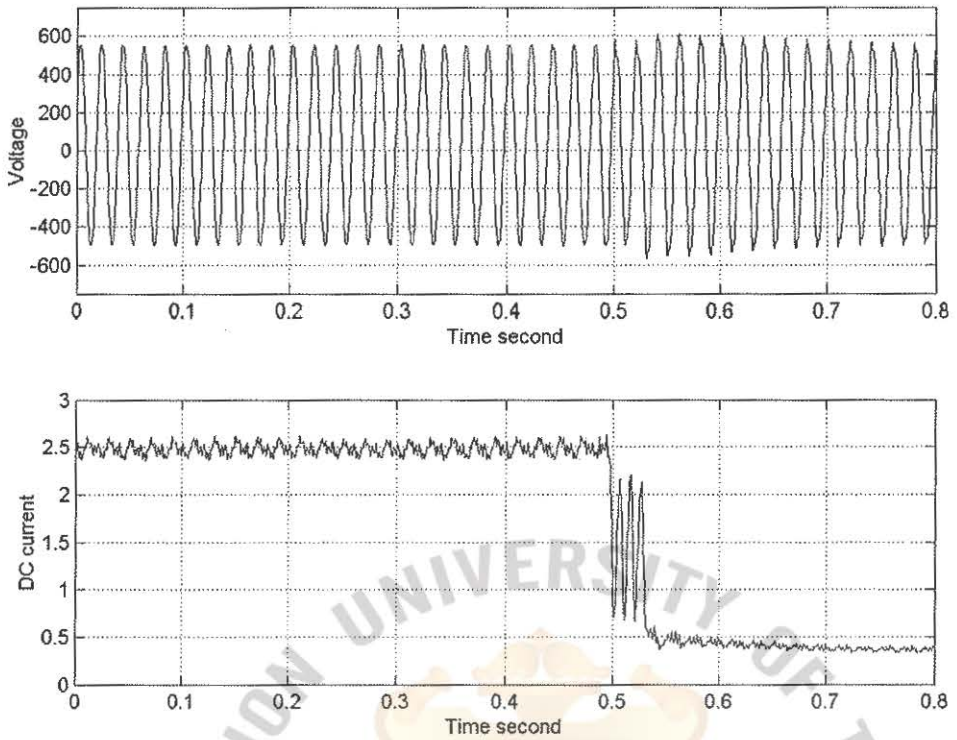

Figure 4.16 Transient response when all load is remove from the inverter

4.3 Parallel Operation of BESS with Electric Grid

4.3.1 Synchronization

The schematic of synchronization strategy is shown in fig 4.17. Modulation index is fixed at the value that get the same voltage level with the grid. After that the zero crossing is detected to find the phase difference and update the frequency of the pwm waveform if the phase change is not close enough the system will not allow to synchronize with the grid. It will adjust until phase change is close enough so the synchronize switch will be close automatically. The difference between this technique with the PLL technique is input information. In case of phase lock loop the phase differenece is continuously fed to the system to adjust in this case at the point of zero crossing will give feed and find an error so it will reduce the computation time of CPU the output will reset and change frequency and wait until find the zero crossing

again and looking for an error after that adjust frequency again. The fig 4.18 show the synchronizing period.

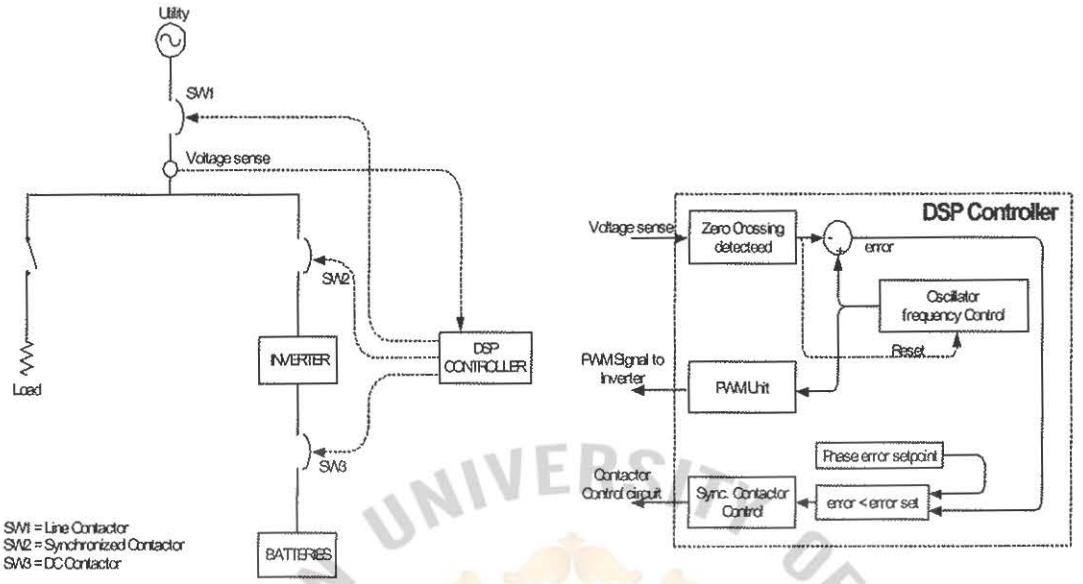

Figure 4.17 Synchronization Strategy

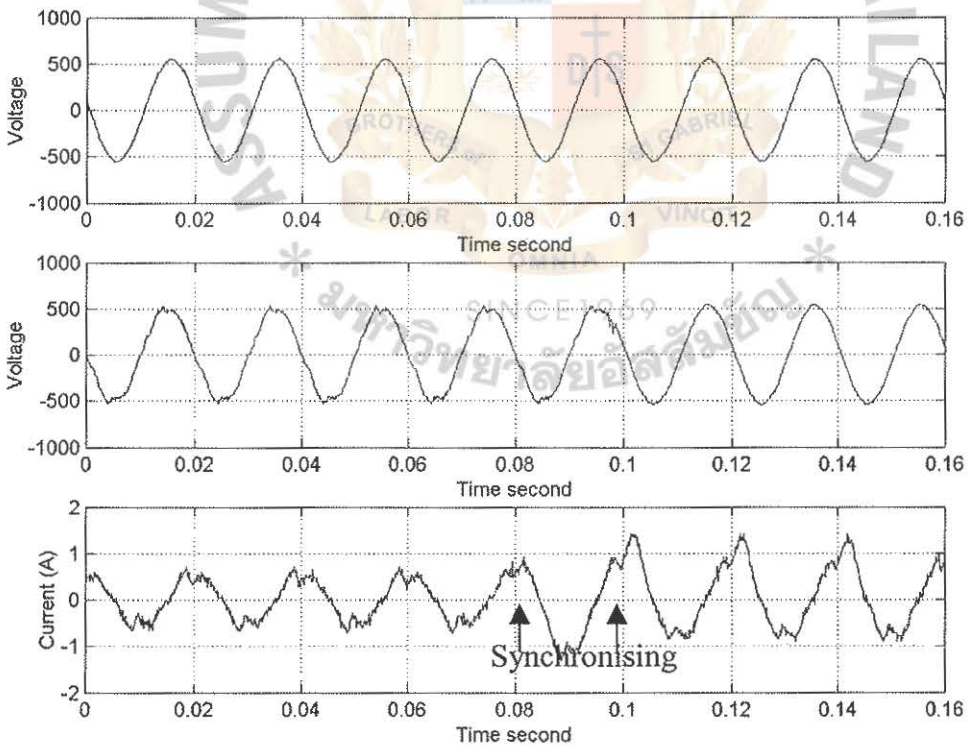

Figure 4.18 The first waveform is voltage line-line of utility, the second waveform is voltage line-line of inverter, the third waveform is current of line 1.

The synchronize period starts when the switch is commanded to closed is happen at 0.08 second. However the voltage wave will be same as the grid voltage nearly 0.1 second because of the settling time of contactor. The 20msec period appears to be the contractor closing time. After the synchronize switch is closed there is an effect to the current waveform because of the phase and the amplitude of the inverter cannot be exactly equal to the utility so there are some amount of current flow. The Steady state voltage, current waveforms after the synchronization is shown in fig. 4.19

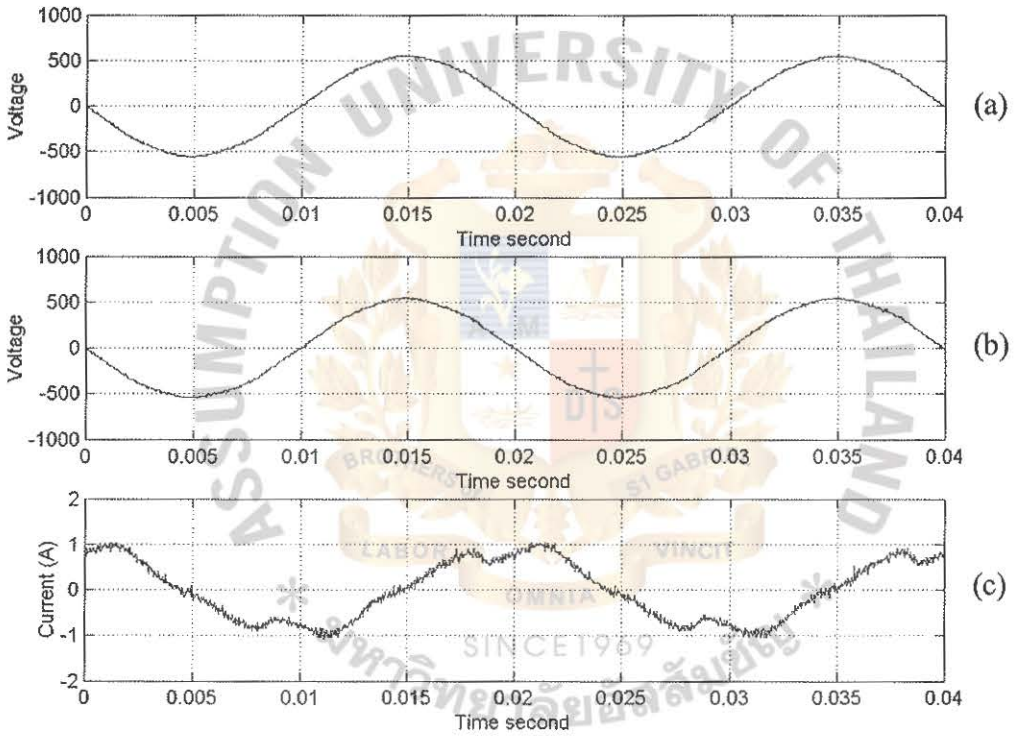

Figure 4.19 Waveform of (a) Voltage of Utility, (b) Voltage of Inverter after synchronization (common point with (a)) and (c) current of line 1 after synchronization at steady state

4.3.2 Charging Mode

In this mode the phase angle δ between E and grid voltage V_S is adjusted such that E lag V_S and power flows from grid to battery. The line voltage, line current are shown in fig 4.20. The power factor is found to be 0.98 or equal to cos10.8. The method of caculating Pf using Matlab as shon in fig 4.21. and voltage THD is 1.5553%, current THD is 7.6427%at V_{rms} is 217.2065V, I_{rms} is 2.2A.

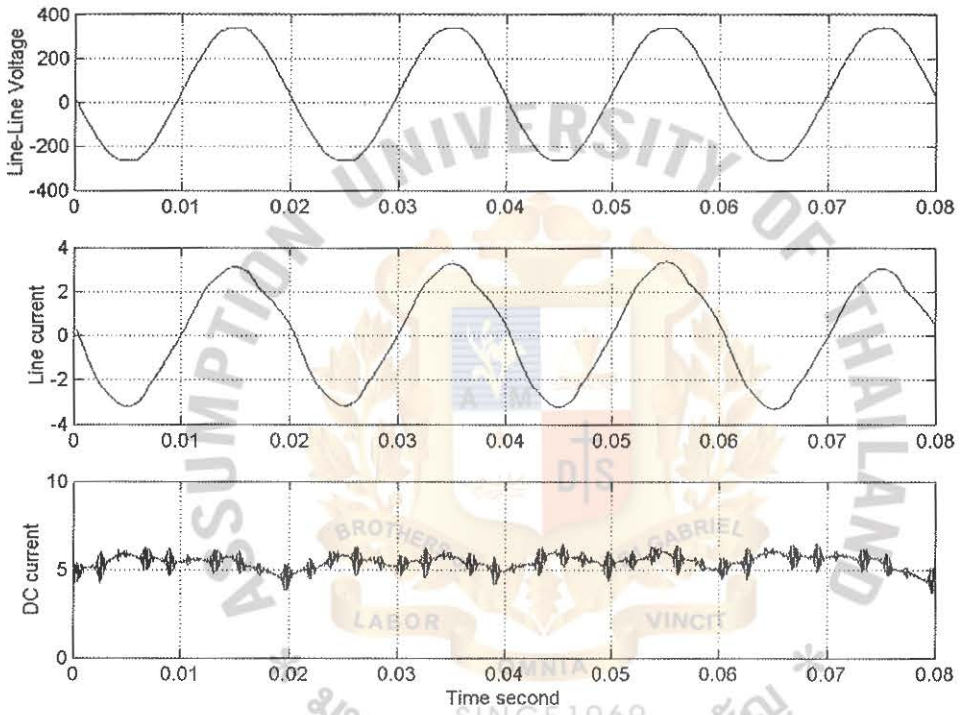

Figure 4.20 Voltage L-N at rated, Voltage THD is 1.5553%, Current THD is 7.6427%, V_{rms} is 217.2065V, I_{rms} is 2.2A, E is 220V, δ is 47.52°

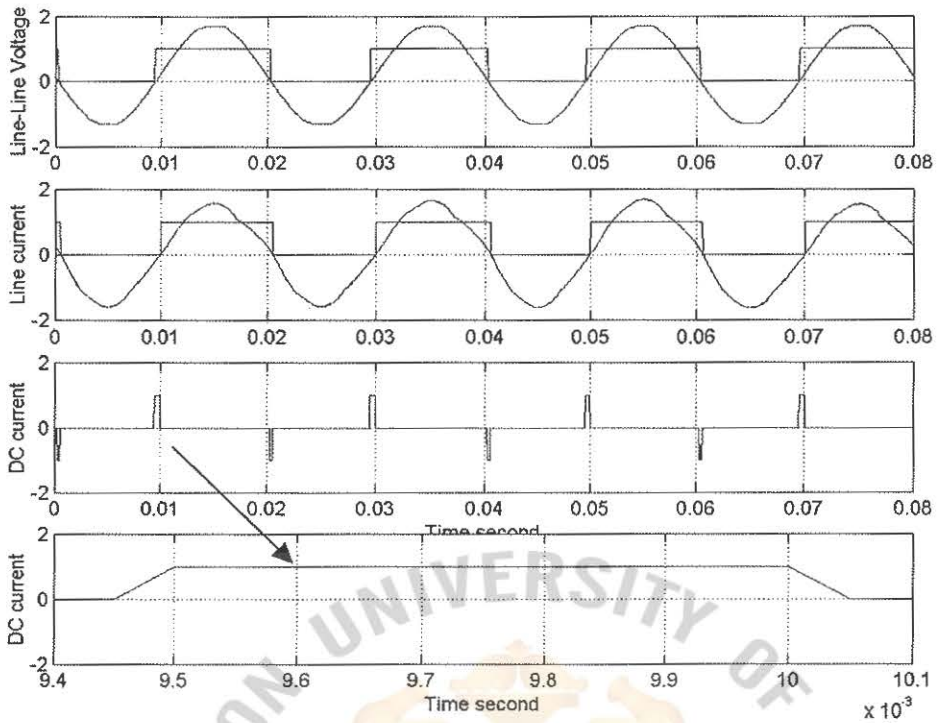

Figure 4.21 Voltage and current phase different to determine Pf (by Matlab)

4.3.3 Discharging Mode

In this mode the phase angle δ between E and grid voltage V_S is adjusted such that E lead V_S and power flows from battery to grid. The line voltage, line current are shown in fig 4.22. The power factor is found to be 0.66or equal to cos48.6°. The method of caculating Pf using Matlab as shon in fig 4.23. and voltage THD is 1.6206%, current THD is 6.3794%, at V_{rms} is V_{rms} is 217.4892V, I_{rms} is 2.5594A

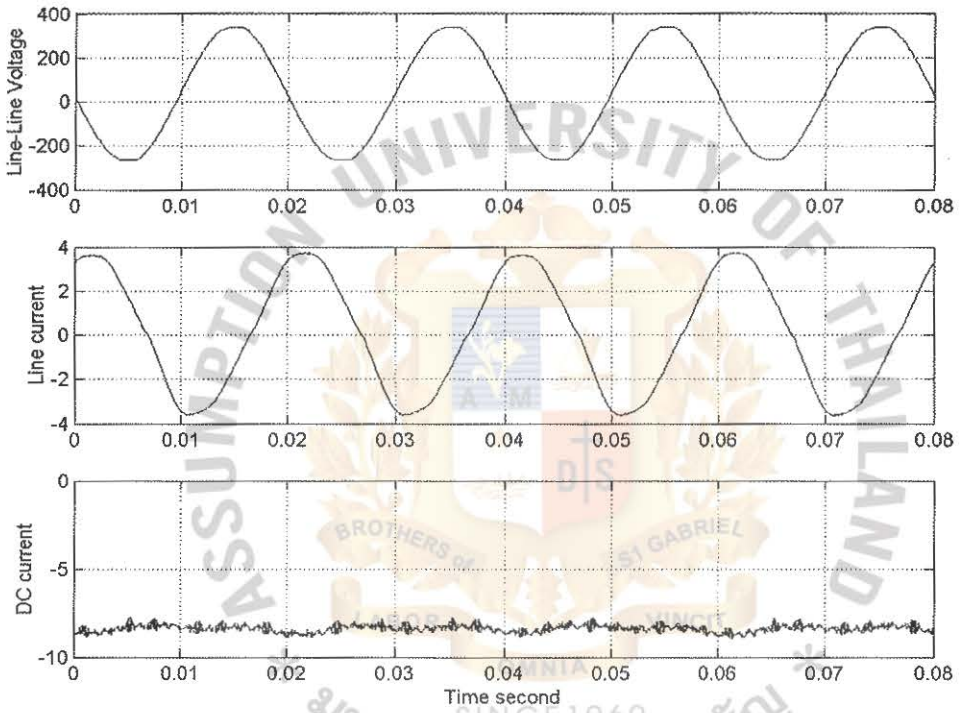

Figure 4.22 Voltage L-N at rated, Voltage THD is 1.6206%, Current THD is 6.3794%, V_{rms} is 217.4892V, I_{rms} is 2.5594A, E is 220V, δ is –61.20°

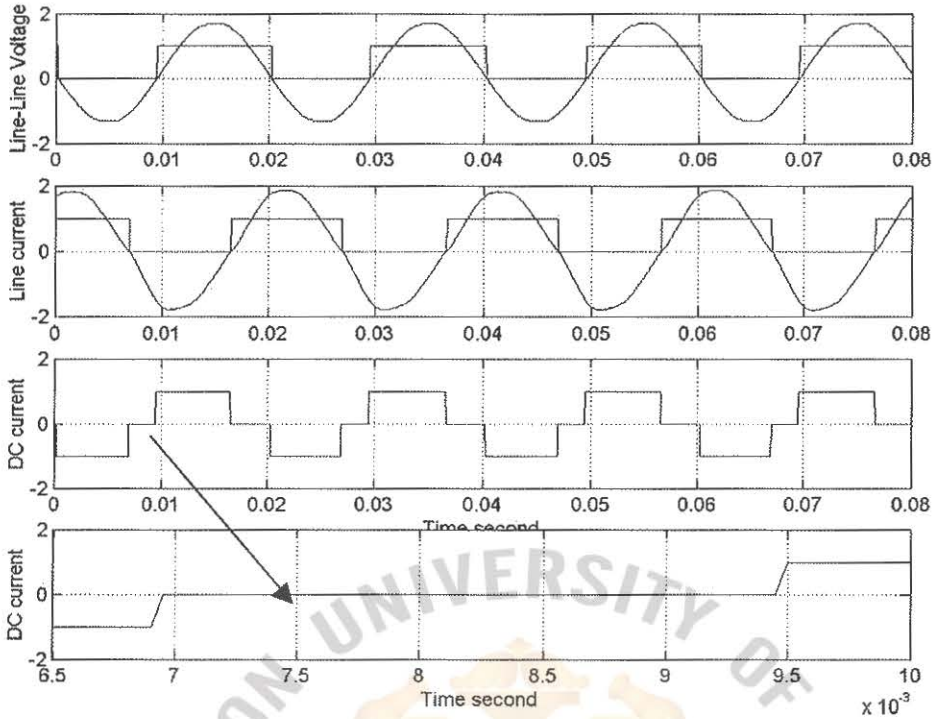

Figure 4.23 Voltage and current phase to determine Pf (by Matlab)

4.4 Demand Control

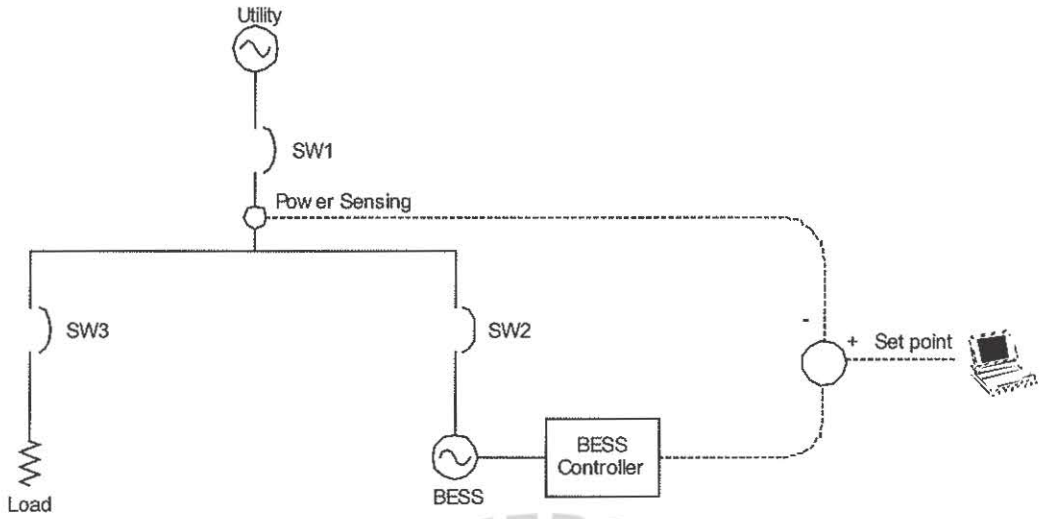

Figure 4.24 Working diagram test condition

At first BESS will be synchronized to the utility by SW1 an SW2 after that the control start working (see fig 4.24) the power set point is set by computer passing through serial communication (RS 232) to controller. The power set point is set equal to zero as shown in fig.4.25. Hence BESS try to keep input power from utility to be zero. After that SW3 is closed so power flow from the grid immediately however the set point still at zero so BESS try to keep input power to be zero again by discharge power from battery bank to grid. Power graph will going down to zero again. After sometime SW3 is removed from the system so power from BESS will flow to utility instead so power graph will going down and because of set point is still zero so the BESS try to keep input power from utility to be zero again. Matlab simulation results are given in fig 4.25-4.27 and the actual test results are given in fig 4.28,4.29. While set point is reached in both cases after load change. The settling time is faster in the simulation than in the actual test. This is to be researched.

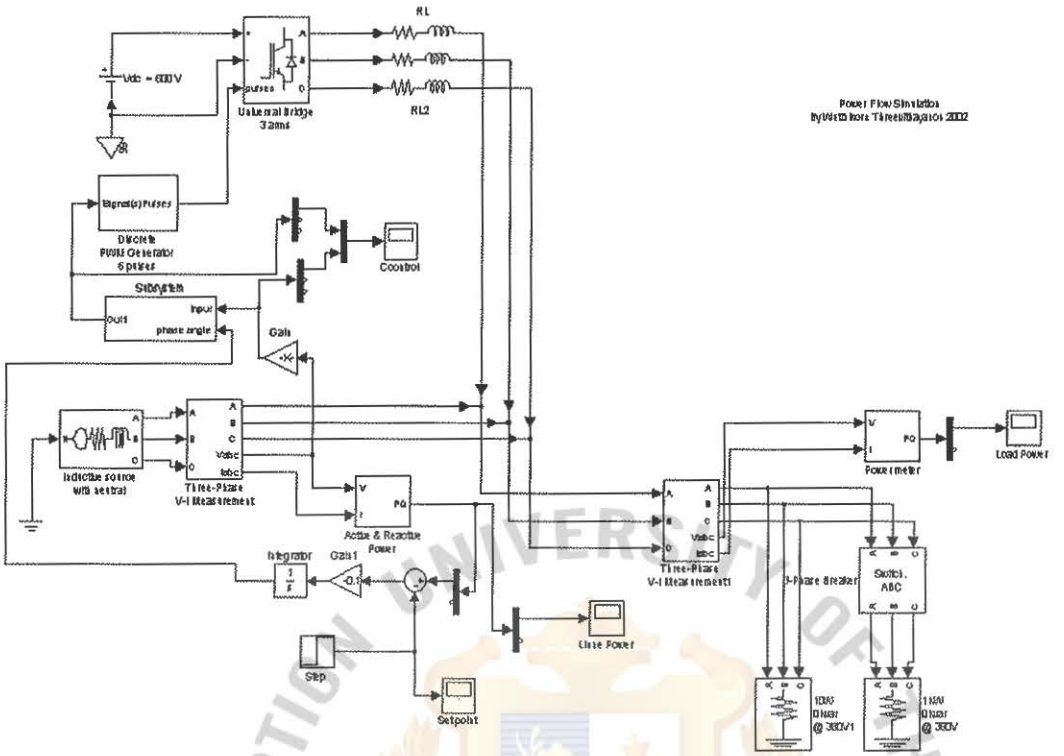

Figure 4.25 Matlab Simulation for power flow schematic

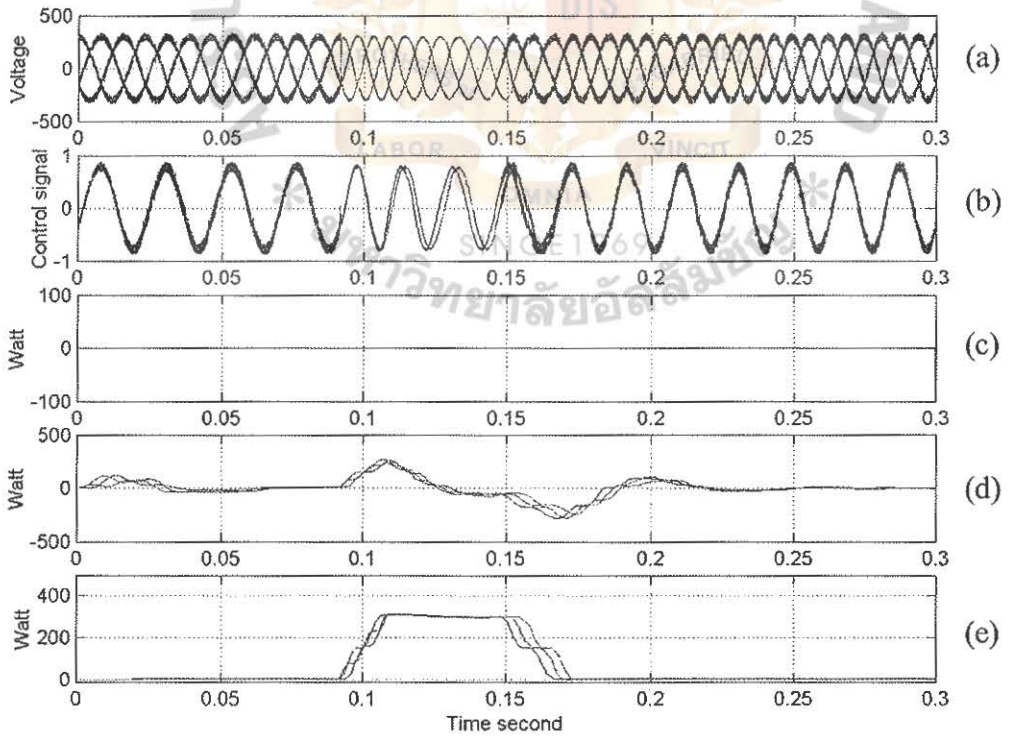

Figure 4.26 Matlab Simulation result, (a) voltage 3 phase, (b) control signal, (c) Power Set-point, (d) Utility grid Power, (e) Load Power

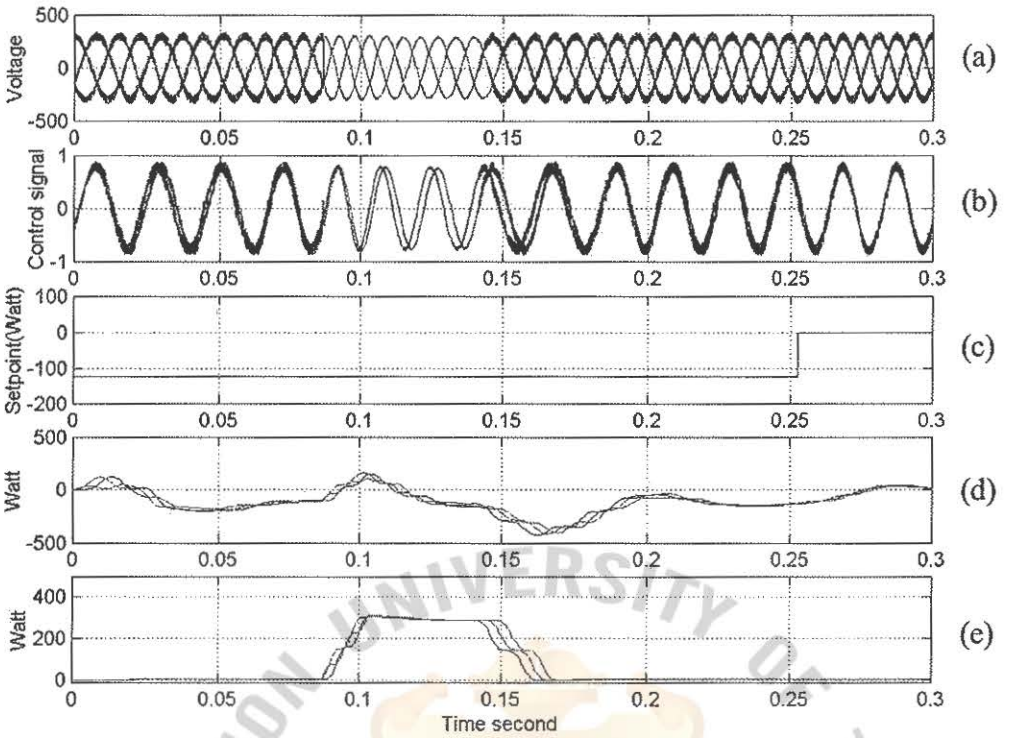

Figure 4.27 Matlab Simulation result set-point change,(a) voltage 3 phase, (b) control signal, (c) Power Set-point, (d) Utility grid Power, (e) Load Power

Data plot in fig.4.27 and fig.4.28 come from the controller unit which will return value of power to the computer. Power ratio in fig.4.27, fig.4.28 is 1W:2000 digits.

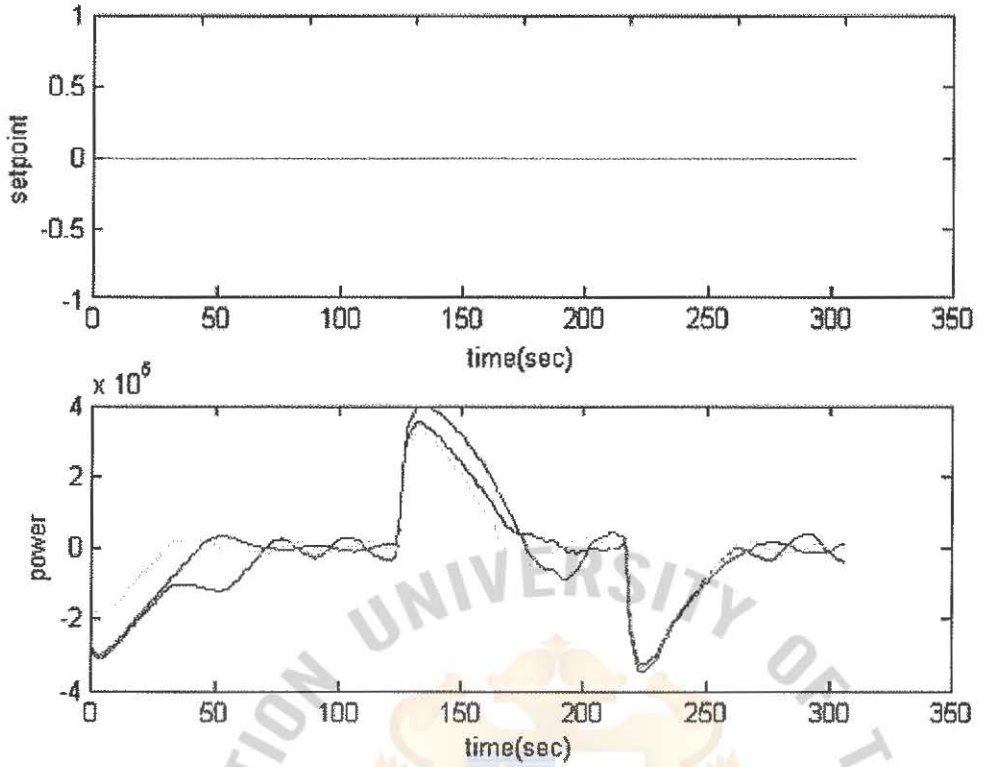

Figure 4.28 Set point is fixed at zero then turn on load after sometime turn off load.

Y axis ratio is 1W:2000

In fig.4.28 set point has been change and –125 watt that mean after synchronize the BESS will send power flow to utility equal 125 watt after that when load is connected to grid BESS try to keep power flow to the utility equal to set point hence the graph power in fig.4.28 will going down to set point again after that the set point has been change to be zero. Then BESS try to trace on the setpoint.

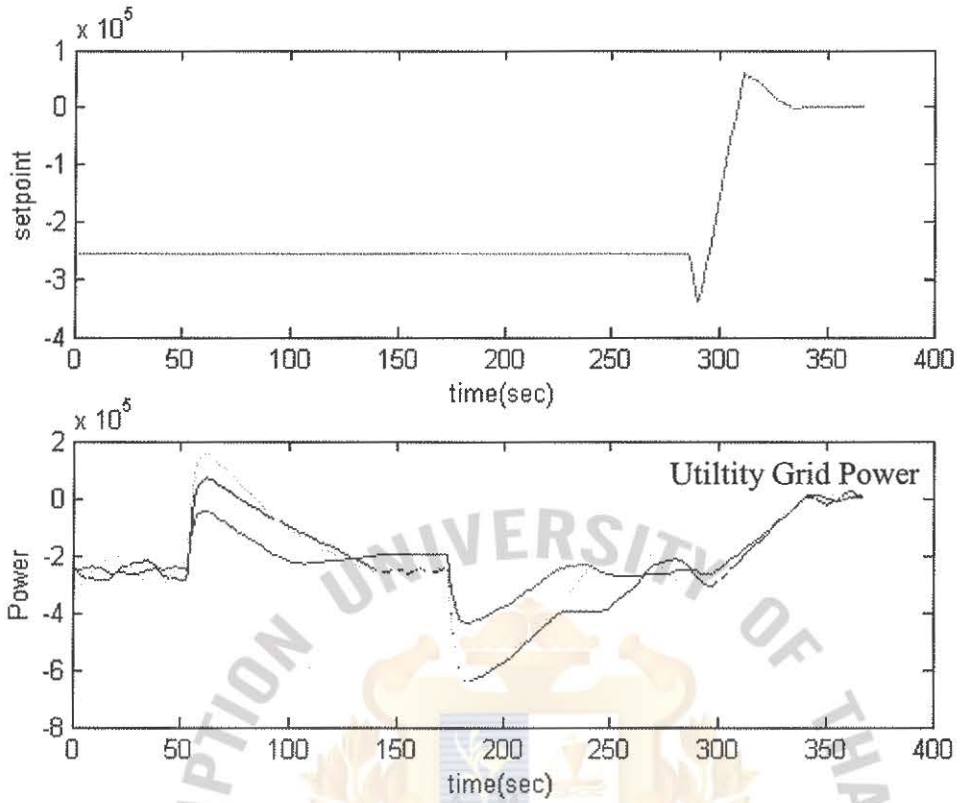

Figure 4.29 Set point is fixed at –125 watt (discharging power from battery string to line) then change set point back to zero.

Chapter 5.

Conclusion

5.1 Summary

A Battery Energy Storage System (BESS) rated for 1.2 kW power level is designed, constructed and tested in the laboratory. In this process steady state performance equations are derived by modeling the BESS as a static synchronous machine. The BESS constructed incorporates modern pwm technology involving IGBT power modules, sensors of line voltages and currents with isolation, gate drivers and above all two numbers of Texas Instruments DSP TMS 320F241 is applied in the overall control of the BESS. The required familiarization with this DSP and its successful application to the control is done by developing the necessary software. The hardware and software developed are tested for their effectiveness by conducting various tests on the BESS. The BESS is tested as an independent generator feeding its own isolated load with frequency and voltage control. Also the BESS is synchronization with the grid, the BESS is tested in discharging and charging modes thus allowing the power and reactive power to flow in either direction between battery bank and the electric supply system under steady state. This is done by adjusting the magnitude and phase angle δ of the inter emf. by software control. These tests confirm the effectiveness of the hardware components and the software developed for the DSPs. to a certain the transient behaviour, the BESS is tested in demand control or power leveling mode. In this mode the response time is found to be large and is due to the computation time

required by the controller. Test results are given in the thesis for all the modes of testing described above.

5.2 Recommendations for further research work

Further research work is to be carried out in the following aspects of BESS operation. (a) As mentioned in 5.1 software is to be developed for power leveling mode to reduce computation time in order to increase the speed of response under changing load conditions. (b) A 50 Hz step up transformer is used in the present work to bring the BESS voltage to the electric supply level. It is better to dispense this transformer as it adds considerable weight to the system. This possible by increasing the d.c voltage level applied to the converter. One suggestion is to use boost converter between battery bank and IGBT converter.This is to be researched into. (c) The BESS is tested in a linear load environment wherein the load currents involved are sinusoidal. When nonlinear loads are connected, they generate harmonic components of current in the supply line. The BESS can be applied as an active harmonic filter to make supply current sinusoidal and at unity power factor. (d) By the present algorithm of control, there are two parameters feedback (Active power, Reactive power) which effect each other so better to study the change characteristic of those parameters to improve the control algorithm. (e) Develop new control method, because the output require is active and reactive power which effect each other so the current control method may give a better performance. However from experience in current control feedback signals are needed filter to remove the switching noise which will effect the control signal. Filter circuit or software filter will effect to the delay time of control signal result in the output change. Hence the delay time and the degree of filter have to compromise.

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Appendix A

C Code for DSP controller

A.1 Converter Control

```
#define PWMA_PERIOD 1024
#include <sys/f24x.h>
#include <sys/wd.h>
#include <sys/pwmA.h>
#include <sys/pwm0.h>
#include <sys/serial.h>
#include <compute/space_v.h>
#include <compute/fun_gen.h>
#include <compute/stat.h>
#include <sys/adc.h>
#include <sys/can.h>
#define MAG_LIMIT 8192
FUN_GEN vd=FUN_GEN_DEFAULTS;
                        /*STAT_AVG_S16 avg = STAT_AVG_S16_DEFAULTS;*/
                        /*STAT_AVG_S16 dc  = STAT_AVG_S16_DEFAULTS;*/
s16 phshf0,phshf1,phshf2;
s16 vin,vout,vinv,pwr0,pwr1,pwr2,magnitude;
s32 vin_old;
u16 control,count1;
void pwmA_PD_interrupt() {
 EVIFRA = 0x0001;   // Reset Interrupt
 }
void pwm0_interrupt() {
 EVIFRB = 0x000F;                    // Reset Interrupt
```

```
}
void pwmA_interrupt() {
 s16 sint,shift;
 asm(" SETC XF");
 adc_get2_start(0,3);
 adc_get2_stop(&vin,&vinv);
 vin<<=4;
 vin-=SC;    /*vin=vin-sc*/
 vin_old = vin_old - (vin_old>>3) + vin;
 vin = vin_old>>3;
/* Generate Signal For Swithing Device */
 /* Filter Signal */
 fun_gen_pll(&vd,vin);
 vd.update(&vd);
 if (phshf0>1500)  phshf0= 1500;
 if (phshf0<-3650) phshf0=-3650;
 if (phshf1>1500)  phshf1= 1500;
 if (phshf1<-3650) phshf1=-3650;
 if (phshf2>1500)  phshf2= 1500;
 if (phshf2<-3650) phshf2=-3650;
 vout = (vd.phase+phshf0);
 if (vout>8192) vout=vout-2*8192;
 if (vout<-8192) vout=vout+2*8192;
 sint = my_sin(vout);
 vout = mul_s16(vd.mag,sint);
 pwmA_put3((vout>>4)+512);
 vout = (vd.phase+2*8192/3)+phshf1;
 /* 8192 = pi */
```

```
  if (vout>8192) vout=vout-16384; /*16384=2*pi (8192x2)*/
  if (vout<-8192) vout=vout+16384;
  sint = my_sin(vout)-1;
  vout = mul_s16(vd.mag,sint);
  pwmA_put1((vout>>4)+512);
  vout = (vd.phase-2*8192/3)+phshf2;
  if (vout>8192) vout=vout-16384;
  if (vout<-8192) vout=vout+16384;
  sint = my_sin(vout)-1;
  vout = mul_s16(vd.mag,sint);
  pwmA_put2((vout>>4)+512);
/* Get value from Can*/
  pwr0 = can_get(0,0);
  pwr1 = can_get(0,1);
  pwr2 = can_get(0,2);
  if (control==1) {
   if (count1==2){
    count1=0;
   if ((magnitude-vinv)<0) vd.mag -=1;
   if ((magnitude-vinv)>0) vd.mag +=1;
   }
    else count1+=1;
  }
  asm(" CLRC XF");
  EVIFRA= 0x0780;  /* Reset Interrupt */
  }
void main_init(void) {
  u32 i;
```

```
 asm(" BCND 01F00h, BIO"); /* For boot Loader*/
 f24x_init();
 wd_init();

 ser_init(42); ser_puts("System Start-Up\r\n");
 ser_puts("Welcome to Automation Research Team\r\n");
 /* Setup Analog to Digital Converter */
/*adc0.a4_ch_sel = 0x0437; /* Channel 0 for setpoint, Channel 1 for VDC Channel 2 for
current,  Channel 3 for voltage */
/*adc0.c1_gain = adc0.c2_gain = adc0.c3_gain = adc0.c4_gain = 0x1000; adc0.init(&adc0);*/
 adc_init();
 pwmA_init();
 pwmA_init_interrupt();
 pwmA_on();
 OCRA = OCRA & (~(1<<3) | ~(1<<4) | ~(1<<5));
 PADATDIR = PADATDIR | ((1<<11) | (1<<12) | (1<<13));
 can_init(500);              /* Initial Can*/
 can_set_id(0,'a');
 can_put8(0,0,0,0,0);      /* Set input can 0 is mail box a
                              0,1 is receive
                              2,3 is auto
                              4,5 is transmit*/

 magnitude = 650;
 vd.mag =3000;
 control =0;
 asm(" CLRC XF");
 }
```

```
void sync(void) {
 u16 cc;
 vd.status = vd.status | (3<<6);
 while((vd.status & (3<<6)) > 1 ) {
   vd.status = (vd.status & (~(3<<4))) | (3<<4);
   ser_puts(" status="); ser_puth_u16(vd.status);
   ser_puts("\r\n");
   wd_kick();
   }
 ser_puts(" Phase 1="); ser_puth_u16(vd.status);
 ser_puts("\r\n");
 vd.status = vd.status | (3<<6);
 while((vd.status & (3<<6)) > 1 ) {
   vd.status = (vd.status & (~(3<<4))) | (2<<4);
   ser_puts(" status="); ser_puth_u16(vd.status);
   ser_puts("\r\n");
   wd_kick();
   }
 ser_puts(" Phase 2="); ser_puth_u16(vd.status);
 ser_puts("\r\n");
 vd.status = vd.status | (3<<6);
 while((vd.status & (3<<6)) > 0 ) {
   vd.status = (vd.status & (~(3<<4))) | (1<<4);
   ser_puts(" status="); ser_puth_u16(vd.status);
   ser_puts("\r\n");
   wd_kick();
   }
 ser_puts(" Phase 3="); ser_puth_u16(vd.status);
```

```
ser_puts("\r\n");
PADATDIR = PADATDIR |(1<<5); /* AC link contactor*/
}
void demand(void) {
s16 x;
u16 i,j,c;
x =1;
while(x>0) {
 for(i=0;i<1000;++i) wd_kick();
 j++;                                  /* running variable can be detect by puting 1's, e.g. 3,F */
 if ((j&0x00F)==0) {
  ser_puts(" Demand");
  ser_puts(" freq="); ser_putd_s16((vd.freq/(53200/501)));
  ser_puts(" freq="); ser_putd_u16(vd.freq);
  ser_puts(" mag=");  ser_putd_s16(vd.mag);
  ser_puts(" phase="); ser_putd_s16(phshf0);
  ser_puts(" status="); ser_puth_u16(vd.status);
  ser_puts(" power="); ser_putd_s16(pwr0);
  ser_puts("\r\n");
  phshf0 = phshf0 + pwr1;
  phshf1 = phshf1 + pwr2;
  phshf2 = phshf2 + pwr0;
  }
      if ((c=ser_getc(2))!=0)
      { switch(c) {
        case 'o':/*increase phase*/
                x = 0;
          }
```

```
    }
   if ((j&0x0F)==0) {
    }
   wd_kick();
  }
}

void main(void) {
 u16 i,j,k,c,check;
 main_init();
 PADATDIR = PADATDIR & (~(1<<5));
 PADATDIR = PADATDIR & (~(1<<4));
 PADATDIR = PADATDIR & (~(1<<3));
 PADATDIR = PADATDIR | (1<<3); /* DC link contactor*/
 PADATDIR = PADATDIR | (1<<4); /* Inverter link contactor*/
 phshf0 = 0;
 phshf1 = 0;
 phshf2 = 0;
 while(1) {
  for(i=0;i<1000;++i) wd_kick();
  j++;  /* running variable can be detect by puting 1's, e.g. 3,F */
  if ((j&0x00F)==0) {
   //ser_puts(" freq="); ser_putd_s16((vd.freq/(53200/501)));
   //ser_puts(" freq="); ser_putd_u16(vd.freq);
   ser_puts(" mag=");  ser_putd_s16(vd.mag);
   ser_puts(" phase="); ser_putd_s16(phshf0);
   ser_puts(" status="); ser_puth_u16(vd.status);
   ser_puts(" power="); ser_putd_s16(pwr0);
```

```
ser_puts(" Vin=");   ser_putd_s16(vin);
ser_puts(" err=");   ser_putd_s16(magnitude-vinv);
ser_puts("\r\n");
/*magnitude change*/
//if ((magnitude-vinv)<-100) vd.mag -=20;
//if ((magnitude-vinv)>100) vd.mag +=20;
//if (((magnitude-vinv)<-10)&&((magnitude-vinv)>-100)) vd.mag -=10;
//if (((magnitude-vinv)>10)&&((magnitude-vinv)<100)) vd.mag +=10;
//if (((magnitude-vinv)<0)&&((magnitude-vinv)>-10)) vd.mag -=1;
//if (((magnitude-vinv)>0)&&((magnitude-vinv)<10)) vd.mag +=1;
}
    if ((c=ser_getc(2))!=0)
    { switch(c) {
      case 'd':/*increase phase*/
                phshf0 = phshf0 + 10;
                phshf1 = phshf1 + 10;
                phshf2 = phshf2 + 10;
            break;
      case 'a':/*decrease phase*/
                phshf0 = phshf0 - 10;
                phshf1 = phshf1 - 10;
                phshf2 = phshf2 - 10;
            break;
      case 'n':/*no phase shift*/
                phshf0 = 0;
                phshf1 = 0;
                phshf2 = 0;
            break;
```

```
case 'w':/*increase magnitude*/

            vd.mag += 10;

            magnitude +=1;

            if (vd.mag>MAG_LIMIT) vd.mag=MAG_LIMIT;        /* Set the limit */

        break;

case 's':/*decrease magnitude*/

            vd.mag -= 10;

            magnitude -=1;

                        if (vd.mag<0) vd.mag=0;

                /* Set the limit */

break;

case 'c':/*synchronization*/

            sync();

break;

case 'u':/*trip AC contactor*/

            PADATDIR = PADATDIR & (~(1<<5)); /* AC link contactor*/

break;

case 'p':/*Go into control loop*/

            sync();

            demand();

break;

case 't':/*control ups*/

            control = 1;

break;

case 'g':/*control ups off*/

            control = 0;

        }
```

```
        }
    if ((j&0x0F)==0) {
      }
    wd_kick();
    }
  }
```

A.2 Metering and power control command

```
#define PWMA_PERIOD 1600  /* 20e6/2/15 = 20kHz */
#define PWM0_PERIOD 15625      // Together with init(5) = 20 Hz
#include <sys/f24x.h>
#include <sys/wd.h>
#include <sys/adc.h>
#include <sys/pwm0.h>
#include <sys/pwmA.h>
#include <sys/serial.h>
#include <sys/can.h>
//#include <ic/s_eeprom.h>
#include <ic/ds1629.h>
#include <ic/lcd.h>
#include <compute/mathi.h>
#include <compute/stat.h>
#pragma DATA_SECTION(time_count,".bakmem")
u16 time_count;
#pragma DATA_SECTION(v_max,".bakmem")
#pragma DATA_SECTION(i_max,".bakmem")
STAT_MAX_S16 v_max[3]={ STAT_MAX_S16_DEFAULTS,
                        STAT_MAX_S16_DEFAULTS,
                        STAT_MAX_S16_DEFAULTS} ;
```

```
STAT_AVG_S16 v_avg[3]={ STAT_AVG_S16_DEFAULTS,
                STAT_AVG_S16_DEFAULTS,
                STAT_AVG_S16_DEFAULTS} ;
STAT_AVG_S32 v_sqr[3]={ STAT_AVG_S32_DEFAULTS,
                STAT_AVG_S32_DEFAULTS,
                STAT_AVG_S32_DEFAULTS} ;
STAT_MAX_S16 i_max[3]={ STAT_MAX_S16_DEFAULTS,
                STAT_MAX_S16_DEFAULTS,
                STAT_MAX_S16_DEFAULTS} ;
STAT_AVG_S16 i_avg[3]={ STAT_AVG_S16_DEFAULTS,
                STAT_AVG_S16_DEFAULTS,
                STAT_AVG_S16_DEFAULTS} ;
STAT_AVG_S32 i_sqr[3]={ STAT_AVG_S32_DEFAULTS,
                STAT_AVG_S32_DEFAULTS,
                STAT_AVG_S32_DEFAULTS} ;
STAT_AVG_S32 pwr[3]  ={ STAT_AVG_S32_DEFAULTS,
                STAT_AVG_S32_DEFAULTS,
                STAT_AVG_S32_DEFAULTS} ;
void log0_update_ph(u08 ph, s16 c1_tmp, s16 c2_tmp) {
 v_avg[ph].update(&(v_avg[ph]), c1_tmp); c1_tmp-=v_avg[ph].value;
 v_max[ph].update(&(v_max[ph]), c1_tmp);
 v_sqr[ph].update(&(v_sqr[ph]), (s32)c1_tmp*(s32)c1_tmp);
 i_avg[ph].update(&(i_avg[ph]), c2_tmp); c2_tmp-=i_avg[ph].value;
 i_max[ph].update(&(i_max[ph]), c2_tmp);
 i_sqr[ph].update(&(i_sqr[ph]), (s32)c2_tmp*(s32)c2_tmp);
 pwr[ph].update(&(pwr[ph]), (s32)c1_tmp*(s32)c2_tmp);
 }
void pwmA_PD_interrupt(){
```

```
 EVIFRA = 0x0001;
 }
void pwm0_interrupt() {
 time_count++;
 EVIFRB = 0x000F;          /* Reset Interrupt */
 }
void pwmA_interrupt() {
 s16 c1_tmp, c2_tmp;
 asm(" SETC XF");
 /* Phase R */
 adc_get2_start(1,0);
 adc_get2_stop(&c1_tmp,&c2_tmp);
 c1_tmp=(c1_tmp<<4)-SC; c2_tmp=(c2_tmp<<4)-SC;
 log0_update_ph(0,c1_tmp,c2_tmp);
 /* Phase S */
 adc_get2_start(3,2);
 adc_get2_stop(&c1_tmp,&c2_tmp);
 c1_tmp=(c1_tmp<<4)-SC; c2_tmp=(c2_tmp<<4)-SC;
 log0_update_ph(1,c1_tmp,c2_tmp);

 /* Phase T */
 adc_get2_start(5,4);
 adc_get2_stop(&c1_tmp,&c2_tmp);
 c1_tmp=(c1_tmp<<4)-SC; c2_tmp=(c2_tmp<<4)-SC;
 log0_update_ph(2,c1_tmp,c2_tmp);
 asm(" CLRC XF");
 EVIFRA= 0x0780;  /* Reset Interrupt */
 }
```

```
void main_init_startup(void) {
  asm(" BCND 01F00h, BIO"); /* For boot loader */
  f24x_init();
  wd_init();
  asm(" CLRC XF");
  ser_init(42);
  can_init(500);
  }
void main_init_timer(void) {
  pwm0_init(5);
  pwm0_init_interrupt();
  /* pwm0_put(PWMA_PERIOD/2); */
  pwmA_init();
  pwmA_init_interrupt();
  /* pwmA_put1(50); pwmA_put2(100); pwmA_put3(150); */
  }
void main_init(void) {
  main_init_startup();
  adc_init();
  main_init_timer();
  /* Write Intro */
   ser_puts("I-Tec");
   SER_NEWLINE();
  }
void main(void) {
  u16 old_time_count,c,syn;
  s16 pa,pb,pc;
  s32 set ;
```

```
 main_init();
 syn = 0;
 set = 0;
while(1) {
  old_time_count=time_count;
  if ((old_time_count%20)==0) {
   ser_puts(" P0="); ser_putd_s32(pwr[0].value);
   ser_puts(" P1="); ser_putd_s32(pwr[1].value);
   ser_puts(" P2="); ser_putd_s32(pwr[2].value);
   ser_puts(" Syns="); ser_putd_s16(syn);
   ser_puts(" Set="); ser_putd_s32(set);
   ser_puts("\r\n");
   }

  if ((c=ser_getc(2))!=0)
   {switch(c)  {
         case 'w': /* increase setpoint */
             set = set+1000;
         break;
         case 's': /* decrease setpoint */
             set = set-1000;
         }
   }
   if (pwr[0].value<set) pa=-1;
   if (pwr[0].value>set) pa=1;
   if (pwr[1].value<set) pb=-1;
   if (pwr[1].value>set) pb=1;
   if (pwr[2].value<set) pc=-1;
```

```
    if (pwr[2].value>set) pc=1;
    can_set_id(4,'a');
    can_put8(4,pa,pb,pc,0);
  do {
   wd_kick();
   } while(old_time_count==time_count);
  }
}
```

Appendix B

Matlab Program

B.1 PWM Harmonics analysis

```
sampling = 1e-7;        %sampling time 1e-7%
ma = 0.8;               %Amplitude Modulation index %
fa = 1000;              %Carier Frequency 10000
f = 50;                 %Fundamental Frequency
ft = 0.08;              %Final time
fifty = 50/((1/sampling)/(ft/sampling));
mf = (fa/50)*fifty;
t=0:(sampling):ft;
ctrl=ma*sin(2*pi*50*t);  %Create sin waveform for control signal%
tri=asin(sin(2*pi*fa*t)); %Create triangular waveform for carier%
tri=tri/asin(1);
pwm=(ctrl>tri);          %Find PWM modulation if Control less than trinangular get
                           logic 1%
                         %ctrl=0;
                         %tri=0;
fre=size(t);
fre=fre(2);
                         %t=0;
freq=0:((1/sampling)/(fre-1)):(1/sampling);
pwm=(pwm-0.5)*2;         %Remove dc component and scale up to 1%

fff = fft(pwm);
```

```
abs(fff(fifty+1));

abs(fff(mf+1));

 k  = 1:1:(fre-1);

b  = (-2/(ft/sampling))*imag(fff);

a  = (2*real(fff)/(ft/sampling));

case1= [ abs(b(mf+1))

  abs(b(mf+2*fifty+1))

  %abs(b(mf-2*fifty+1))

  abs(b(mf+4*fifty+1))

  %abs(b(mf-4*fifty+1))

  abs(b((2*mf)+1*fifty+1))

  %abs(b((2*mf)-1*fifty+1))

  abs(b((2*mf)+3*fifty+1))

  %abs(b((2*mf)-3*fifty+1))

  abs(b((2*mf)+5*fifty+1))

  %abs(b((2*mf)-5*fifty+1))

  abs(b((3*mf)+1))

  abs(b((3*mf)+2*fifty+1))

  %abs(b((3*mf)-2*fifty+1))

  abs(b((3*mf)+4*fifty+1))

  %abs(b((3*mf)-4*fifty+1))

  abs(b((3*mf)+6*fifty+1))

  %abs(b((3*mf)-6*fifty+1))

  abs(b((4*mf)+1*fifty+1))

  %abs(b((4*mf)-1*fifty+1))
```

```
  abs(b((4*mf)+3*fifty+1))
  %abs(b((4*mf)-3*fifty+1))
  abs(b((4*mf)+5*fifty+1))
  %abs(b((4*mf)-5*fifty+1))
  %abs(b((4*mf)+7*fifty+1))
  abs(b((4*mf)-7*fifty+1))
 ]
 %plot(freq,b)
%axis([0,200e3,0,1.5]);
%figure(2);
hell = abs(b);
plot(freq,hell)
axis([-5e3,300e3,0,1.5]);
ylabel('Magnitude');
xlabel('Frequency');
 figure(2)
subplot(2,1,1);
plot(t,ctrl);
axis([0,0.02,-1.5,1.5]);
hold on;
plot(t,tri);
axis([0,0.02,-1.5,1.5]);
hold off;
xlabel('Time Second');
ylabel('Magnitude');
```

```
%axis([0,0.02,-1.5,1.5]);
%subplot(2,1,2);
%plot(t,tri);
%axis([0,0.02,-1.5,1.5]);
subplot(2,1,2);
plot(t,pwm);
axis([0,0.02,-1.5,1.5]);
xlabel('Time Second');
ylabel('Magnitude');
```

B.2 LC filter Bode plot

```
r  = 20/(220/30)^2;
l  = 107.62e-3;
c  = 1e-6
% vout/vin = 1/(S^2LC+SRC+1)

aa=tf([0 1],[(l*c) (r*c) 1]);
bb=tf([0 1],[(l*c) 0 1]);
bode(aa,{(2*pi),(100e3*pi)})
figure(2)
bode(bb,{(2*pi),(100e3*pi)})
[a,b]=bode(aa,(50*(2*pi)))
[a1,b1]=bode(aa,(10e3*(2*pi)))
```

B.3 Power flow

```
delta  = -pi:(2*pi/360):pi;%angle between Vinv and Vs
t      = delta*180/pi;
Vs     = 220; %Source Voltage
E      = 340; %Inverter Voltage
r      = 20; %resistance of Z
L      = 107.62e-3; %inductor value
f      = 50; %frequency
XL     = 2*pi*f*L; %inductor impedance or inductance
Z      = r+i*XL; %Impedance of system
zeta   = atan(XL/r); %Angle of Impedance

PXL    = (Vs*E/XL)*sin(delta); %Power in case no resistance
QXL    = (Vs^2/XL)-(Vs*E/XL)*cos(delta); %Reactive Power in case no resistance
P      = (Vs*E)*cos(delta-zeta)/sqrt(r^2+XL^2)-Vs^2*cos(zeta)/sqrt(r^2+XL^2);
%Power in case including resistance
Q      = (Vs*E)*sin(delta-zeta)/sqrt(r^2+XL^2)+Vs^2*sin(zeta)/sqrt(r^2+XL^2);
%subplot(2,1,1);
plot(t,PXL,'b-')
hold
plot(t,QXL,'g-')
axis([-180,180,-3000,4000])
%subplot(2,1,2);
plot(t,P,'r-')
%hold
```

```
plot(t,Q,'m-')
axis([-180,180,-3000,4000])
xlabel('Angle Degree');
ylabel('Power and Reactive power Watt,Var');
legend('Power without R', 'Reactive Power without R', 'Power with R', 'Reactive
Power with R');
grid on
```

B.4 BESS operation charts

```
Vs    = 220;
I     = 2;
f     = 50;
L     = 107.62e-3;
r     = 20;
%r    = 0;
XL    = 2*pi*f*L;
fi    = 0:1:360;
firad = ((2*pi)/360)*fi;
Z     = r + XL*i;
%Calculate VL IL*XL%
pf    = cos(firad);
IL    = I*cos(firad)+(I*sin(firad))*i;
VL    = IL*Z;
Vinv  = VL + Vs;
ABSVinv = abs(Vinv);
```

```
delta   = angle(Vinv);
delta   = delta*(360/2/pi);
VLreal  = real(VL);
VLimag  = imag(VL);
%subplot(2,1,1);
plot(ABSVinv,delta)
%ylabel('Angle in Degree (delta)');
title('Angle in Degree (delta)');
xlabel('Magnitude in Volts');
text(abs(Vinv(1)),delta(1),'upf = 1.00')
text(abs(Vinv(31)),delta(31),'pf = 0.87 lag')
text(abs(Vinv(61)),delta(61),'pf = 0.50 lag')
text(abs(Vinv(91)),delta(91),'pf = 0.00 lag')
text(abs(Vinv(121)),delta(121),'pf = 0.50 lag')
text(abs(Vinv(151)),delta(151),'pf = 0.87 lag')
text(abs(Vinv(181)),delta(181),'upf = 1.00')
text(abs(Vinv(211)),delta(211),'pf = 0.87 lag')
text(abs(Vinv(241)),delta(241),'pf = 0.50 lag')
text(abs(Vinv(271)),delta(271),'pf = 0.00 lead')
text(abs(Vinv(301)),delta(301),'pf = 0.50 lead')
text(abs(Vinv(331)),delta(331),'pf = 0.87 lead')
text(abs(Vinv(361)),delta(361),'upf = 1')
grid on
%figure(2);
%plot(VLreal,VLimag);
```

%grid on

pf(1)

pf(31)

pf(61)

pf(91)

pf(121)

pf(151)

pf(181)

pf(211)

pf(241)

pf(271)

pf(301)

pf(331)

pf(361)

abs(Vinv(1))

abs(Vinv(31))

abs(Vinv(61))

abs(Vinv(91))

abs(Vinv(121))

abs(Vinv(151))

abs(Vinv(181))

abs(Vinv(211))

abs(Vinv(241))

abs(Vinv(271))

abs(Vinv(301))

abs(Vinv(331))

abs(Vinv(361))

delta(1)

delta(31)

delta(61)

delta(91)

delta(121)

delta(151)

delta(181)

delta(211)

delta(241)

delta(271)

delta(301)

delta(331)

delta(361)

B.5 Example of Harmonics analysis of output scope waveforms.

```
sampling = 1600;
ft       = 0.04;
fifty    = (50/(1/ft))+1;
a=1:1:sampling;
t=rawdat(a,1)*200;
f1=rawdat(a,2)*200;
f2=rawdat(a,3)*200;
f3=rawdat(a,4)*200;
```

```
f4=rawdat(a,5)*200;

f5=rawdat(a,6)*200;

ff1 = fft(f1);

ff2 = fft(f2);

ff3 = fft(f3);

ff4 = fft(f4);

ff5 = fft(f5);

b1  = (-2/(sampling))*imag(ff1);

b2  = (-2/(sampling))*imag(ff2);

b3  = (-2/(sampling))*imag(ff3);

b4  = (-2/(sampling))*imag(ff4);

b5  = (-2/(sampling))*imag(ff5);

a1  = 2*real(ff1)/sampling;

a2  = 2*real(ff2)/sampling;

a3  = 2*real(ff3)/sampling;

a4  = 2*real(ff4)/sampling;

a5  = 2*real(ff5)/sampling;

a01  = ff1(1)/sampling;

a02  = ff2(1)/sampling;

a03  = ff3(1)/sampling;

a04  = ff4(1)/sampling;

a05  = ff5(1)/sampling;

out1 = sqrt(a1.^2+b1.^2);

out2 = sqrt(a2.^2+b2.^2);

out3 = sqrt(a3.^2+b3.^2);
```

```
out4 = sqrt(a4.^2+b4.^2);
out5 = sqrt(a5.^2+b5.^2);
subplot(2,1,1);
plot(f1)
ylabel('Voltage(L-L)')
xlabel('Frequency(Hz)')
grid on
subplot(2,1,2);
plot((a-1)*25,out1)
axis([0,1e3,0,600]);
ylabel('Voltage(L-L)')
xlabel('Frequency(Hz)')
grid on
figure(2)
subplot(2,1,1);
plot(f2)
ylabel('Voltage(L-L)')
xlabel('Frequency(Hz)')
grid on
subplot(2,1,2);
plot((a-1)*25,out2)
axis([0,1e3,0,600]);
ylabel('Voltage(L-L)')
xlabel('Frequency(Hz)')
grid on
```

```
figure(3)
subplot(2,1,1);
plot(f3)
ylabel('Voltage(L-L)')
xlabel('Frequency(Hz)')
grid on
subplot(2,1,2);
plot((a-1)*25,out3)
axis([0,1e3,0,600]);
ylabel('Voltage(L-L)')
xlabel('Frequency(Hz)')
grid on
figure(4)
subplot(2,1,1);
plot(f4)
ylabel('Voltage(L-L)')
xlabel('Frequency(Hz)')
grid on
subplot(2,1,2);
plot((a-1)*25,out4)
axis([0,1e3,0,600]);
ylabel('Voltage(L-L)')
xlabel('Frequency(Hz)')
grid on
```

```
figure(5)
subplot(2,1,1);
plot(f5)
ylabel('Voltage(L-L)')
xlabel('Frequency(Hz)')
grid on
subplot(2,1,2);
plot((a-1)*25,out5)
axis([0,1e3,0,800]);
ylabel('Voltage(L-L)')
xlabel('Frequency(Hz)')
grid on
%Thd Calculation
a1 = a1(2:length(a1)/2);
b1 = b1(2:length(b1)/2);
a2 = a2(2:length(a2)/2);
b2 = b2(2:length(b2)/2);
a3 = a3(2:length(a3)/2);
b3 = b3(2:length(b3)/2);
a4 = a4(2:length(a4)/2);
b4 = b4(2:length(b4)/2);
a5 = a5(2:length(a5)/2);
b5 = b5(2:length(b5)/2);
fifty = fifty-1;
```

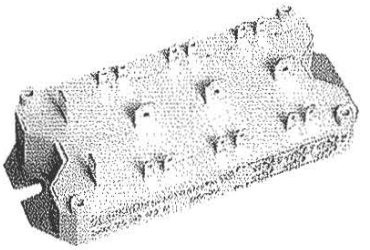
```
out1 = sqrt(a1.^2+b1.^2);

out2 = sqrt(a2.^2+b2.^2);

out3 = sqrt(a3.^2+b3.^2);

out4 = sqrt(a4.^2+b4.^2);

out5 = sqrt(a5.^2+b5.^2);

thd1=(sqrt(((sqrt(sum(a1.^2+b1.^2)))^2)-((out1(fifty))^2))/out1(fifty))*100

thd2=(sqrt(((sqrt(sum(a2.^2+b2.^2)))^2)-((out2(fifty))^2))/out2(fifty))*100

thd3=(sqrt(((sqrt(sum(a3.^2+b3.^2)))^2)-((out3(fifty))^2))/out3(fifty))*100

thd4=(sqrt(((sqrt(sum(a4.^2+b4.^2)))^2)-((out4(fifty))^2))/out4(fifty))*100

thd5=(sqrt(((sqrt(sum(a5.^2+b5.^2)))^2)-((out5(fifty))^2))/out5(fifty))*100

out1(fifty)/sqrt(2)

out2(fifty)/sqrt(2)

out3(fifty)/sqrt(2)

out4(fifty)/sqrt(2)

out5(fifty)/sqrt(2)
```

Absolute Maximum Ratings Symbol	Conditions [1]	Values	Units
V_{CES}		1200	V
V_{CGR}	R_{GE} = 20 kΩ	1200	V
I_C	T_{case} = 25/80 °C	40 / 30	A
I_{CM}	T_{case} = 25/80 °C; t_p = 1 ms	70 / 50	A
V_{GES}		± 20	V
P_{tot}	per IGBT, T_{case} = 25 °C	220	W
T_j, (T_{stg})		– 40 . . .+150 (125)	°C
V_{isol}	AC, 1 min.	2 500	V
humidity	DIN 40 040	Class F	
climate	DIN IEC 68 T.1	40/125/56	
Inverse Diode			
I_F= – I_C	T_{case} = 25/80 °C	45 / 30	A
I_{FM}= – I_{CM}	T_{case} = 25/80 °C; t_p = 1 ms	70 / 50	A
I_{FSM}	t_p = 10 ms; sin.; T_j = 150 °C	350	A
I^2t	t_p = 10 ms; T_j = 150 °C	600	A^2s

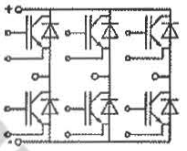
Characteristics Symbol	Conditions [1]	min.	typ.	max.	Units
$V_{(BR)CES}$	V_{GE} = 0, I_C = 0,8 mA	≥ V_{CES}	–	–	V
$V_{GE(th)}$	V_{GE} = V_{CE}, I_C = 1 mA	4,5	5,5	6,5	V
I_{CES}	V_{GE} = 0, T_j = 25 °C	–	0,1	1	mA
	V_{CE} = V_{CES}, T_j = 125 °C	–	3	–	mA
I_{GES}	V_{GE} = 20 V, V_{CE} = 0	–	–	200	nA
V_{CEsat}	I_C = 25 A; V_{GE} = 15 V; T_j = 25 (125) °C	–	2,5(3,1)	3(3,7)	V
V_{CEsat}	I_C = 40 A; V_{GE} = 15 V; T_j = 25 (125) °C	–	3,1(3,9)	–	V
g_{fs}	V_{CE} = 20 V, I_C = 25 A		20	–	S
C_{CHC}	per IGBT	–	–	300	pF
C_{ies}	V_{GE} = 0, V_{CE} = 25 V, f = 1 MHz	–	1600	2100	pF
C_{oes}		–	250	300	pF
C_{res}		–	110	150	pF
L_{CE}		–	–	60	nH
$t_{d(on)}$	V_{CC} = 600 V	–	70	–	ns
t_r	V_{GE} = + 15 V / - 15 V [3]	–	55	–	ns
$t_{d(off)}$	I_C = 25 A, ind. load	–	400	–	ns
t_f	R_{Gon} = R_{Goff} = 40 Ω	–	40	–	ns
E_{on} [5]	T_j = 125 °C	–	3,8	–	mWs
E_{off} [5]		–	2,3	–	mWs
Inverse Diode [8]					
V_F = V_{EC}	I_F = 25 A; V_{GE} = 0 V; T_j = 25 (125) °C	–	2,0(1,8)	2,5	V
V_F = V_{EC}	I_F = 40 A; V_{GE} = 0 V; T_j = 25 (125) °C	–	2,3(2,1)	–	V
V_{TO}	T_j = 125 °C	–	1,1	1,2	V
r_T	T_j = 125 °C	–	25	44	mΩ
I_{RRM}	I_F = 25 A; T_j = 25 (125) °C [2]	–	19(25)	–	A
Q_{rr}	I_F = 25 A; T_j = 25 (125) °C [2]	–	1,5(4,5)	–	µC
Thermal Characteristics					
R_{thjc}	per IGBT	–	–	0,56	°C/W
R_{thjc}	per diode	–	–	1,0	°C/W
R_{thch}	per module	–	–	0,05	°C/W

SEMITRANS® M
IGBT Modules

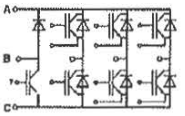
SKM 40 GD 123 D
SKM 40 GD 123 D L*)
SKM 40 GDL 123 D **)



Sixpack



GD



GDL **)

Features

- MOS input (voltage controlled)
- N channel, homogeneous Si
- Low inductance case
- Very low tail current with low temperature dependence
- High short circuit capability, self limiting to 6 * I_{cnom}
- Latch-up free
- Fast & soft inverse CAL diodes [8]
- Isolated copper baseplate using DCB Direct Copper Bonding Technology
- Large clearance (9 mm) and creepage distances (13 mm).

Typical Applications

- Switched mode power supplies
- Three phase inverters for AC motor speed control
- Pulse frequencies also above 15 kHz

1) T_{case} = 25 °C, unless otherwise specified
2) I_F = – I_C, V_R = 600 V, – di_F/dt = 500 A/µs, V_{GE} = 0 V
3) Use V_{GEoff} = -5 ... -15 V
5) See fig. 2 + 3; R_{Goff} = 40 Ω
8) CAL = Controlled Axial Lifetime Technology.

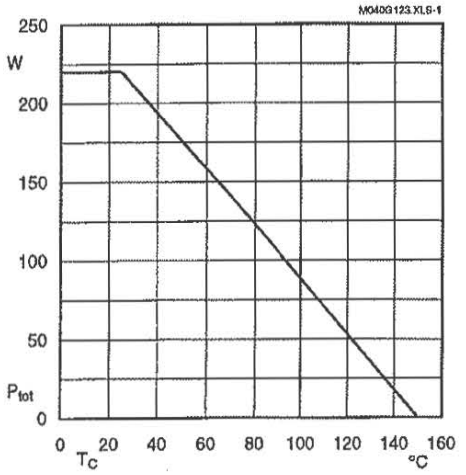
***) Main terminals = 2 mm dia.**

outline → B 6 – 68

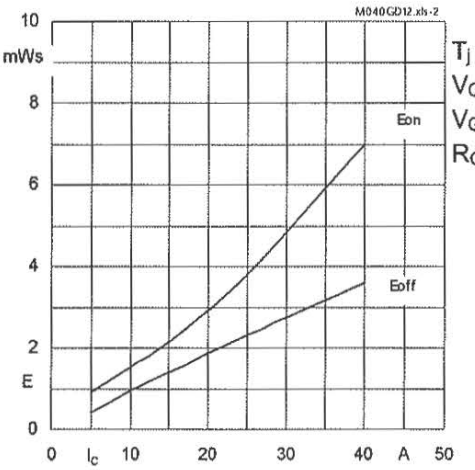
****) Sevenpack, picture → B6 - 99**

Cases and mech. data → B6 - 74

Sixpack and Sevenpack

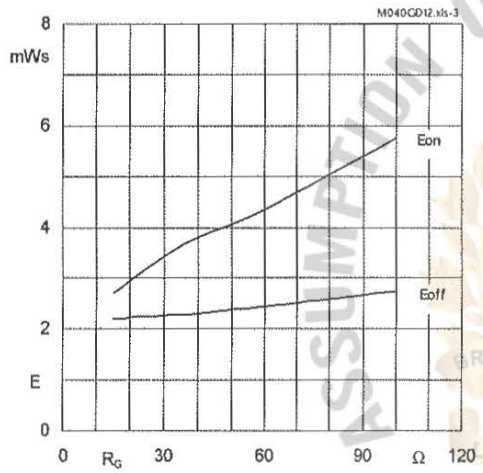


ig. 1 Rated power dissipation $P_{tot} = f(T_C)$



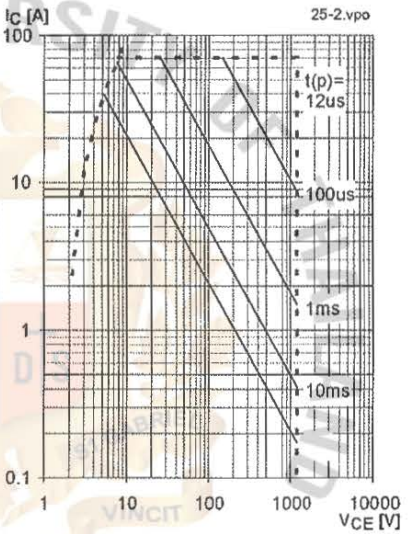
T_j = 125 °C
V_{CE} = 600 V
V_{GE} = ± 15 V
R_G = 40 Ω

Fig. 2 Turn-on /-off energy = f (I_C)



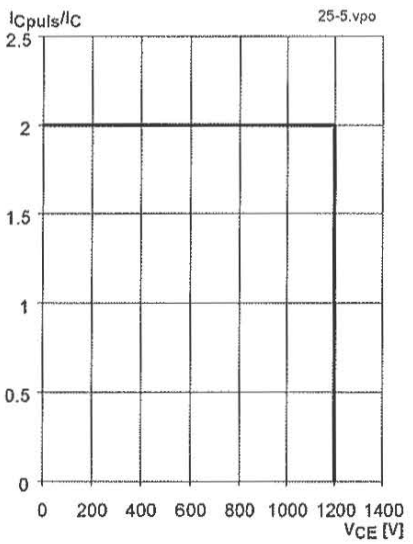
T_j = 125 °C
V_{CE} = 600 V
V_{GE} = ± 15 V
I_C = 25 A

ig. 3 Turn-on /-off energy = f (R_G)



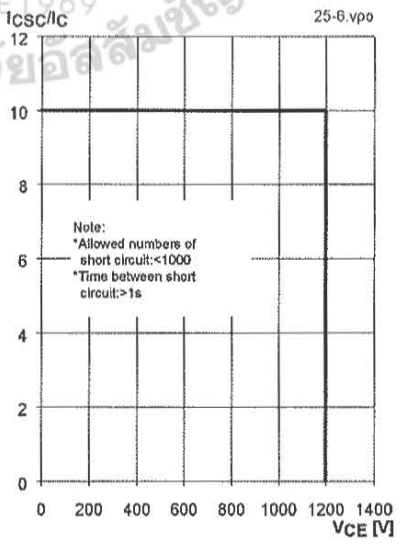
1 pulse
T_C = 25 °C
$T_j \leq$ 150 °C

Fig. 4 Maximum safe operating area (SOA) $I_C = f(V_{CE})$



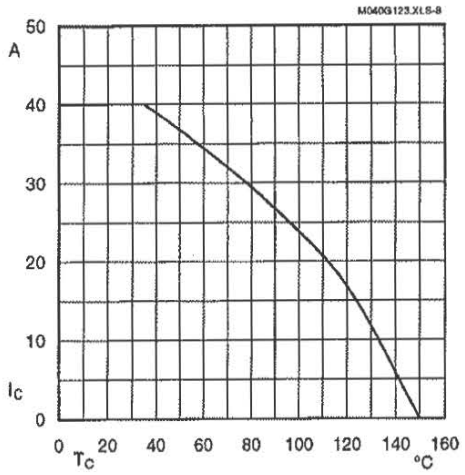
$T_j \leq$ 150 °C
V_{GE} = ± 15 V
R_{Goff} = 40 Ω
I_C = 25 A

g. 5 Turn-off safe operating area (RBSOA)



$T_j \leq$ 150 °C
V_{GE} = ± 15 V
$t_{sc} \leq$ 10 µs
L < 50 nH
I_C = 25 A

Fig. 6 Safe operating area at short circuit $I_C = f(V_{CE})$



T_j = 150 °C
$V_{GE} \geq$ 15 V

Fig. 8 Rated current vs. temperature $I_C = f(T_C)$

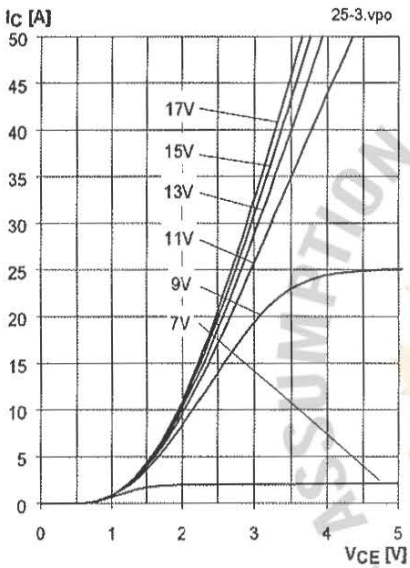


Fig. 9 Typ. output characteristic, t_p = 80 µs; 25 °C

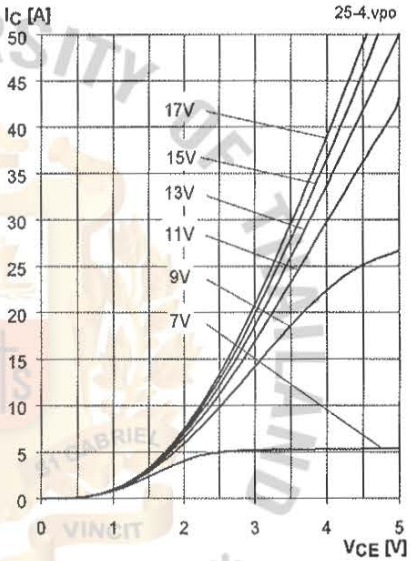


Fig. 10 Typ. output characteristic, t_p = 80 µs; 125 °C

$P_{cond(t)} = V_{CEsat(t)} \cdot I_{C(t)}$

$V_{CEsat(t)} = V_{CE(TO)(Tj)} + r_{CE(Tj)} \cdot I_{C(t)}$

$V_{CE(TO)(Tj)} \leq 1{,}5 + 0{,}002\ (T_j - 25)$ [V]

typ.: $r_{CE(Tj)} = 0{,}040 + 0{,}00016\ (T_j - 25)$ [Ω]

max.: $r_{CE(Tj)} = 0{,}060 + 0{,}00020\ (T_j - 25)$ [Ω]

valid for $V_{GE} = +15\ ^{+2}_{-1}$ [V]; $I_C \geq 0{,}3\ I_{Cn}$

Fig. 11 Saturation characteristic (IGBT)
Calculation elements and equations

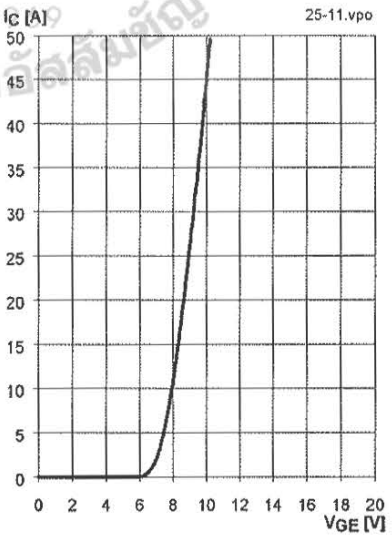
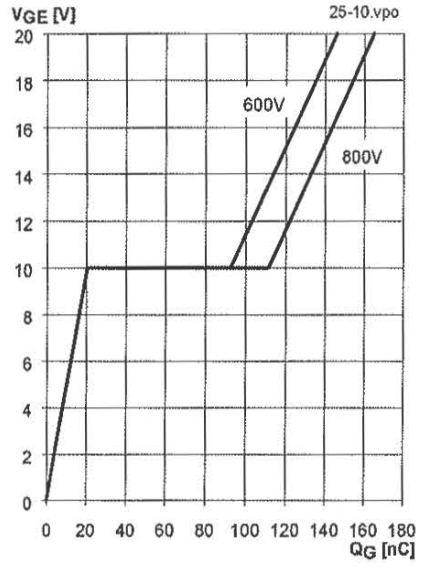
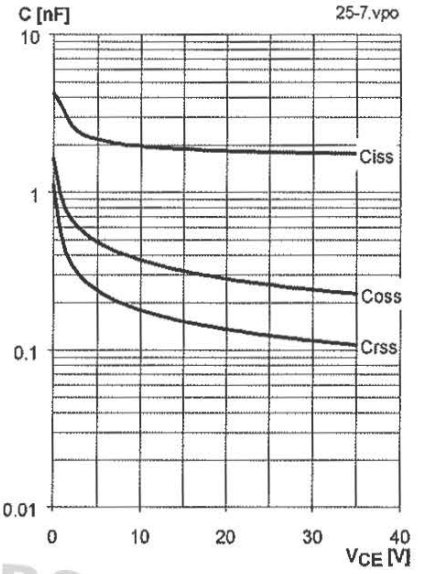


Fig. 12 Typ. transfer characteristic, t_p = 80 µs; V_{CE} = 20 V



ig. 13 Typ. gate charge characteristic

I_{Cpuls} = 25 A

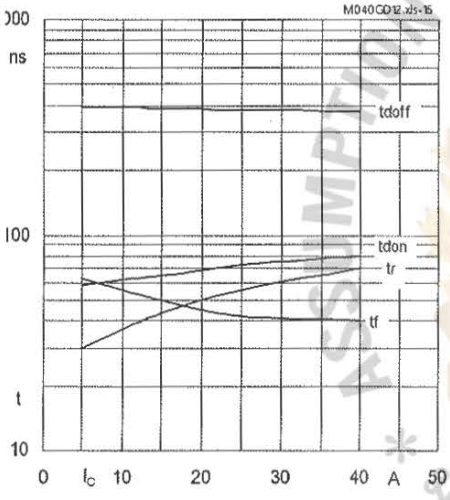


V_{GE} = 0 V
f = 1 MHZ

C_{ies}

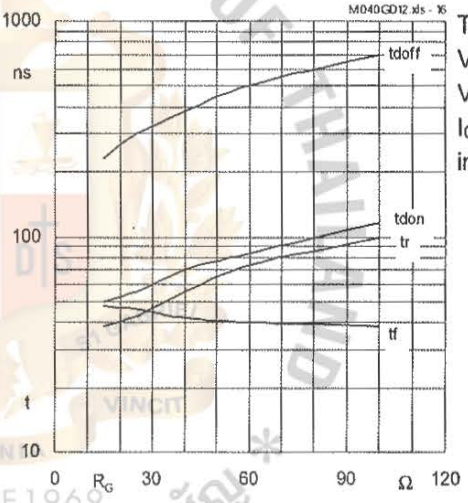
C_{oes}
C_{res}

Fig. 14 Typ. capacitances vs.V_{CE}



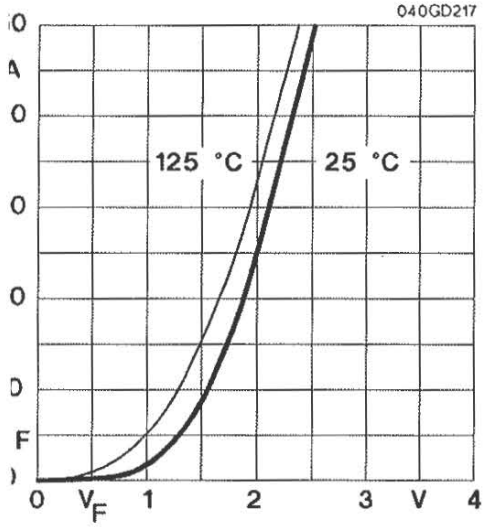
g. 15 Typ. switching times vs. I_C

T_j = 125 °C
V_{CE} = 600 V
V_{GE} = ± 15 V
R_{Gon} = 40 Ω
R_{Goff} = 40 Ω
induct. load



T_j = 125 °C
V_{CE} = 600 V
V_{GE} = ± 15 V
I_C = 25 A
induct. load

Fig. 16 Typ. switching times vs. gate resistor R_G



g. 17 Typ. CAL diode forward characteristic

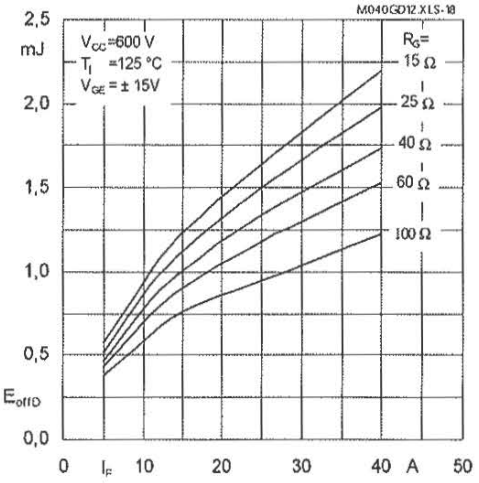


Fig. 18 Diode turn-off energy dissipation per pulse

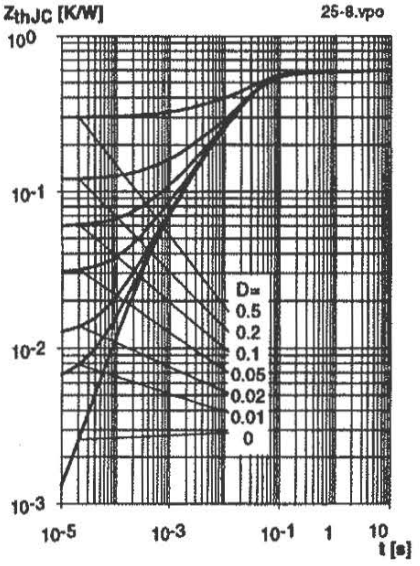


Fig. 19 Transient thermal impedance of IGBT
$Z_{thJC} = f(t_p)$; $D = t_p / t_c = t_p \cdot f$

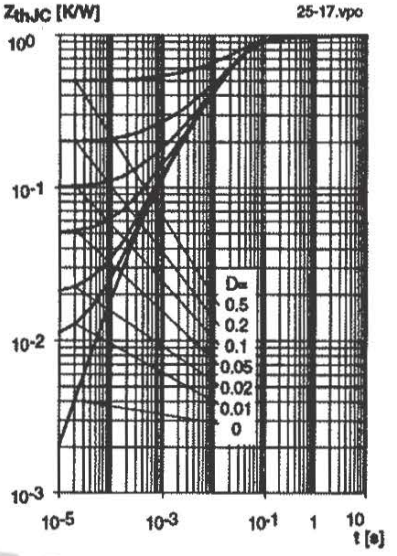


Fig. 20 Transient thermal impedance of inverse CAL diodes $Z_{thJC} = f(t_p)$; $D = t_p / t_c = t_p \cdot f$

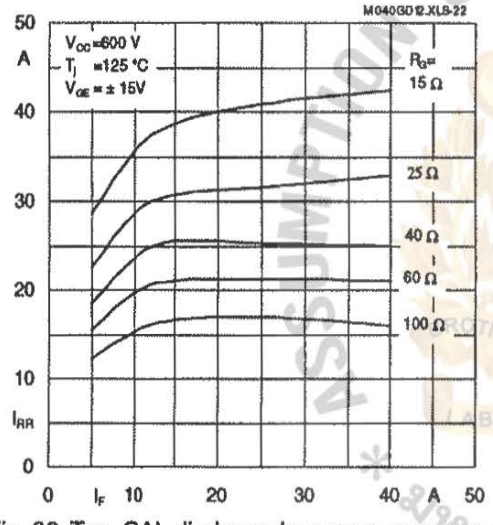


Fig. 22 Typ. CAL diode peak reverse recovery current $I_{RR} = f(I_F; R_G)$

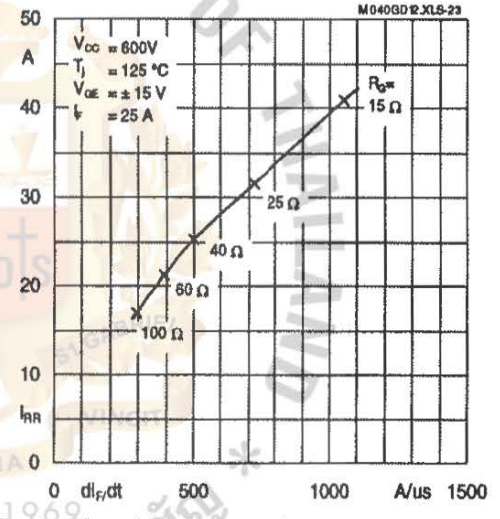


Fig. 23 Typ. CAL diode peak reverse recovery current $I_{RR} = f(di/dt)$

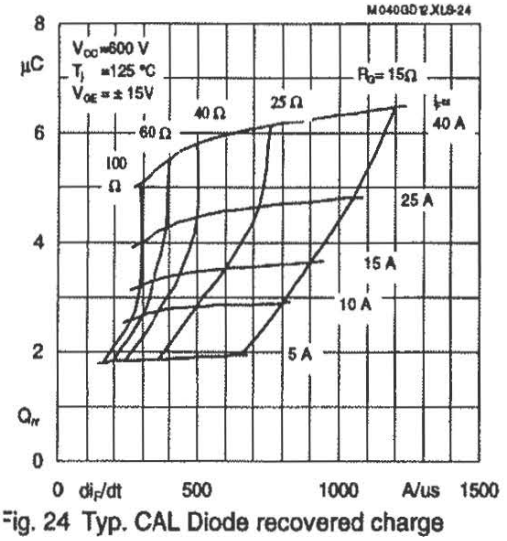


Fig. 24 Typ. CAL Diode recovered charge

SEMITRANS Sixpack

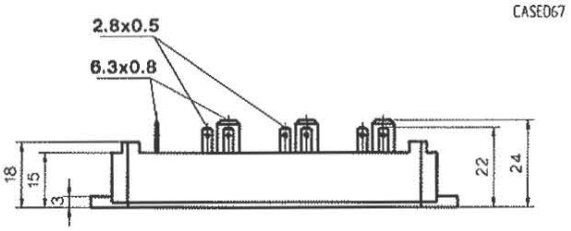
Case D 67

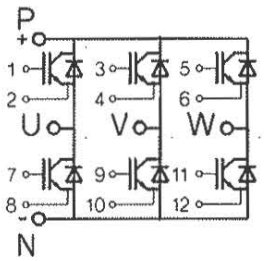
UL Recognized

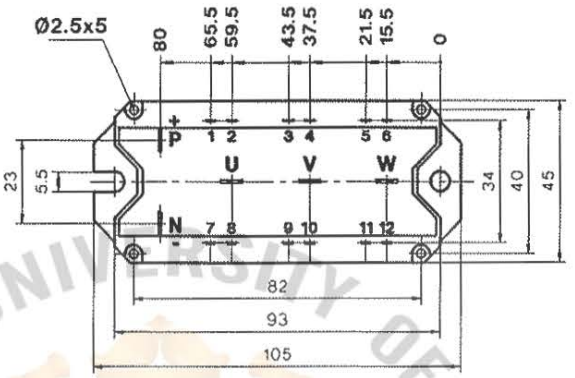
File no. E 63 532

SKM 40 GD 123 D

CASED67







SEMITRANS Sevenpack

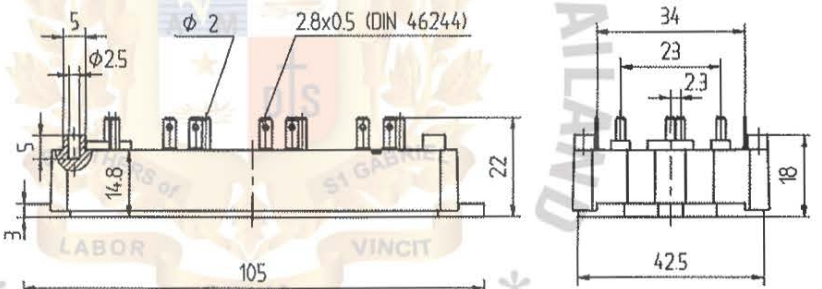
Case D 73

UL Recognized

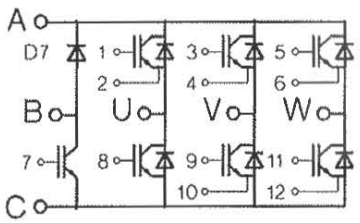
File no. E 63 532

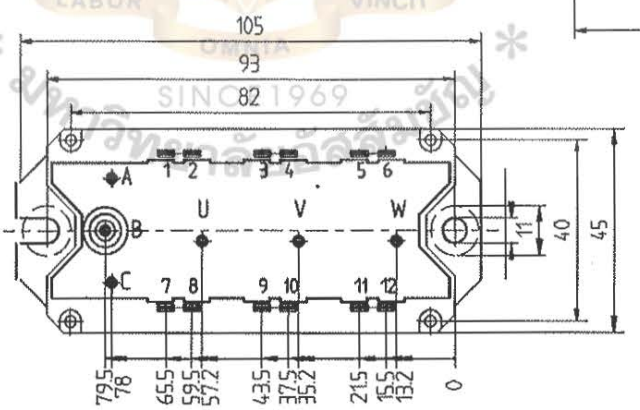
SKM 40 GDL 123 D

CASED73



GCIGGDL





Dimensions in mm

ase outlines and circuit diagrams

Mechanical Data

Symbol	Conditions		Values min.	typ.	max.	Units
M_1	to heatsink, SI Units	(M5)	4	–	5	Nm
	to heatsink, US Units		35	–	44	lb.in.
			–	–	5x9,81	m/s^2
			–	–	175	g

This is an electrostatic discharge sensitive device (ESD). Please observe the international standard IEC 747-1, Chapter IX.

Two devices are supplied in one SEMIBOX A.

Larger packing units (10 and 20 pieces) are used if suitable.

SEMIBOX→ C – 1.