

The Fault Tolorance Modification of Benes Network

Mr. Montai Settapokin 381 6199

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Presented to

Dr. Guennadi Vesselovski

By

1. Mr. Montai	Settapokin	Adm.Code no. 381 6199
2. Ms. Taminee	Shinasharkey	Adm.Code no. 381 6293

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We sincerely welcome comment, suggestions and tactfully stated criticisms from the reader and others that may come into contact with this report.

Mr. Montai Settapokin
Ms. Taminee Shinasharkey

ABSTRACT

This project is about the fault tolerant modification of Benes Network. Benes Network is a kind of multistage switching network with no blocking, and it's fault tolerant modification guarantee that when there is a fault occurs in the network, the data can still reach it's destination using an alternate path.



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CHAPTER 1 :

INTRODUCTION



INTRODUCTION

Single instruction stream-multiple data stream (SIMD) multiprocessor computing systems have a significant place among parallel computing system architectures. In these systems, N processors or “processor elements” (PE) execute the same instruction with different operands. SIMD computers are vector machines with speed currently in the range of billions and tens of billions of floating-point arithmetic operations per second; the number of processors in the system may reach several thousands. One of the main difficulties in SIMD computers, as in other parallel systems, is timely delivery of data to all the processors. Efficient choice of switching networks helps to overcome this difficulty.

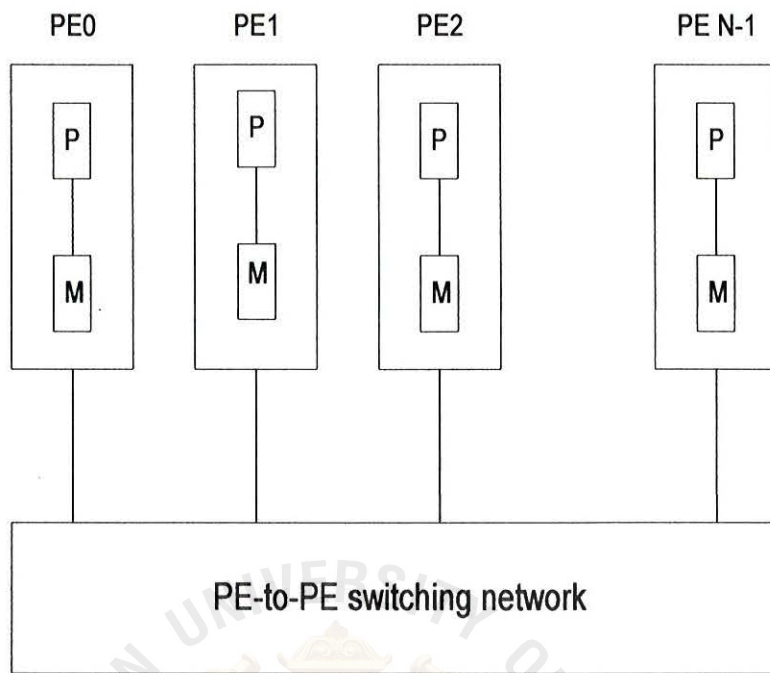
Two basic switching structures are available for SIMD computers. In the first structure (Fig. 1a), each processor has its own individual memory M and is linked by a switching network to other identical processors. In the second structure, the switching network is interposed between the processors and the shared memory modules M of all the processors (Fig. 1b).

The advantage of the second switching structure compared with the first is that each processor has access to the entire addressing space of the shared memory. The main shortcomings are additional delay introduced by the switching network when accessing the memory and the possibility of collision when two or more processors try to access the same memory module.

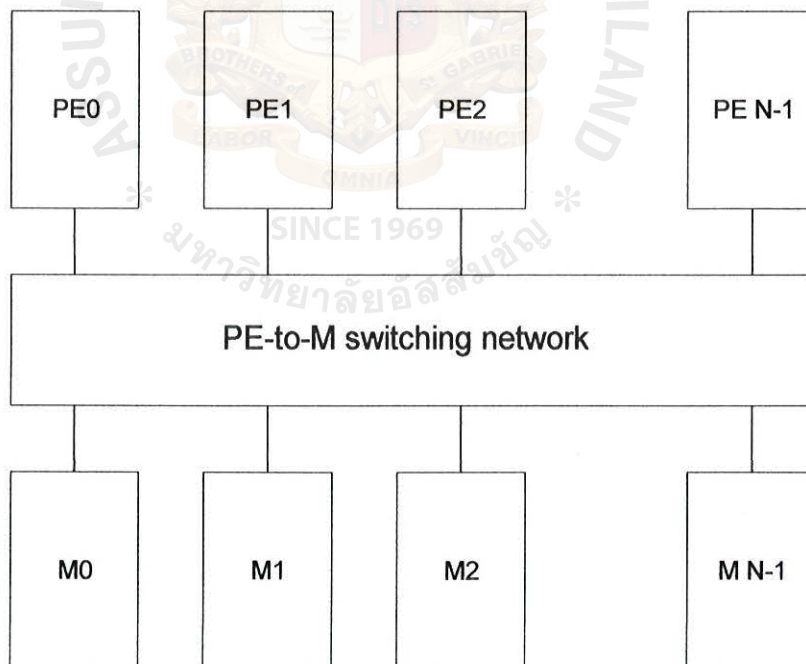
Sequential switching structures originally used in early SIMD computers, e.g., the connection of each PE to four neighbors in Illiac, are an obstacle to increasing the performance of new-generation systems, while the crossbar switch for a system with hundreds and certainly thousands of PEs should be prohibitively costly. Literature analysis shows that the design of switching systems in these architectures largely relied on multistage switching networks (MSN).

MSN are designed for both synchronous and asynchronous parallel systems with a large number of PEs (hundreds and more), where crossbar switching provides the only competitive alternative in performance terms. We will show that MSN have certain advantages compared to crossbar switching systems – the hardware costs are lower and the performance is higher, but the MSN are more difficult to control. In the last two decades, the theory of these networks has made considerable progress and some successful implementations are known.

We consider the main properties and parameter of multistage switching networks and perform a comparative analysis of various MSN types. We consider the techniques for improving their fault-tolerance, and estimate the gain in execution time of some standard procedures with MSN compared to sequential ring type switching systems. Of the enormous variety of multistage switching system configurations, we only consider the basic topologies, which have been implemented or are reportedly being incorporated in future, SIMD supercomputers.



a.



b.

Fig. 1

CHAPTER 2 :

THEORY AND DESIGN



BASIC TYPES OF DATA TRANSFER

The choice of the switching network depends on the frequently used types of messages. The attempts to identify the main types of data transfer in parallel computing systems are of fairly recent origin. The classification of frequently used permutations proposed by Lenfant has become quite popular. According to this classification, the main types of permutations can be grouped into five families. Below we present the main results of the classification of transfers for SIMD computers, based on actual experience with the PS-2000 computers, which supports the validity of this classification.

Frequently used permutations include arbitrary shifts and perfect shuffle. Programming experience on the Illiac IV has shown that these permutations occur so frequently in user programs that to be acceptable, a switching network must ensure efficient implementation of these basic permutations.

Let n be a positive integer, E^n the set of binary vectors $x = (x_n, x_{n-1}, \dots, x_1)$ representing the integers $:= \sum x_i 2^{i-1}$ from 0 to $2^{n-1} - 1$. In application to our case, there are the processor addresses. Then an arbitrary shift by a implies that any z is mapped to $(z + a) \bmod 2^n$, where a is an integer.

Of practical interest are also cyclic shifts of amplitude a within the segment 2^{n-j} , i.e., $z \rightarrow (z + a) \bmod 2^{n-j}$. Efficient execution of arbitrary shifts primarily requires matrix transposition. Matrix transposition is one of the basic procedures in statistical analysis of large vectors and matrices, in aero and hydrodynamic problems, in linear algebra problems, and in some other problems, and it urgently needs hardware support.

The so-called perfect shuffle permutation is a mapping on the component i mapping on the components of the binary vector x :

$$x = (x_n, x_{n-1}, \dots, x_2, x_1) \rightarrow (x_{n-1}, x_{n-2}, \dots, x_1, x_0).$$

Perfect shuffle is useful for fast Fourier transform (FFT), for various sorting procedures, for polynomial evaluation, etc.

A fairly popular permutation of the components of the binary vectors x and λ has the form $x \rightarrow x \bullet \lambda$, where $\bullet$ is “sum mod 2.” Like ideal shuffle, this permutation is used in FFT. An other useful permutation is “reversal” (reversing the sequence of bits in x) in the entire set E^n and in segments of length $2n-j$, i.e.,

$$x = (x_n, x_{n-1}, \dots, x_2, x_1) \rightarrow (x_1, x_2, \dots, x_{n-1}, x_n).$$

Reversal is also used in FFT. Various segment shuffles are also among the frequently used permutations.

“One-to-many” transfers (with “one-to-all” as a particular case) are common in solving systems of differential equations, both ordinary and partial. Such transfers are usually called nonordinal.

The finite element method (for solving the equations of mathematical physics) and logic circuit modeling use irregular (arbitrary) permutations.

MULTISTAGE SWITCHING NETWORKS WITH BLOCKING

Multistage switching networks for SIMD computers can be provided into two main categories: blocking networks, in which certain permutations may lead to collision, and nonblocking networks. For blocking networks we obviously have $C < 1$, while for nonblocking networks $C = 1$.

Note that blocking networks for SIMD computers usually allow self-routing or distributed control, while nonblocking networking require centralized control, and the setup of such networks is very time consuming. This accounts for the considerable “popularity” of blocking networks in SIMD computers.

Typical representatives of blocking networks are the omega network and the n-cube network. An 8 x 8-omega network is shown in Fig. 2. Each stage in this network implements the interconnections by the perfect shuffle scheme. This network is defined by two functions: the shuffle function and the exchange function. The shuffle function is

$$\text{Shuffle}(g_{n-1}g_{n-2}\dots g_1g_0) = g_{n-2}g_{n-3}\dots g_1g_0g_{n-1}. \quad (1)$$

The exchange function is defined as

$$\text{Exch}(g_{n-1}g_{n-2}\dots g_1g_0) = g_{n-1}g_{n-2}\dots g_1g_0. \quad (2)$$

The $N \times N$ omega network consists of $n = \log_2 N$ identical stages. The network may be realized as “one-to-one” or “one-to-many” interconnections. The control is by tags. The binary representation of the address of the output w to which the input v is to be connected is called the destination tag

$w = w_{n-1}w_{n-2}\dots w_1w_0$, and the binary representation of the input $v = v_{n-1}v_{n-2}\dots v_1v_0$, is called the source tag. When routing the network starting with the input v , the first switch connected with v is switched to the upper output if $w_{n-1} = 0$, and to the lower output if $w_{n-1} = 1$. The same occurs in the subsequent stages, i.e., the switching in stage i is controlled by w_i . Figure 2 shows how the second input is connected with the sixth output by this

algorithm. The omega network does not realize all the permutations without collision. Thus, we see in Fig. 2 that a collision in second-stage interconnections will occur when we attempt to connect simultaneously the zeroth input with the zeroth output and the fourth input with the second output.

There are omega network implementations using elements with more than two switchable channels. To establish the interconnections in this case, a cyclic left shift by one position is applied to the terminal address representation in a system with the base equal to the number of switching element inputs. The network control algorithm is similarly modified, i.e., the switching elements in each stage are controlled by the corresponding digit of the destination tag represented in a system with the chosen base.

The n-cube network belongs to the same class as the omega network. It derives its names from its geometrical interpretation as a n-dimensional cube whose vertices are the processor address in binary representation. In what follows, we will call this network simply a cube. An 8×8 cube network is shown in Fig. 3. The synthesis algorithm for the cube network is quite simple. If the upper and lower outputs for each switch have the same addresses as the upper and lower inputs, then the i-th stage pairs on the switch inputs those input lines whose addresses differ only in the i-th position (in the binary representations if the terminal addressed). Functionally, the cube is equivalent to the omega network, i.e., it realizes without collision the same classes of permutations and has the same control algorithm.

For a network with $N = 2^n$ inputs and binary representation of the input address in the form $g_{n-1}g_{n-2} \dots g_1g_0$, the cube network may be regarded as consisting of n functions:

$$Cube_i(g_{n-1} \dots g_{i+1}g_i g_{i-1} \dots g_0) = g_{n-1} \dots g_{i-1} \bar{g}_i g_{i-1} \dots g_0.$$

Cube and omega are essentially topological modifications of the same network. The same class of networks also includes the so-called indirect cube (the full name is “indirect binary n-cube”). In the direct cube network, the sequence of stages is reversed compared to the indirect cube (Fig. 4). The indirect cube is functionally equivalent to the direct cube with all the input and output addresses transformed from $g_{n-1} \dots g_1 g_0$ to $g_0 g_1 \dots g_{n-1}$.

The indirect cube is useful for PE-to-PE switching (Fig. 1a), because the hardware implementation of a growing processor array and its division into subarrays is simpler here than omega network, say.

From the list of frequently used permutations described above, the cube network and its modifications realize without collisions all the arbitrary shifts, including shifts within segments, and the permutations of the form $x \rightarrow x \bullet \lambda$, but neither ideal shuffle nor reversal can be realized in one pass through the network, i.e., these networks fail, in particular, for permutations that are useful for efficient FFT algorithms.

Banyan networks are topologically equivalent to cube networks. However, Banyan networks differ from the cube and its modifications by their use of the switching elements, which have six, and not four, admissible states (we are referring to 2×2 switching elements).

A fundamental property of the different networks considered above is that they all lay a unique path from each input to each output. This produces “intersecting” routes and may cause collisions in the network.

Another type of a blocking network is PM2I (Plus-Minus 2^i). An example of a PM2I network is the data manipulator. This network consists of n stages with N switches each, and the switch j in stage I is connected to three switches in stage $I - 1$; specifically: to the switch $(j + 2^i) \bmod N$, to the switch $(j - 2^i)$

$\text{mod } N$, and to the switch j , where $0 \leq j < N$ and $0 \leq I < n$. Note that in this context a stage is a column of switching elements together with all their outgoing connections (Fig.5). Unlike the networks considered above, PM2I uses 3×3 switches, and data can be transmitted at any given time only from one input to any of the three outputs. Different control techniques have been proposed for such a network. A network with individual control of the switching elements has been termed augmented data manipulator (ADM). It can be shown that the ADM is functionally superior to the previously considered networks. Thus, the ADM can realize all the permutations realized by omega plus some additional permutations not realized by omega, such as perfect shuffle. In other words, the ADM will execute without blocking a greater number of permutations than either the cube or the omega, but still it will not execute all $N!$ possible permutations. The price of the greater functional capabilities is higher hardware cost and more complex control than in the omega network.

There are also data manipulator modifications using two-input elements, which are topologically equivalent to omega, cube, and other networks.

Switching networks of this class are used in a number of currently available and projected computers, such as STARAN, Ultracomputer, RVAP (Reconfigurable Varistructured Array Processor), PASM (Partitionable SIMD/MIMD – a Purdue University project), the IBM RP3, some military systems, and data flow machines.

An interesting approach to switching was proposed by Burroughs for the NASF system. NASF (Numerical Aerodynamics Simulation Facility) is being developed under contract to NASA, and its main purpose is to solve aerodynamic problems during spacecraft design. Analysis has shown that an average problem in this field requires speeds of an order of 1 billion floating-point operations per second. In the NASF architecture, Burroughs proposes to solve the access problem by means of a certain compromise between Lawrie's system and the BSP solution. (See above) The facility will consist of 512

processors, a shared memory field using a prime number of memory modules greater than the number of processors, and a pair of 1024 x 1024 omega switching networks (“upper” and “lower”). Each processor thus can be connected to two ports (one by the upper network and one by the lower network). The access priorities on the upper network are the reverse of the lower-network priorities. If the upper network blocks access to memory, and automatic attempt is made to switch through the lower network.

Thus, the choice of a particular blocking network for SIMD computers is determined by the need to ensure collision-free transfers on some classes of frequently used permutations in the specific problem-oriented multiprocessor system.

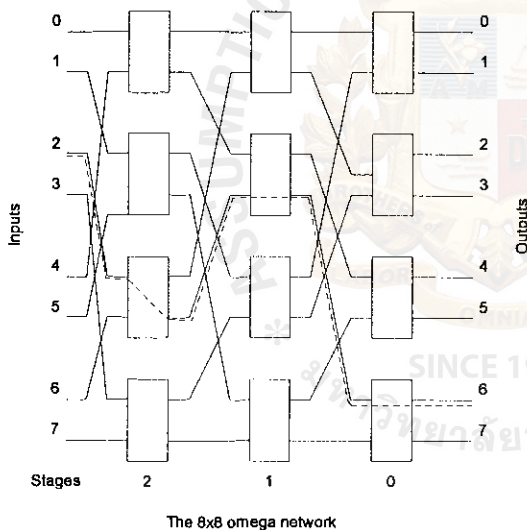


Fig. 2

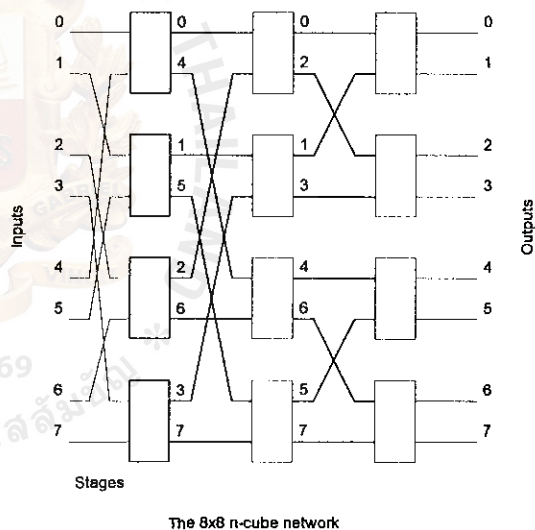
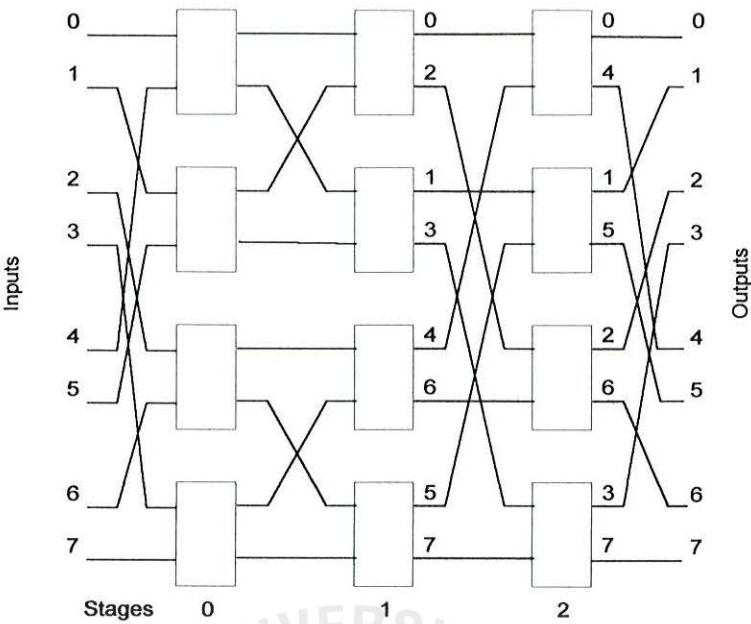
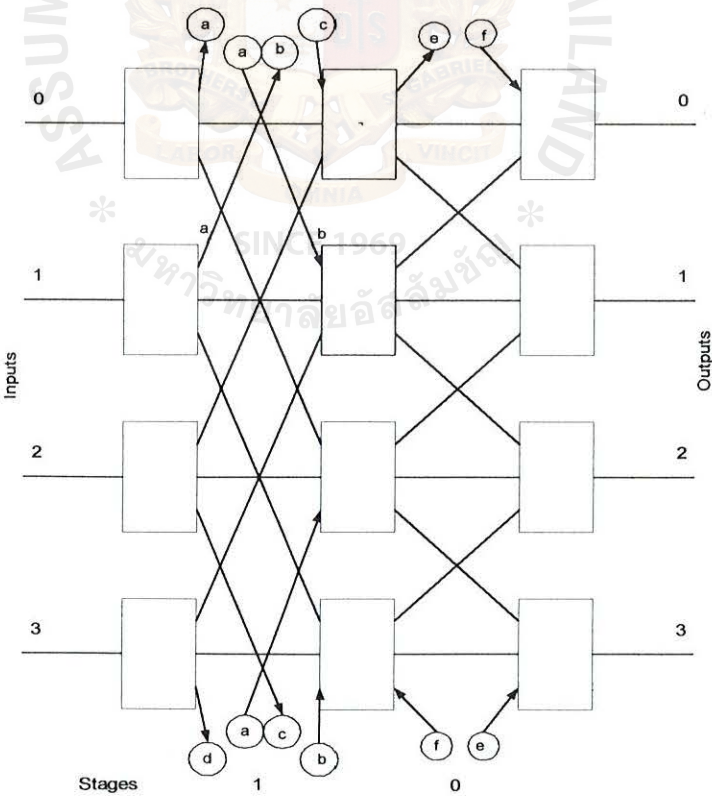


Fig. 3



The 8 x 8 indirect cube network

Fig. 4



The 4 x 4 data manipulator network

Fig. 5

THE BENES NETWORK AND ITS MODIFICATIONS

A second class of multistage switching networks that are of considerable practical interest are the so-called Clos-Benes nonblocking network representing a fairly wide class of network topologies. The objective was to develop a multistage network-realizing crossbar switching functions, i.e., no blocking, yet having fewer connection points than in crossbar networks. We should especially note the considerable contribution of Soviet scientists, in particular, Kharkevich and Neiman, to the theory of nonblocking switching networks.

Below we consider some networks contained in the class of networks studied by C. Clos and V. Benes. These networks consist of square subnetworks, and are thus of particular interest in computer systems.

Let $N = dq$, where d and q are integers. Then the $N \times N$ Clos network is represented by three stages (Fig. 6). The input and output stages contain N/d $d \times d$ subnetworks each (one of the input stage subnetworks can be eliminated – in Fig. 6 this subnetwork is enclosed in a broken box). The intermediate stage consists of d identical $N/d \times N/d$ subnetworks. Such a network is usually termed as a base- d network.

Such networks are fairly efficient in terms of hardware costs and are known in the literature as “rearrangeable,” because in case of blocking there is always a possibility of realizing the desired connection by rearranging (“rerouting”) some of the previously established connections. For these networks, there are algorithms for collision free realization of arbitrary permutations with simultaneous establishment of all the specified connections in the network. This is typical of the class of synchronous systems, which includes the SIMD computer systems as a particular case. Thus, for rearrangeable networks $C = 1$.

The network in Fig. 6 has an iterative structure, and for $d = 2$ successive decomposition of the middle stage into three-stage structures produces a network implemented using only two-input elements. The network constructed in such a way is usually called Benes network. Figure 7 is a base-2 8×8 network. With $N = 2^n$ inputs, the Benes network has $2 \log_2 N - 1$ stages. Its main shortcoming as compared with cube networks is the need for centralized control; moreover, it uses a complex and essentially sequential algorithm in order to compute the collection of signals controlling subnetwork switching (the “control vector” in what follows) during the realization of an arbitrary permutation.

We will now describe the so-called looping algorithm, which is basic for intersection control in Benes networks. Assume that the Benes network shown in Fig. 7 is required to realize the permutation p : $0 \rightarrow 3, 1 \rightarrow 7, 2 \rightarrow 4, 3 \rightarrow 0, 4 \rightarrow 2, 5 \rightarrow 6, 6 \rightarrow 1, 7 \rightarrow 5$, which is usually represented in the compact form the

$$p = \begin{array}{cccccccc} 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 \\ 3 & 7 & 4 & 0 & 2 & 6 & 1 & 5 \end{array}$$

First, this permutation should be described as an interconnection map (Fig. 8). The pair of network inputs that belong to the same switching element of the output stage defines the row address and the pair of network inputs that belong to the same switching element of the input stage defines the column address. Crosses in the corresponding positions mark pairs of input-output connections of the given permutation. Then the input into the map is chosen arbitrarily. For example, choosing as the starting point the “cross” (we call it the “input” in what follows) in rows 23 and column 01, we look for the next input in the same row or in the same column so as to form a loop. In Fig. 8, the input row 23 and column 45 is chosen. The process is continued until no loop can be formed because we return to row

23 and column 01. The loop inputs are then alternately named a and b. A second loop is formed similarly. Then the input and output lines names a are assigned to the subnetwork a, while the line name b are assigned to the subnetwork b. The resulting control of the input and output switching elements is shown in Fig. 9.

Using the given permutation and the established connections in the input and output stages, we can easily identify the permutations that should be realized by the subnetworks a and b. Then the looping algorithm is recursively applied to both subnetworks.

Such algorithm run in time $O(N \log_2 N)$. These time requirements to compute the control vector are obviously very large and may be totally unacceptable in some cases. To avoid this difficulty, we can compute the control vectors in advance (e.g., in the compiling stage) and store them in a "control vector table." Such tables take up a lot of memory space – not less than $(2 \log_2 N - 1) N/2$ bits per control vector for one permutation.

Another possibility is to focus on the frequently used permutations in the classification introduced above. The number of frequently used permutations is of order of $2^{2 \log_2 N}$, which is quite small compared with the total number of all permutations $N!$. Therefore, the permutation name can be encoded within the limits of the parameter field of the instruction "Start a frequently used permutation." On-line recursive algorithms have been proposed for such regular permutations, in which the times to compute a control vector does not introduce a noticeable delay into switching network operation. Arbitrary permutations, which are fairly noticeable delay into switching network operation. Arbitrary permutations, which are fairly infrequent in applications, should be realized by one of the general algorithms.

Of considerable interest is the switching network solution adopted in the Phoenix system. The final configuration of this system will consist of 1040 processors combined into groups of 65 (one standby processor in each group), ensuring a maximum speed of over 10 billion floating-point operations per second (GFLOP). One of the major innovations in system architecture adopted in this project is the decision to use a switching network that allows any possible interconnection of processors. A modified Benes network is proposed for this purpose. The advantage of this modification is that the distribution processors can be spatially divided into groups of close processors together with the associated switching network elements interconnected by close links (Fig. 10). If the central stages are connected "straight," the network is partitionable into independent local subnetworks.

Another example of a rearrangeable switching network is used in the GF-11 supercomputer. It consists of 576 processors and ensures speeds of up to 11 GFLOP. A nonblocking rearrangeable three-stage network interconnects the processors. Each stage in this network consists of 24 switching elements of 24×24 each.

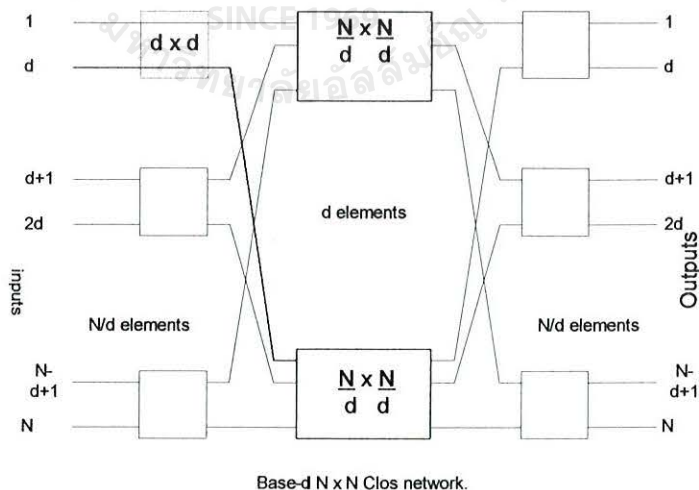


Fig. 6

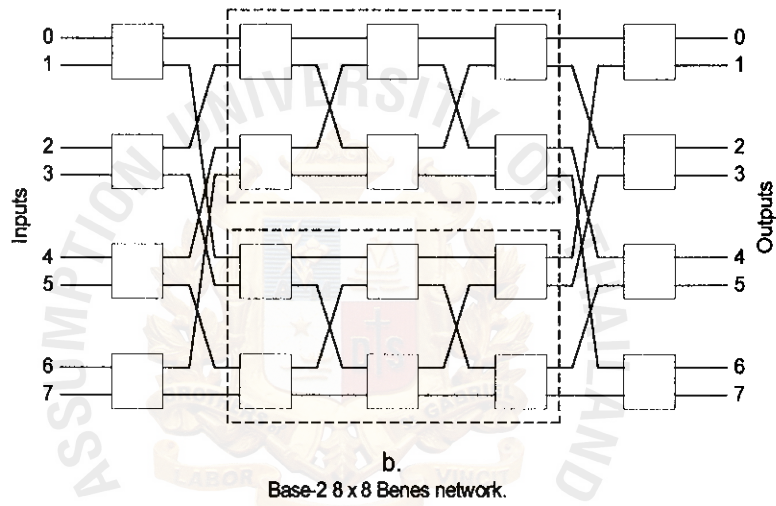
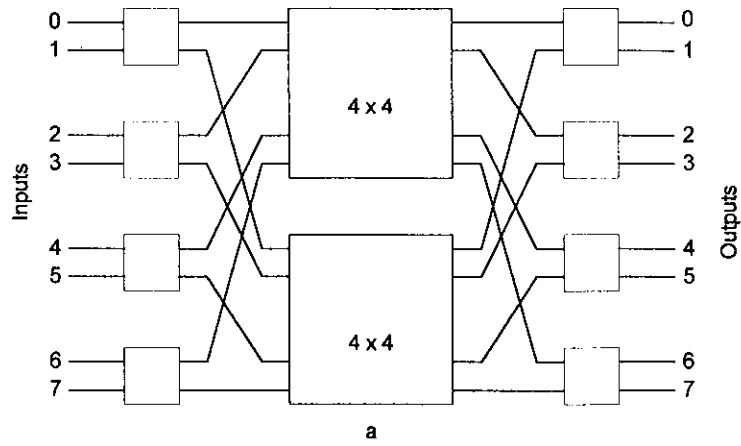


Fig. 7

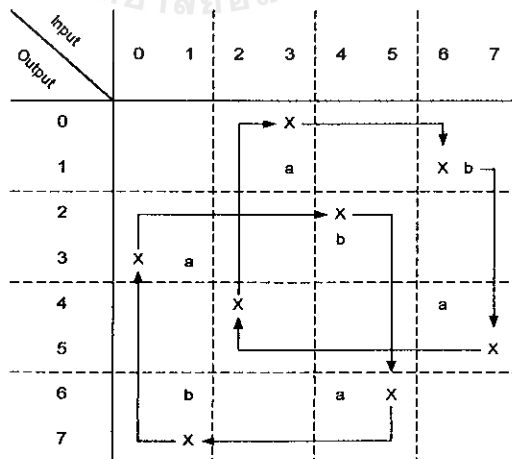


Fig. 8

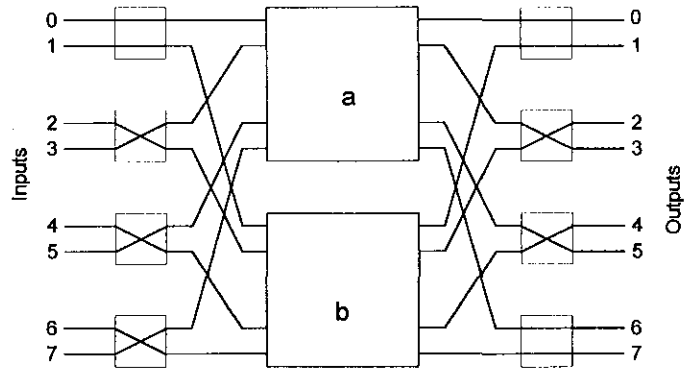
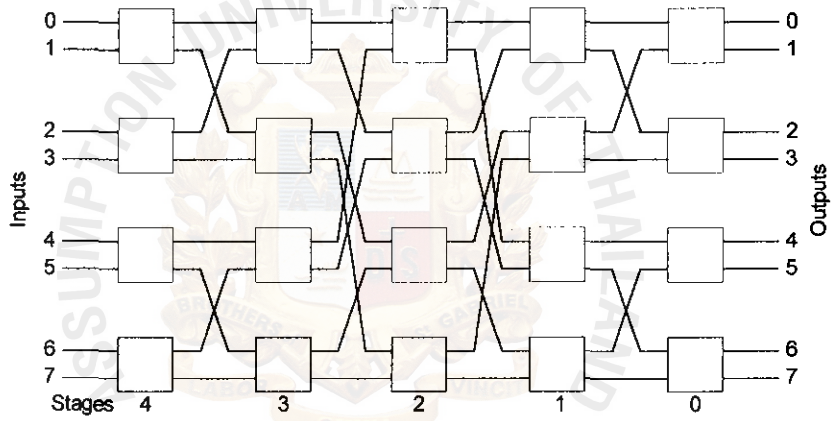


Fig. 9



A modified 8 x 8 Benes network partitionable into local subnetworks.

Fig. 10

FAULT-TOLERANT SWITCHING NETWORKS

The examples of switching networks considered above show that with a large number of processors (hundreds and thousands) these networks are fairly complex devices. The switching control algorithms are also fairly complex, especially for Benes networks. Since the reliability of a switching network has a direct impact on the reliability of the entire system, reliability improvement can be achieved by designing networks that are fault-tolerant with respect to (usually) single faults. The problems of design of a fault-tolerant network are formulated as follows.

1. For single faults in switching elements and their interconnections, the network should realize without collision the original classes of admissible permutations.
2. A fault-tolerant network should have a sufficiently simple algorithm that will rearrange it in case of a fault.
3. Network control should be capable of partitioning the network into subnetworks of equal size, coupled both electrically and structurally. The last requirement makes it possible to disconnect the faulty half of the network for repair, while the nonfaulty half continues functioning, emulating the complete switching network with performance reduced by a factor of 4.

Fault-tolerance implies neutralization of the effect of faults in the network. This is possible only if we provide static redundancy, e.g., masking in a three-fold majority-voting structure, or dynamic redundancy, which pinpoints the fault and reconfigures the network or the data flows. In what follows, we consider dynamic redundancy techniques.

The data transmitted in a single clock cycle through the switching network may be one bit, one byte, or one processor word. In the last two cases, faults may be detected by appending a parity bit or several bits in the Hamming code. However, these methods, while signaling the existence of a fault, do not pinpoint the fault location in the switching network. It is better to use for this purpose special diagnostic tests which are run periodically as part of network testing or after a fault has been detected.

Simple and efficient diagnostic tests are available for the class of single stuck-at faults $\text{const} \equiv 1$ (or $\equiv 0$) on one of the information inputs (outputs) or on the control input of the switching element in a base-2 switching network. The main idea of these tests is the following. Apply an input combination to the N network inputs such that each switching element receives the signal 01 or 10 on its two inputs, with the same control signal on all the elements. As all the input values are inverted in a nonfaulty network, each output terminal should successively procedure the two values 01 and 10. If this sequence is not observed on one of the output terminals, there is a fault in the information channel connected with this terminal. Repeating the same test for inverted values of the control signal on each switching element, we may detect another information channel passing through the same faulty component. The fault is in the component, which is common to both information channels.

These tests are similarly applied to check for control signal faults. An error in the output signal is detected by comparing the output values with a reference. A reference signal is needed because if there is a fault in the control signal of the switching elements in the last stage, a 1-out-of-2 code will not be violated on the network output terminals (unlike the case of such a fault in all the other stages), and the output therefore have to be tested by comparison with reference values.

All the above remains valid for cube and omega networks, their generalizations and also for Benes networks.

Thus, a base-2 switching network can be diagnosed by four test combinations, which identify the faulty switching element or the faulty component in the transmission channel.

The diagnostic results make it possible to move to the next stage of recovery in a faulty switching network – neutralizing the effect of the fault. Here two approaches are available. The first relies on the introduction of an extra stage in cube networks. Because of the extra stage, there are now two paths from any source to any destination in the switching network.

The second approach designs a switching network with a given constant number of nonintersecting routes from any source to the destination. For blocking network, the existence of alternative routes is ensured by a special choice of the switching element base in the network. Both approaches are considered in more detail below.

In the Benes network, there are more than one independent path for each input-output pair, so that in principle it is possible to bypass single faults and to realize any given permutation in two passes without extra stages. If the first and the last stages in the Benes network are augmented with multiplexors-demultiplexors (fig. 12), then the modified Benes network will be fault-tolerant to single faults. In this case, fault tolerance is also accomplished in two passes through the network. In the first pass, the data are switched through the nonfaulty paths, while in the second pass alternative paths switch the remaining connections. Because of the perfect symmetry of the two alternative path in the second pass by passing the control signals from the switching elements of one “storey” of intermediate stages to another “storey” (in Fig. 12, the “stories” are enclosed in broken boxes). The control signals are generated in advance for the given interconnection list by one of the known algorithms, assuming a nonfaulty network. The control for the switching elements of the first and the last stages participating in the unrealized connection is reversed, i.e.,

if one element was initially connected “straight”, it is now switched to “exchange,” and conversely.

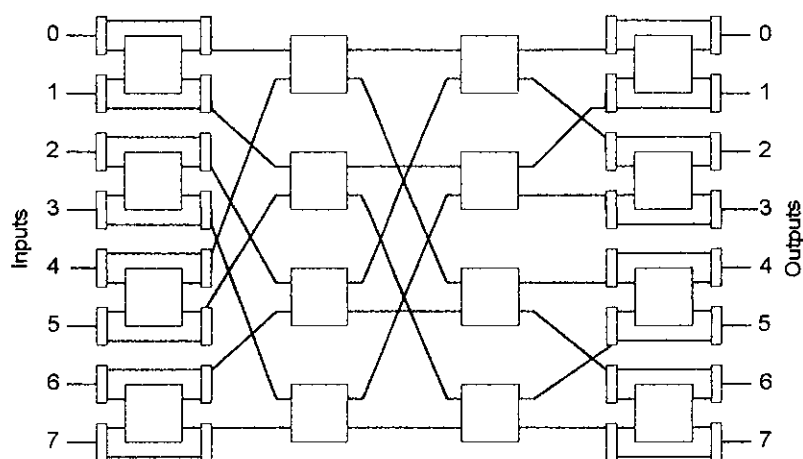
If the fault is detected in the first or the last stage, then the network control is somewhat different. Specifically, if the fault is detected in a switching element of the first (last) stage connected “straight,” then this element is disconnected, the bypass multiplexors-demultiplexors are activated, and the required switching can be realized even in a single pass, because all the other control signals are not altered. If the faulty element was realizing the exchange function (connected cross-cross), then the fault element, are switched in the first pass, and the bypass multiplexors-demultiplexors of the faulty element are activated in the second pass, when the control signals from the first “storey” of intermediate stages are transferred to the second “storey” and conversely, thus exciting two alternative paths relative to the initial paths in the faulty network.

Note that the modified Benes network (Fig. 10) allows decomposition of the entire network into two subnetworks of equal size, so that the nonfaulty half can emulate the entire network. This decomposition is useful during the recovery of the faulty half of the network.

The previously considered approach to fault-tolerance relies on explicitly appending an extra stage to the cube network in order to produce an additional route between any input-output pair. The alternative approach implicitly uses the redundant switching capabilities of the switching elements in order to achieve fault-tolerance of the network. These capabilities arise when fault-tolerant networks are designed using a base $W = 2^\gamma$ omega network, where γ is an integer greater than 1; the number of stages in the network is $\lceil \log_w N \rceil$, where $\lceil x \rceil$ is the nearest integer greater than x . A theorem is proved which claims that for a $N \times N$ uniform network of this kind, with $N = 2^n$. The number of different routes R between input-output pair is given by $R = W^{\lceil n/\gamma \rceil}$, where $\lceil x \rceil$ is the difference between the nearest integer

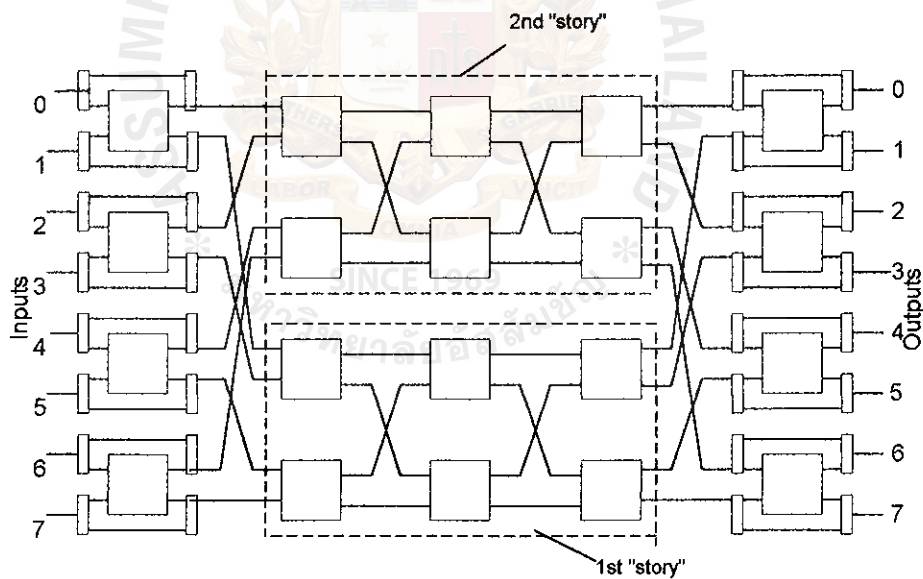
equal to or greater than the real number x and x . Note that N should be divisible by W , but for $N = W^t$ the modified omega reduces to an ordinary omega network, i.e., a network with a unique route for each input-output pair. Figure 15 shows a modified base-8 16×16 omega network. The network consists of two stages. In this case, $n = 4$, $\gamma = 3$, $N = 2^4 = 16$, $W = 2^3 = 8$, $\lceil n/\gamma \rceil = \lceil 4/3 \rceil = 2/3$, and therefore, $R = W^{\lceil n/\gamma \rceil} = 8^{2/3} = 8(2/3) = 4$. The existence of four possible routes for each input-output pair essentially improves the fault-tolerance of the network. Thus the network shown in Fig. 5 will realize the initial permutation in two passes in the presence of any two faults in the interconnections between the stages.





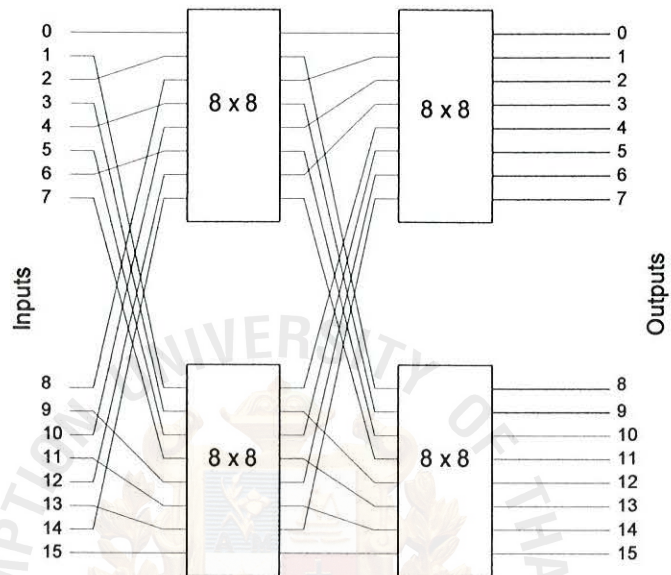
A fault-tolerant modification of the 8 x 8 Benes network.

Fig. 11



A fault-tolerant modification of the 8 x 8 Benes network.

Fig. 12



A fault-tolerant modification of the 16 x 16 omega network with four routes of each input-output pair.

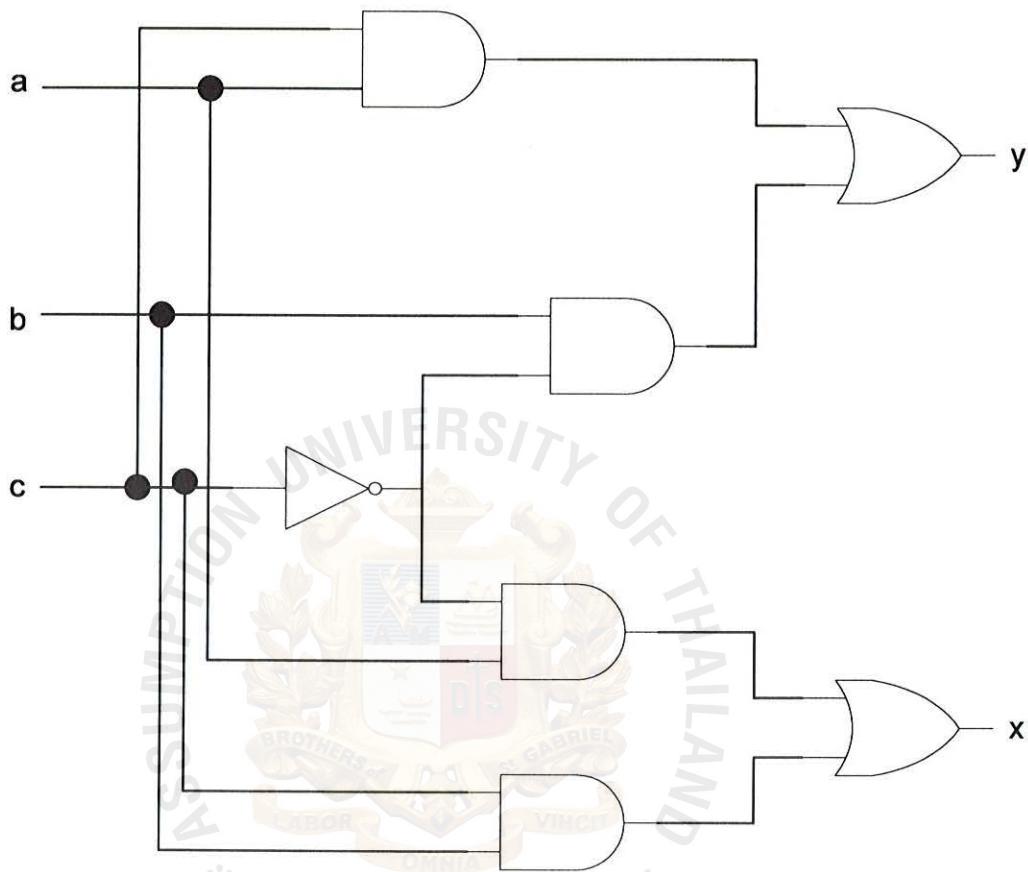
Fig. 13

CHAPTER 3 :

FABRICATION AND CONSTRUCTION

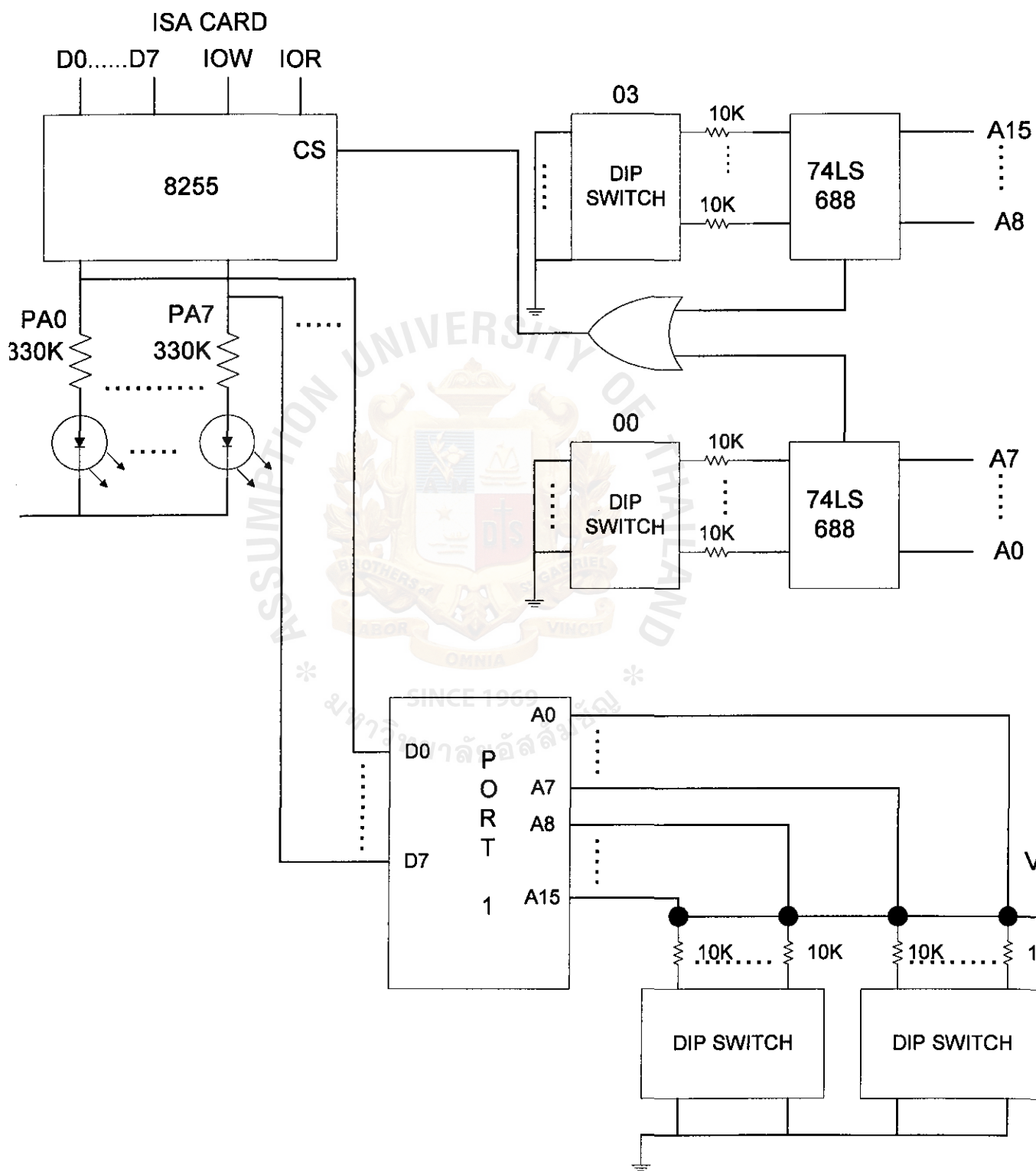


Circuit Diagram of the switch

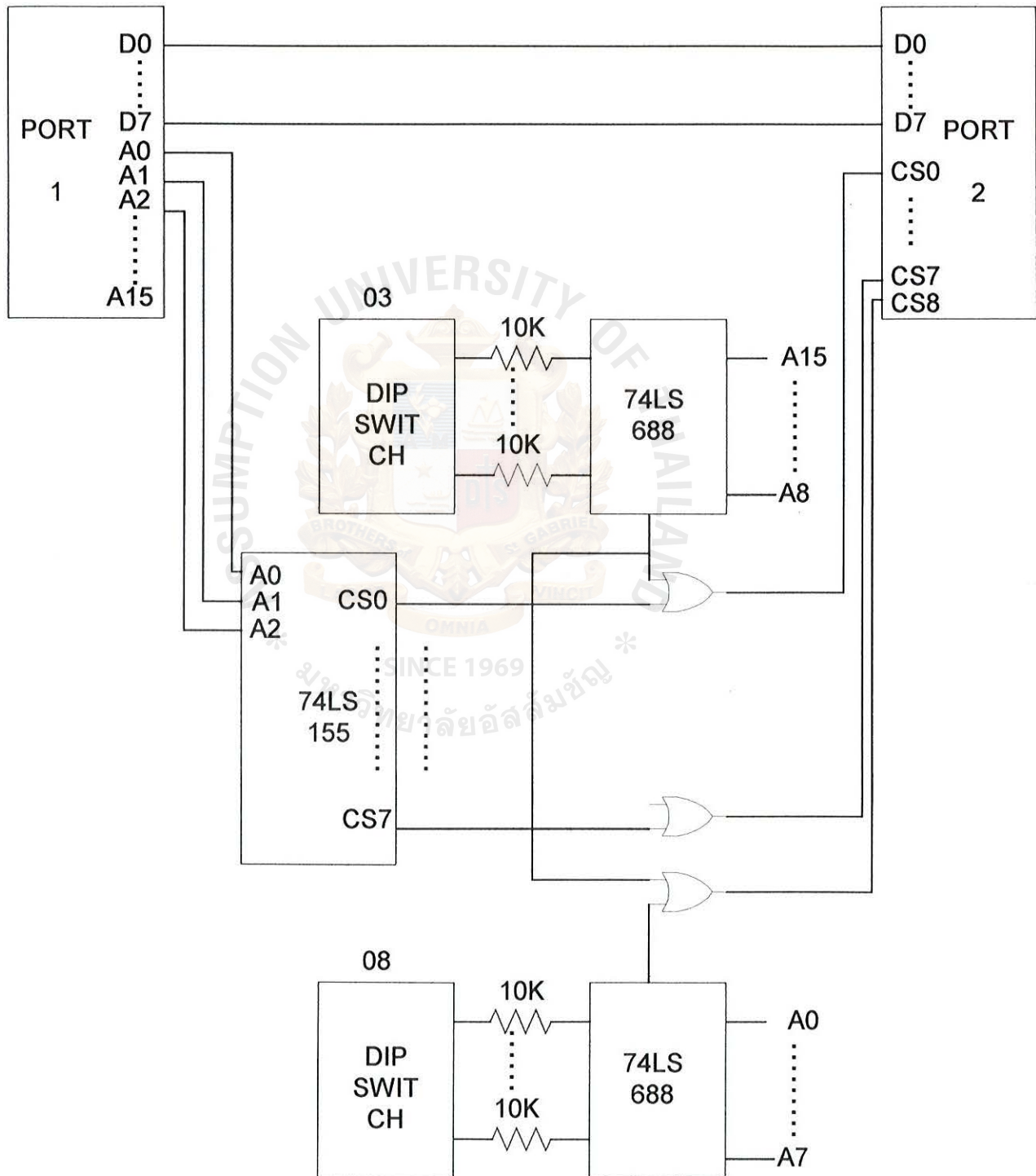


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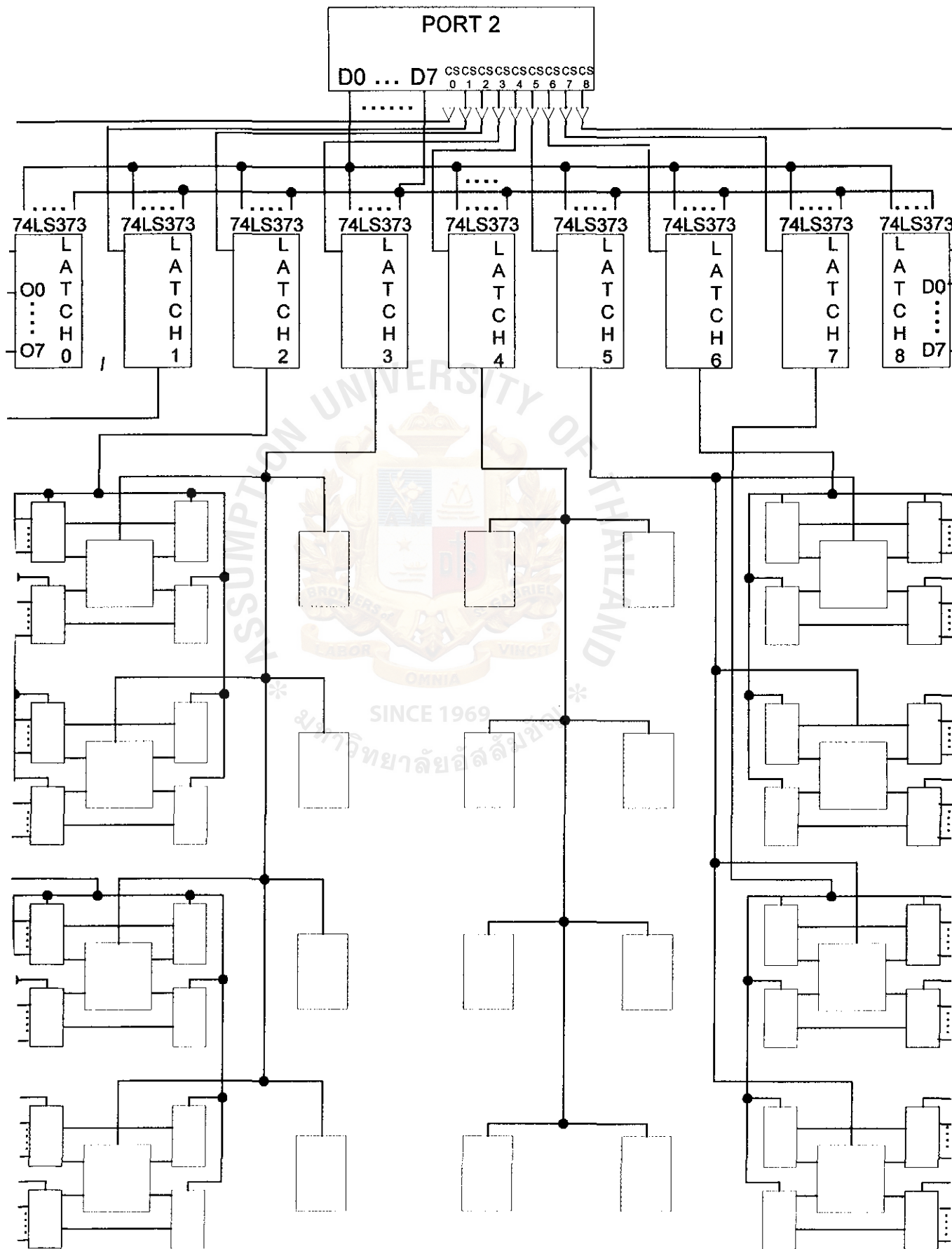
Circuit Diagram of the address decoder



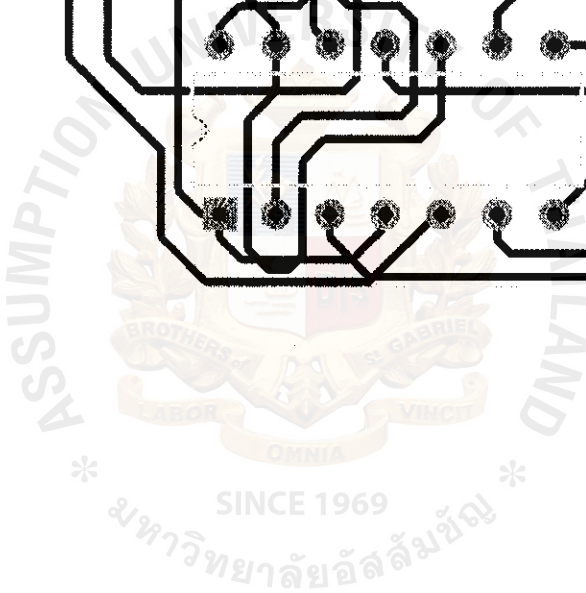
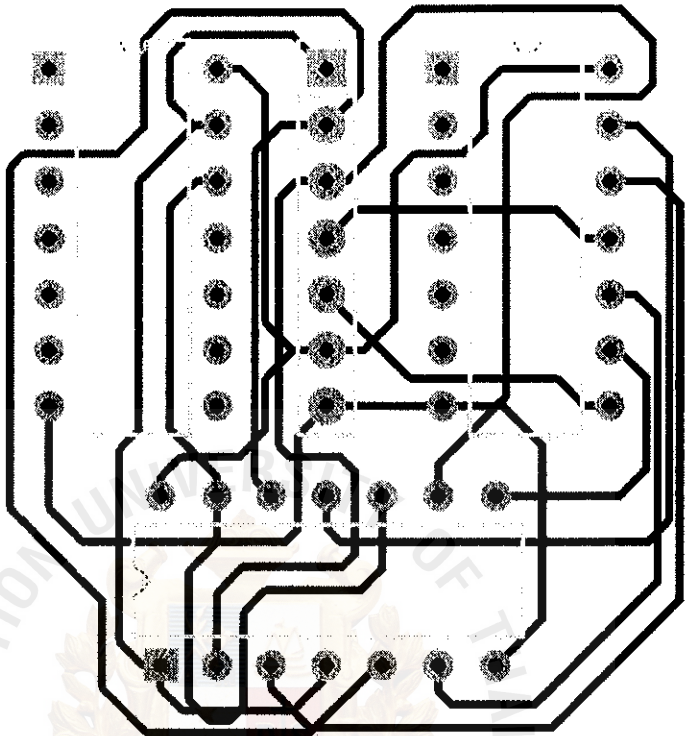
Circuit Diagram of the address decoder 2



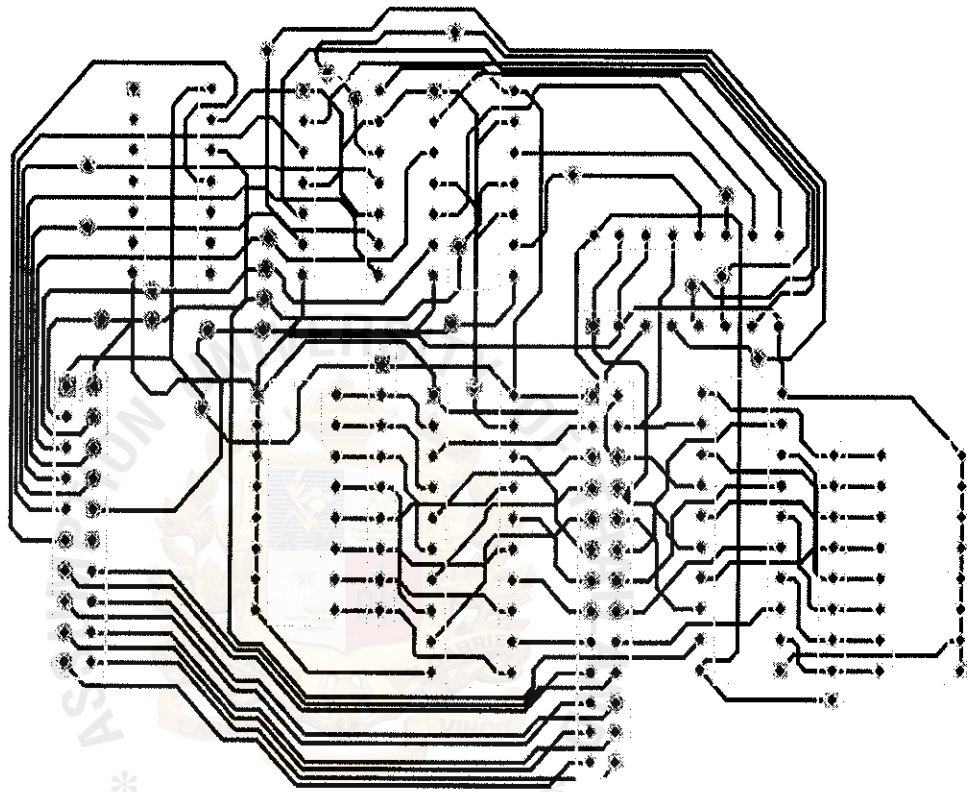
Circuit Diagram of the Benes Network



PCB design for switch

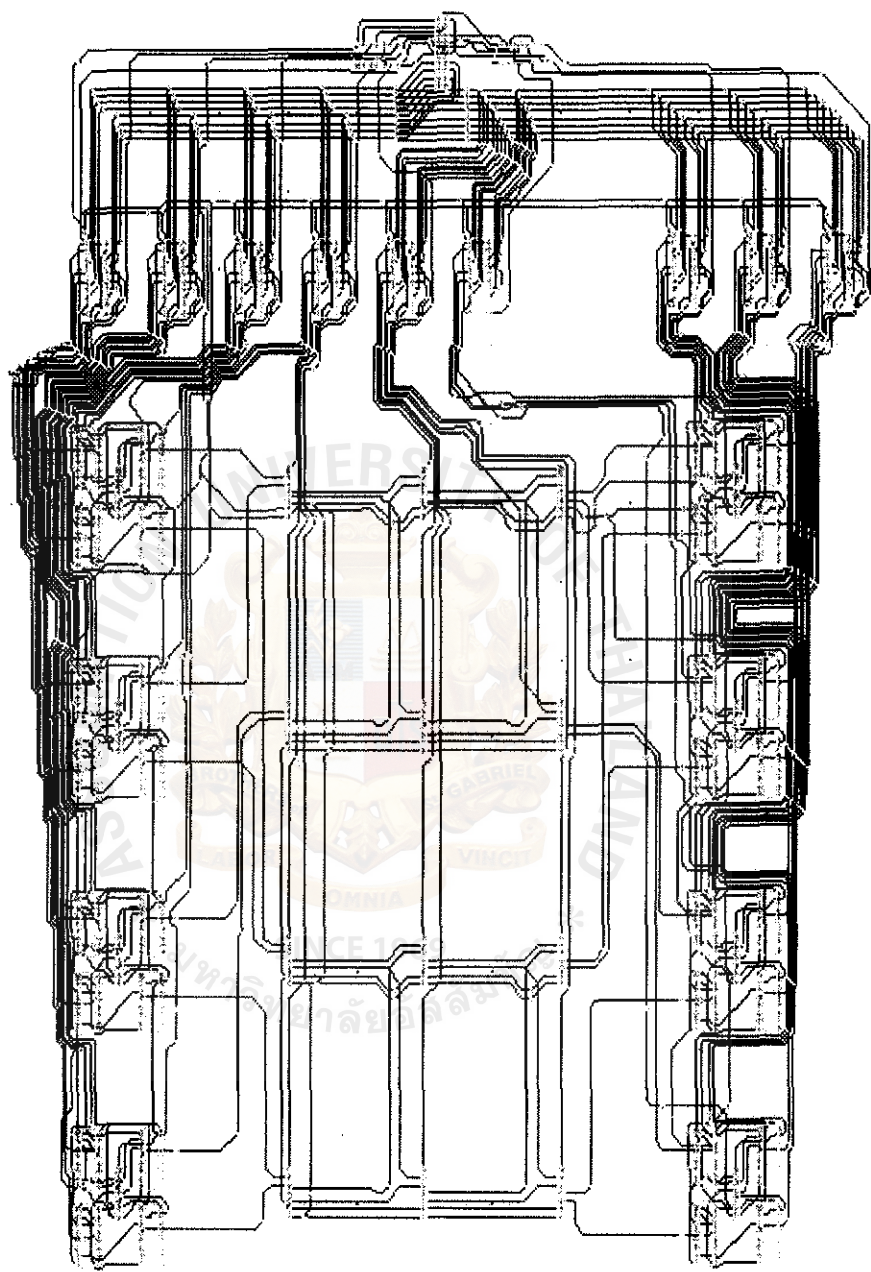


PCB design for address decoder



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PCB design for Benes Network



Outputs correspondence to inputs with chosen permutation requests

```
#include<stdio.h>
#include<conio.h>
#include<ctype.h>
void main(void)
{
    int m[21];
    int a[8],b[8];
    int a1=0,a2=0,a3=0,a4=0;
    int n;
    char high,low;
    clrscr();
    printf("*****\n");
    printf("***    1.Perfect Shuffle    **\n");
    printf("***    2.Bit Reverse      **\n");
    printf("***    3.Flip Permutation   **\n");
    printf("***    4.Cyclic Shift      **\n");
    printf("*****\n");
    printf("Please choose a number : ");
    scanf("%d",&n);

    if (n==1)
    { m[1]=0; m[5]=0; m[9]=0; m[13]=0; m[17]=0;
      m[2]=0; m[6]=1; m[10]=1; m[14]=1; m[18]=1;
      m[3]=1; m[7]=0; m[11]=0; m[15]=1; m[19]=0;
      m[4]=1; m[8]=1; m[12]=1; m[16]=0; m[20]=1;
    }
    if (n==2)
    { m[1]=0; m[5]=0; m[9]=0; m[13]=0; m[17]=0;
      m[2]=0; m[6]=0; m[10]=0; m[14]=0; m[18]=0;
      m[3]=1; m[7]=0; m[11]=1; m[15]=1; m[19]=1;
      m[4]=1; m[8]=1; m[12]=1; m[16]=0; m[20]=1;
    }
    if (n==3)
    {
        clrscr();
        printf("*****\n");
        printf("***    1. 101    **\n");
        printf("***    2. 011    **\n");
        printf("***    3. 010    **\n");
        printf("***    4. 111    **\n");
        printf("*****\n");
        printf("Please choose a number : ");
        scanf("%d",&n);

        if (n==1)
        { m[1]=1; m[5]=0; m[9]=1; m[13]=0; m[17]=0;
          m[2]=1; m[6]=0; m[10]=1; m[14]=0; m[18]=0;
          m[3]=1; m[7]=0; m[11]=1; m[15]=0; m[19]=0;
          m[4]=1; m[8]=0; m[12]=1; m[16]=0; m[20]=0;
        }
        if (n==2)
        { m[1]=0; m[5]=0; m[9]=0; m[13]=1; m[17]=1;
          m[2]=0; m[6]=0; m[10]=0; m[14]=1; m[18]=1;
          m[3]=0; m[7]=0; m[11]=0; m[15]=1; m[19]=1;
          m[4]=0; m[8]=0; m[12]=0; m[16]=1; m[20]=1;
        }
    }
}
```

```

if (n==3)
{ m[1]=0; m[5]=0; m[9]=0; m[13]=1; m[17]=0;
  m[2]=0; m[6]=0; m[10]=0; m[14]=1; m[18]=0;
  m[3]=0; m[7]=0; m[11]=0; m[15]=1; m[19]=0;
  m[4]=0; m[8]=0; m[12]=0; m[16]=1; m[20]=0;
}
if (n==4)
{ m[1]=0; m[5]=0; m[9]=1; m[13]=1; m[17]=1;
  m[2]=0; m[6]=0; m[10]=1; m[14]=1; m[18]=1;
  m[3]=0; m[7]=0; m[11]=1; m[15]=1; m[19]=1;
  m[4]=0; m[8]=0; m[12]=1; m[16]=1; m[20]=1;
}
}
if (n==4)
{ clrscr();
  printf("Please enter a number[1 , 2] : ");
  scanf("%d",&n);

  if (n==1)
  { m[1]=0; m[5]=0; m[9]=0; m[13]=0; m[17]=0;
    m[2]=0; m[6]=1; m[10]=1; m[14]=1; m[18]=1;
    m[3]=1; m[7]=0; m[11]=0; m[15]=1; m[19]=0;
    m[4]=1; m[8]=1; m[12]=1; m[16]=0; m[20]=1;
  }
  if (n==2)
  { m[1]=0; m[5]=0; m[9]=0; m[13]=0; m[17]=0;
    m[2]=1; m[6]=1; m[10]=1; m[14]=1; m[18]=0;
    m[3]=0; m[7]=1; m[11]=0; m[15]=0; m[19]=1;
    m[4]=1; m[8]=0; m[12]=1; m[16]=1; m[20]=1;
  }
}
clrscr();
printf("The controls are as shown below.\n\n");
printf(" %d %d %d %d %d \n",m[1],m[5],m[9],m[13],m[17]);
printf(" %d %d %d %d %d \n",m[2],m[6],m[10],m[14],m[18]);
printf(" %d %d %d %d %d \n",m[3],m[7],m[11],m[15],m[19]);
printf(" %d %d %d %d %d \n",m[4],m[8],m[12],m[16],m[20]);
printf("\nPlease enter the data.\n");
printf("\nThe higher 4 bits of data in HEX = ");
scanf("%c",&high);
scanf("%c",&high);
printf("The lower 4 bits of data in HEX = ");
scanf("%c",&low);
scanf("%c",&low);

if (high == '1')
a1 = 1;
else if (high == '2')
a2 = 1;
else if (high == '3')
{ a2 = 1; a1 = 1; }
else if (high == '4')
a3 = 1;
else if (high == '5')
{ a3 = 1; a1 = 1; }
else if (high == '6')
{ a2 = 1; a3 = 1; }
else if (high == '7')
{ a2 = 1; a1 = 1; a3 = 1; }
else if (high == '8')

```

```

a4 = 1;
else if (high == '9')
{ a1 = 1; a4 = 1; }
else if (high == 'A' || high == 'a')
{ a2 = 1; a4 = 1; }
else if (high == 'B' || high == 'b')
{ a2 = 1; a4 = 1; a1 = 1; }
else if (high == 'C' || high == 'c')
{ a3 = 1; a4 = 1; }
else if (high == 'D' || high == 'd')
{ a3 = 1; a4 = 1; a1 = 1; }
else if (high == 'E' || high == 'e')
{ a3 = 1; a4 = 1; a2 = 1; }
else if (high == 'F' || high == 'f')
{ a3 = 1; a4 = 1; a2 = 1; a1 = 1; }

a[1]=a1; a[2]=a2; a[3]=a3; a[4]=a4; a1 = 0; a2 = 0; a3 = 0; a4 = 0;
if (low == '1')
a1 = 1;
else if (low == '2')
a2 = 1;
else if (low == '3')
{ a2 = 1; a1 = 1; }
else if (low == '4')
a3 = 1;
else if (low == '5')
{ a3 = 1; a1 = 1; }
else if (low == '6')
{ a2 = 1; a3 = 1; }
else if (low == '7')
{ a2 = 1; a1 = 1; a3 = 1; }
else if (low == '8')
a4 = 1;
else if (low == '9')
{ a1 = 1; a4 = 1; }
else if (low == 'A' || low == 'a')
{ a2 = 1; a4 = 1; }
else if (low == 'B' || low == 'b')
{ a2 = 1; a4 = 1; a1 = 1; }
else if (low == 'C' || low == 'c')
{ a3 = 1; a4 = 1; }
else if (low == 'D' || low == 'd')
{ a3 = 1; a4 = 1; a1 = 1; }
else if (low == 'E' || low == 'e')
{ a3 = 1; a4 = 1; a2 = 1; }
else if (low == 'F' || low == 'f')
{ a3 = 1; a4 = 1; a2 = 1; a1 = 1; }

a[5]=a1; a[6]=a2; a[7]=a3; a[8]=a4;
if (m[1]==0)
{ b[1]=a[1];
  b[2]=a[2];
}
else
{ b[1]=a[2];
  b[2]=a[1];
}
if (m[2]==0)
{ b[3]=a[3];
  b[4]=a[4];
}

```

```

}
else
{ b[3]=a[4];
  b[4]=a[3];
}
if (m[3]==0)
{ b[5]=a[5];
  b[6]=a[6];
}
else
{ b[5]=a[6];
  b[6]=a[5];
}
if (m[4]==0)
{ b[7]=a[7];
  b[8]=a[8];
}
else
{ b[7]=a[8];
  b[8]=a[7];
}
a[1]=b[1]; a[2]=b[3]; a[3]=b[5]; a[4]=b[7];
a[5]=b[2]; a[6]=b[4]; a[7]=b[6]; a[8]=b[8];
m[1]=m[5]; m[2]=m[6]; m[3]=m[7]; m[4]=m[8];
if (m[1]==0)
{ b[1]=a[1];
  b[2]=a[2];
}
else
{ b[1]=a[2];
  b[2]=a[1];
}
if (m[2]==0)
{ b[3]=a[3];
  b[4]=a[4];
}
else
{ b[3]=a[4];
  b[4]=a[3];
}
if (m[3]==0)
{ b[5]=a[5];
  b[6]=a[6];
}
else
{ b[5]=a[6];
  b[6]=a[5];
}
if (m[4]==0)
{ b[7]=a[7];
  b[8]=a[8];
}
else
{ b[7]=a[8];
  b[8]=a[7];
}

a[1]=b[1]; a[2]=b[3]; a[3]=b[2]; a[4]=b[4];
a[5]=b[5]; a[6]=b[7]; a[7]=b[6]; a[8]=b[8];

```

```

m[1]=m[9]; m[2]=m[10]; m[3]=m[11]; m[4]=m[12];
if (m[1]==0)
{ b[1]=a[1];
  b[2]=a[2];
}
else
{ b[1]=a[2];
  b[2]=a[1];
}
if (m[2]==0)
{ b[3]=a[3];
  b[4]=a[4];
}
else
{ b[3]=a[4];
  b[4]=a[3];
}
if (m[3]==0)
{ b[5]=a[5];
  b[6]=a[6];
}
else
{ b[5]=a[6];
  b[6]=a[5];
}
if (m[4]==0)
{ b[7]=a[7];
  b[8]=a[8];
}
else
{ b[7]=a[8];
  b[8]=a[7];
}
a[1]=b[1]; a[2]=b[3]; a[3]=b[2]; a[4]=b[4];
a[5]=b[5]; a[6]=b[7]; a[7]=b[6]; a[8]=b[8];
m[1]=m[13]; m[2]=m[14]; m[3]=m[15]; m[4]=m[16];
if (m[1]==0)
{ b[1]=a[1];
  b[2]=a[2];
}
else
{ b[1]=a[2];
  b[2]=a[1];
}
if (m[2]==0)
{ b[3]=a[3];
  b[4]=a[4];
}
else
{ b[3]=a[4];
  b[4]=a[3];
}
if (m[3]==0)
{ b[5]=a[5];
  b[6]=a[6];
}
else
{ b[5]=a[6];
  b[6]=a[5];
}

```

```

if (m[4]==0)
{ b[7]=a[7];
  b[8]=a[8];
}
else
{ b[7]=a[8];
  b[8]=a[7];
}
a[1]=b[1]; a[2]=b[5]; a[3]=b[2]; a[4]=b[6];
a[5]=b[3]; a[6]=b[7]; a[7]=b[4]; a[8]=b[8];
m[1]=m[17]; m[2]=m[18]; m[3]=m[19]; m[4]=m[20];
if (m[1]==0)
{ b[1]=a[1];
  b[2]=a[2];
}
else
{ b[1]=a[2];
  b[2]=a[1];
}
if (m[2]==0)
{ b[3]=a[3];
  b[4]=a[4];
}
else
{ b[3]=a[4];
  b[4]=a[3];
}
if (m[3]==0)
{ b[5]=a[5];
  b[6]=a[6];
}
else
{ b[5]=a[6];
  b[6]=a[5];
}
if (m[4]==0)
{ b[7]=a[7];
  b[8]=a[8];
}
else
{ b[7]=a[8];
  b[8]=a[7];
}
printf("\nThe output data is %d%d%d%d%d%d%d%d.",b[8],b[7],b[6],b[5],b[4],b[3],b[2],b[1]);
getch();
}

```

```
#include<stdio.h>
#include<conio.h>
#include<ctype.h>
void main(void)
{
    int a[9],b[9];
    int i,c,d;
    clrscr();
    printf("The data of the first pass.\n");
    for (i=7;i>=1;i--)
    {
        printf("D%d= ",i);
        scanf("%d",&a[i+1]);
    }
    printf("\nThe data of the second pass.\n");
    for (i=7;i>=1;i--)
    {
        printf("D%d= ",i);
        scanf("%d",&b[i+1]);
    }
    printf("\nThe first error bit = ");
    scanf("%d",&c);
    printf("\nThe second error bit = ");
    scanf("%d",&d);
    c++;
    d++;
    a[c]=b[c];
    a[d]=b[d];

    printf("\nThe correct output is %d%d%d%d%d%d%d%d.",a[8],a[7],a[6],a[5],a[4],a[3],a[2],a[1]);
    getch();
}
```

the first set of the
the second set of
the third set of the
the third set of the
the forth set of the
the data inputs.\$'
g the data to
match the data
d by 1 position.\$'
d by 2

the first set of the
the second set of
the third set of the
the third set of the
the forth set of the
the data inputs.\$'
g the data to
match the data

the first set of the
the second set of
the third set of the
the third set of the
the forth set of the
the data inputs.\$'
g the data to
match the data
d by 1 position.\$'
d by 2

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```
LEA DX,MSG2
MOV AH,9
```


[illegible]

```
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG3
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,89H
MOV DX,0303H
OUT DX,AL

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
```

INT 21H
LEA DX,MSG4
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG5
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,10101100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,01101010B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9

INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00001010B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG9
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG11
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9

INT 21H
LEA DX,MSG10
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,DAT
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG12
MOV AH,9
INT 21H

MOV AH,1
INT 21H
JMP EXIT

BI: LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG3
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,89H
MOV DX,0303H
OUT DX,AL

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG4
MOV AH,9

INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG5
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,10001100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,01001100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9

INT 21H
 MOV AH,1
 INT 21H

 MOV AL,00001100B
 MOV DX,0300H
 OUT DX,AL

LEA DX,CLRF
 MOV AH,9
 INT 21H

LEA DX,MSG13
 MOV AH,9
 INT 21H
 LEA DX,CLRF
 MOV AH,9
 INT 21H
 LEA DX,MSG8
 MOV AH,9
 INT 21H
 MOV AH,1
 INT 21H

MOV AL,00110011B
 MOV DX,0300H
 OUT DX,AL

LEA DX,CLRF
 MOV AH,9
 INT 21H

LEA DX,MSG13
 MOV AH,9
 INT 21H
 LEA DX,CLRF
 MOV AH,9
 INT 21H
 LEA DX,MSG9
 MOV AH,9
 INT 21H
 MOV AH,1
 INT 21H

MOV AL,00110011B
 MOV DX,0300H
 OUT DX,AL

LEA DX,CLRF
 MOV AH,9
 INT 21H

LEA DX,MSG11
 MOV AH,9
 INT 21H
 LEA DX,CLRF
 MOV AH,9
 INT 21H
 LEA DX,MSG10
 MOV AH,9

INT 21H
 MOV AH,1
 INT 21H

 MOV AL,DAT
 MOV DX,0300H
 OUT DX,AL

LEA DX,CLRF
 MOV AH,9
 INT 21H

LEA DX,MSG12
 MOV AH,9
 INT 21H

MOV AH,1
 INT 21H
 JMP EXIT

FL: LEA DX,CLRF
 MOV AH,9
 INT 21H
 LEA DX,MSG14
 MOV AH,9
 INT 21H
 LEA DX,CLRF
 MOV AH,9
 INT 21H
 LEA DX,MSG15
 MOV AH,9
 INT 21H
 LEA DX,CLRF
 MOV AH,9
 INT 21H
 LEA DX,MSG16
 MOV AH,9
 INT 21H
 LEA DX,CLRF
 MOV AH,9
 INT 21H
 LEA DX,MSG17
 MOV AH,9
 INT 21H
 LEA DX,CLRF
 MOV AH,9
 INT 21H
 LEA DX,CLRF
 MOV AH,9
 INT 21H
 LEA DX,MSG1
 MOV AH,9
 INT 21H
 MOV AH,1
 INT 21H

 CMP AL,31H
 JE F1
 CMP AL,32H

JE F22	MOV AH,9
CMP AL,33H	INT 21H
JE F33	LEA DX,CLRF
CMP AL,34H	MOV AH,9
JE F44	INT 21H
JMP EXIT	LEA DX,MSG5
	MOV AH,9
F22: JMP F2	INT 21H
F33: JMP F3	MOV AH,1
F44: JMP F4	INT 21H
F1: LEA DX,CLRF	MOV AL,00001111B
MOV AH,9	MOV DX,0300H
INT 21H	OUT DX,AL
LEA DX,MSG13	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	
MOV AH,9	LEA DX,MSG13
INT 21H	MOV AH,9
LEA DX,MSG3	INT 21H
MOV AH,9	LEA DX,CLRF
INT 21H	MOV AH,9
MOV AH,1	INT 21H
INT 21H	LEA DX,MSG6
	MOV AH,9
MOV AL,89H	INT 21H
MOV DX,0303H	MOV AH,1
OUT DX,AL	INT 21H
MOV AL,00110011B	MOV AL,00001111B
MOV DX,0300H	MOV DX,0300H
OUT DX,AL	OUT DX,AL
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG13	LEA DX,MSG13
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG4	LEA DX,MSG7
MOV AH,9	MOV AH,9
INT 21H	INT 21H
MOV AH,1	MOV AH,1
INT 21H	INT 21H
MOV AL,00110011B	MOV AL,00000000B
MOV DX,0300H	MOV DX,0300H
OUT DX,AL	OUT DX,AL
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG13	LEA DX,MSG13

MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	
MOV AH,9	MOV AH,1
INT 21H	INT 21H
LEA DX,MSG8	JMP EXIT
MOV AH,9	
INT 21H	F2: LEA DX,CLRF
MOV AH,1	MOV AH,9
INT 21H	INT 21H
MOV AL,00110011B	LEA DX,MSG13
MOV DX,0300H	MOV AH,9
OUT DX,AL	INT 21H
	LEA DX,CLRF
LEA DX,CLRF	MOV AH,9
MOV AH,9	INT 21H
INT 21H	LEA DX,MSG3
	MOV AH,9
LEA DX,MSG13	INT 21H
MOV AH,9	MOV AH,1
INT 21H	INT 21H
LEA DX,CLRF	
MOV AH,9	MOV AL,89H
INT 21H	MOV DX,0303H
LEA DX,MSG9	OUT DX,AL
MOV AH,9	
INT 21H	MOV AL,00110011B
MOV AH,1	MOV DX,0300H
INT 21H	OUT DX,AL
MOV AL,00110011B	LEA DX,CLRF
MOV DX,0300H	MOV AH,9
OUT DX,AL	INT 21H
LEA DX,CLRF	LEA DX,MSG13
MOV AH,9	MOV AH,9
INT 21H	INT 21H
	LEA DX,CLRF
LEA DX,MSG11	MOV AH,9
MOV AH,9	INT 21H
INT 21H	LEA DX,MSG4
LEA DX,CLRF	MOV AH,9
MOV AH,9	INT 21H
INT 21H	MOV AH,1
LEA DX,MSG10	INT 21H
MOV AH,9	
INT 21H	MOV AL,00110011B
MOV AH,1	MOV DX,0300H
INT 21H	OUT DX,AL
MOV AL,DAT	LEA DX,CLRF
MOV DX,0300H	MOV AH,9
OUT DX,AL	INT 21H
LEA DX,CLRF	LEA DX,MSG13
MOV AH,9	MOV AH,9
INT 21H	INT 21H
	LEA DX,CLRF
LEA DX,MSG12	MOV AH,9

INT 21H
LEA DX,MSG5
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00000000B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11110000B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00001111B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9

INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG9
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG11
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG10
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,DAT
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG12
MOV AH,9
INT 21H

MOV AH,1

INT 21H JMP EXIT	MOV AH,1 INT 21H
F3: LEA DX,CLRF MOV AH,9 INT 21H	MOV AL,00000000B MOV DX,0300H OUT DX,AL
LEA DX,MSG13 MOV AH,9 INT 21H LEA DX,CLRF MOV AH,9 INT 21H LEA DX,MSG3 MOV AH,9 INT 21H MOV AH,1 INT 21H	LEA DX,CLRF MOV AH,9 INT 21H
MOV AL,89H MOV DX,0303H OUT DX,AL	LEA DX,MSG13 MOV AH,9 INT 21H LEA DX,CLRF MOV AH,9 INT 21H LEA DX,MSG6 MOV AH,9 INT 21H MOV AH,1 INT 21H
MOV AL,00110011B MOV DX,0300H OUT DX,AL	MOV AL,11110000B MOV DX,0300H OUT DX,AL
LEA DX,CLRF MOV AH,9 INT 21H	LEA DX,CLRF MOV AH,9 INT 21H
LEA DX,MSG13 MOV AH,9 INT 21H LEA DX,CLRF MOV AH,9 INT 21H LEA DX,MSG4 MOV AH,9 INT 21H MOV AH,1 INT 21H	LEA DX,MSG13 MOV AH,9 INT 21H LEA DX,CLRF MOV AH,9 INT 21H LEA DX,MSG7 MOV AH,9 INT 21H MOV AH,1 INT 21H
MOV AL,00110011B MOV DX,0300H OUT DX,AL	MOV AL,00000000B MOV DX,0300H OUT DX,AL
LEA DX,CLRF MOV AH,9 INT 21H	LEA DX,CLRF MOV AH,9 INT 21H
LEA DX,MSG13 MOV AH,9 INT 21H LEA DX,CLRF MOV AH,9 INT 21H LEA DX,MSG5 MOV AH,9 INT 21H	LEA DX,MSG13 MOV AH,9 INT 21H LEA DX,CLRF MOV AH,9 INT 21H LEA DX,MSG8 MOV AH,9 INT 21H

MOV AH,1	MOV AH,9
INT 21H	INT 21H
MOV AL,00110011B	LEA DX,MSG13
MOV DX,0300H	MOV AH,9
OUT DX,AL	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG13	LEA DX,MSG3
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	MOV AH,1
MOV AH,9	INT 21H
INT 21H	MOV AL,89H
LEA DX,MSG9	MOV DX,0303H
MOV AH,9	OUT DX,AL
INT 21H	MOV AL,00110011B
MOV AH,1	MOV DX,0300H
INT 21H	OUT DX,AL
MOV AL,00110011B	LEA DX,CLRF
MOV DX,0300H	MOV AH,9
OUT DX,AL	INT 21H
LEA DX,CLRF	LEA DX,MSG13
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG11	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,MSG4
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG10	MOV AH,1
MOV AH,9	INT 21H
INT 21H	MOV AL,00110011B
MOV AH,1	MOV DX,0300H
INT 21H	OUT DX,AL
MOV AL,DAT	LEA DX,CLRF
MOV DX,0300H	MOV AH,9
OUT DX,AL	INT 21H
LEA DX,CLRF	LEA DX,MSG13
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG12	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
MOV AH,1	LEA DX,MSG5
INT 21H	MOV AH,9
JMP EXIT	INT 21H
	MOV AH,1
	INT 21H
F4: LEA DX,CLRF	MOV AL,00000000B

MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,1111111B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00001111B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B

MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG9
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG11
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG10
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,DAT
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG12
MOV AH,9
INT 21H

MOV AH,1
INT 21H
JMP EXIT

CY: LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG18
MOV AH,9

INT 21H	INT 21H
LEA DX,CLRF	LEA DX,MSG4
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG19	MOV AH,1
MOV AH,9	INT 21H
INT 21H	
LEA DX,CLRF	MOV AL,00110011B
MOV AH,9	MOV DX,0300H
INT 21H	OUT DX,AL
LEA DX,CLRF	
MOV AH,9	LEA DX,CLRF
INT 21H	MOV AH,9
LEA DX,MSG1	INT 21H
MOV AH,9	
INT 21H	LEA DX,MSG13
MOV AH,1	MOV AH,9
INT 21H	INT 21H
	LEA DX,CLRF
CMP AL,31H	MOV AH,9
JE S1	INT 21H
CMP AL,32H	LEA DX,MSG5
JE S22	MOV AH,9
JMP EXIT	INT 21H
	MOV AH,1
	INT 21H
S22: JMP S2	
	MOV AL,10101100B
S1: LEA DX,CLRF	MOV DX,0300H
MOV AH,9	OUT DX,AL
INT 21H	
	LEA DX,CLRF
LEA DX,MSG13	MOV AH,9
MOV AH,9	INT 21H
INT 21H	
LEA DX,CLRF	LEA DX,MSG13
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG3	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
MOV AH,1	LEA DX,MSG6
INT 21H	MOV AH,9
	INT 21H
MOV AL,89H	MOV AH,1
MOV DX,0303H	INT 21H
OUT DX,AL	
	MOV AL,01101010B
MOV AL,00110011B	MOV DX,0300H
MOV DX,0300H	OUT DX,AL
OUT DX,AL	
	LEA DX,CLRF
LEA DX,CLRF	MOV AH,9
MOV AH,9	INT 21H
INT 21H	
	LEA DX,MSG13
LEA DX,MSG13	MOV AH,9
MOV AH,9	INT 21H
INT 21H	LEA DX,CLRF
LEA DX,CLRF	MOV AH,9
MOV AH,9	

INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00001010B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG9
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG11
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9

INT 21H
LEA DX,MSG10
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,DAT
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG12
MOV AH,9
INT 21H

MOV AH,1
INT 21H
JMP EXIT

S2: LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG3
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,89H
MOV DX,0303H
OUT DX,AL

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG4
MOV AH,9
INT 21H

MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG5
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,01101010B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,10101010B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H

MOV AH,1
INT 21H

MOV AL,00001100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG9
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG11
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG10
MOV AH,9
INT 21H

MOV AH,1
INT 21H

MOV AL,DAT
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG12
MOV AH,9
INT 21H

MOV AH,1
INT 21H
JMP EXIT

EXIT: MOV DX,0300H
MOV AL,00
OUT DX,AL

MOV AX,4C00H
INT 21H

CODE ENDS
END START



Benes Network with first
or last stage fault

DATA SEGMENT

PERF DB '1.Perfect Shuffle\$'

BIT DB '2.Bit Reverse\$'

FLIP DB '3.Flip Permutation\$'

SHIF DB '4.Cyclic Shift\$'

CLRF DB 10,13,'\$'

DAT DB ?

MSG1 DB 'Please choose a number:
\$'

MSG2 DB 'Please enter the data: \$'

MSG13 DB 'Sending controls to
port....\$'

MSG3 DB '0301 , the first set of the
bypass circuits.\$'

MSG4 DB '0302 , the second set of
the bypass circuits.\$'

MSG5 DB '0303 , the first set of the
switches.\$'

MSG6 DB '0304 , the second set of
the switches.\$'

MSG7 DB '0305 , the third set of the
switches.\$'

MSG8 DB '0306 , the third set of the
bypass circuits.\$'

MSG9 DB '0307 , the forth set of the
bypass circuits.\$'

MSG10 DB '0300 , the data inputs.\$'

MSG11 DB 'Sending the data to
port....\$'

MSG12 DB 'Please latch the data
port.\$'

MSG14 DB '1.101\$'

MSG15 DB '2.011\$'

MSG16 DB '3.010\$'

MSG17 DB '4.111\$'

MSG18 DB '1.Shifted by 1 position.\$'

MSG19 DB '2.Shifted by 2
positions.\$'

MSG20 DB 'First or Last Stage
Fault\$'

MSG22 DB '1.Straight State.\$'

MSG23 DB '2.Exchange State.\$'

DATA ENDS

CODE SEGMENT

ASSUME CS:CODE , DS:DATA

START: MOV AX,DATA

MOV DS,AX

FIRST:

LEA DX,CLRF

MOV AH,9

INT 21H

LEA DX,CLRF

MOV AH,9

INT 21H

LEA DX,CLRF

MOV AH,9

INT 21H

LEA DX,CLRF

MOV AH,9

INT 21H

LEA DX,CLRF

MOV AH,9

INT 21H

LEA DX,CLRF

MOV AH,9

INT 21H

LEA DX,CLRF

MOV AH,9

INT 21H

LEA DX,CLRF

MOV AH,9

INT 21H

LEA DX,CLRF

MOV AH,9

INT 21H

LEA DX,CLRF

MOV AH,9

INT 21H

LEA DX,CLRF

MOV AH,9

INT 21H

LEA DX,CLRF

MOV AH,9

INT 21H

LEA DX,CLRF

MOV AH,9

INT 21H

LEA DX,CLRF

MOV AH,9

INT 21H

LEA DX,CLRF

MOV AH,9

INT 21H

LEA DX,CLRF

MOV AH,9

INT 21H

LEA DX,CLRF

MOV AH,9

INT 21H

LEA DX,CLRF

MOV AH,9

INT 21H

LEA DX,CLRF

MOV AH,9

INT 21H

LEA DX,CLRF

MOV AH,9

INT 21H

LEA DX,CLRF

MOV AH,9

INT 21H

LEA DX,CLRF

MOV AH,9

INT 21H

LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG20	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,PERF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,BIT	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,FLIP	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,SHIF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG1	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
MOV AH,1	LEA DX,CLRF
controls	MOV AH,9
INT 21H	INT 21H
MOV BL,AL	LEA DX,CLRF
	MOV AH,9
	INT 21H

;Get the

MOV AH,9	CMP AL,31H	;Straight
INT 21H	or Exchange	
LEA DX,CLRF	JE PE_S	
MOV AH,9	JMP PE_X	
INT 21H		
LEA DX,CLRF	PE_S: LEA DX,CLRF	
MOV AH,9	MOV AH,9	
INT 21H	INT 21H	
LEA DX,CLRF		
MOV AH,9	LEA DX,MSG13	
INT 21H	MOV AH,9	
LEA DX,CLRF	INT 21H	
MOV AH,9	LEA DX,CLRF	
INT 21H	MOV AH,9	
LEA DX,CLRF	INT 21H	
MOV AH,9	LEA DX,MSG3	
INT 21H	MOV AH,9	
LEA DX,CLRF	INT 21H	
MOV AH,9	MOV AH,1	
INT 21H	INT 21H	
LEA DX,CLRF		
MOV AH,9	MOV AL,89H	
INT 21H	MOV DX,0303H	
LEA DX,CLRF	OUT DX,AL	
MOV AH,9		
INT 21H	MOV AL,00110011B	
LEA DX,CLRF	MOV DX,0300H	
MOV AH,9	OUT DX,AL	
INT 21H		
LEA DX,CLRF	LEA DX,CLRF	
MOV AH,9	MOV AH,9	
INT 21H	INT 21H	
LEA DX,CLRF	LEA DX,MSG13	
MOV AH,9	MOV AH,9	
INT 21H	INT 21H	
LEA DX,CLRF	LEA DX,CLRF	
MOV AH,9	MOV AH,9	
INT 21H	INT 21H	
LEA DX,MSG22	LEA DX,MSG4	
MOV AH,9	MOV AH,9	
INT 21H	INT 21H	
LEA DX,CLRF	MOV AH,1	
MOV AH,9	INT 21H	
INT 21H		
LEA DX,MSG23	MOV AL,11001100B	
MOV AH,9	MOV DX,0300H	
INT 21H	OUT DX,AL	
LEA DX,CLRF		
MOV AH,9	LEA DX,CLRF	
INT 21H	MOV AH,9	
LEA DX,CLRF	INT 21H	
MOV AH,9		
INT 21H	LEA DX,MSG13	
LEA DX,MSG1	MOV AH,9	
MOV AH,9	INT 21H	
INT 21H	LEA DX,CLRF	
MOV AH,1	MOV AH,9	
INT 21H	INT 21H	
	LEA DX,MSG5	

MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,10101100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,01101010B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00001010B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8

MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00111100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG9
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00111100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG11
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG10
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,DAT
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG12
MOV AH,9
INT 21H

MOV AH,1
INT 21H
JMP EXIT

LEA DX,MSG3
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,89H
MOV DX,0303H
OUT DX,AL

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG4
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11001100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG5
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,10001100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9

INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,01001100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00001100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11001100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9

[illegible]

MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG3
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,89H
MOV DX,0303H
OUT DX,AL

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG4
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG5
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00001111B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00001111B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00000000B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

[illegible]

```
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
```

```
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG22
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG23
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG1
MOV AH,9
INT 21H
MOV AH,1
INT 21H
```

```

CMP AL,31H      ;Straight
or Exchange
JE F2_S
JMP F2_X

```

```
F2_S: LEA DX,CLRF
      MOV AH,9
      INT 21H
      LEA DX,CLRF
      MOV AH,9
      INT 21H
      LEA DX,CLRF
      MOV AH,9
      INT 21H
      LEA DX,CLRF
      MOV AH,9
```

[illegible]

INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG3
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,89H
MOV DX,0303H
OUT DX,AL

MOV AL,11001100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG4
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11001100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG5

MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00000000B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11110000B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00001111B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8

INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG3
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,89H
MOV DX,0303H
OUT DX,AL

MOV AL,11001100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG4
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11001100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9

INT 21H
LEA DX,MSG5
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00000000B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11110000B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00000000B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9

LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG3
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,89H
MOV DX,0303H
OUT DX,AL

MOV AL,11001100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG4
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11001100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H

LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG5
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00000000B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11111111B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00001111B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H

LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG18	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG19	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG1	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
MOV AH,1	LEA DX,CLRF
INT 21H	MOV AH,9
	INT 21H
CMP AL,31H	LEA DX,CLRF
JE S1	MOV AH,9
CMP AL,32H	INT 21H
JE S22	LEA DX,CLRF
JMP EXIT	MOV AH,9
	INT 21H
S22: JMP S2	LEA DX,CLRF
	MOV AH,9
S1:	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H

MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG3
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,89H
MOV DX,0303H
OUT DX,AL

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG4
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11001100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG5
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,10101100B

MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,01101010B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00001010B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00111100B

[illegible]

```

MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9

```

```
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
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LEA DX,CLRF
MOV AH,9
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INT 21H
LEA DX,CLRF
MOV AH,9
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INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
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LEA DX,CLRF
MOV AH,9
INT 21H
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LEA DX,CLRF
MOV AH,9
INT 21H
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LEA DX,CLRF
MOV AH,9
INT 21H
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LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
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LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
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LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
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LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
```

```
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
```

```
LEA DX,CERT
MOV AH,9
INT 21H
LEA DX,CLRF
```

```
MOV AH,9
INT 21H
LEA DX,CLRF
```

```
MOV AH,9
INT 21H
LEA DX,CLRF
```


INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG3
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,89H
MOV DX,0303H
OUT DX,AL

MOV AL,00111100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG4
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00111100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG5
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,01101010B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,10101010B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00001100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11001100B	INT 21H
MOV DX,0300H	LEA DX,MSG13
OUT DX,AL	MOV AH,9
LEA DX,CLRF	INT 21H
MOV AH,9	LEA DX,CLRF
INT 21H	MOV AH,9
LEA DX,MSG13	INT 21H
MOV AH,9	LEA DX,MSG3
INT 21H	MOV AH,9
LEA DX,CLRF	INT 21H
MOV AH,9	MOV AH,1
INT 21H	INT 21H
LEA DX,MSG9	MOV AL,89H
MOV AH,9	MOV DX,0303H
INT 21H	OUT DX,AL
MOV AH,1	MOV AL,11001100B
INT 21H	MOV DX,0300H
MOV AL,00110011B	OUT DX,AL
MOV DX,0300H	LEA DX,CLRF
OUT DX,AL	MOV AH,9
LEA DX,CLRF	INT 21H
MOV AH,9	LEA DX,MSG13
INT 21H	MOV AH,9
LEA DX,MSG11	INT 21H
MOV AH,9	LEA DX,CLRF
INT 21H	MOV AH,9
LEA DX,CLRF	INT 21H
MOV AH,9	LEA DX,MSG4
INT 21H	MOV AH,9
LEA DX,MSG10	INT 21H
MOV AH,9	MOV AH,1
INT 21H	INT 21H
MOV AH,1	MOV AL,00110011B
INT 21H	MOV DX,0300H
MOV AL,DAT	OUT DX,AL
MOV DX,0300H	LEA DX,CLRF
OUT DX,AL	MOV AH,9
LEA DX,CLRF	INT 21H
MOV AH,9	LEA DX,MSG13
INT 21H	MOV AH,9
LEA DX,MSG12	INT 21H
MOV AH,9	LEA DX,CLRF
INT 21H	MOV AH,9
MOV AH,1	INT 21H
INT 21H	LEA DX,MSG5
JMP EXIT	MOV AH,9
	INT 21H
	MOV AH,1
	INT 21H
PE_X: LEA DX,CLRF	MOV AL,10100011B
MOV AH,9	MOV DX,0300H

OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,10011010B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00000101B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11000011B
MOV DX,0300H

OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG9
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11000011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG11
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG10
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,DAT
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG12
MOV AH,9
INT 21H

MOV AH,1
INT 21H
JMP EXIT

BI_X: LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13

MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG3
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,89H
MOV DX,0303H
OUT DX,AL

MOV AL,11001100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG4
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG5
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00100011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF

MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00010011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00000011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF

MOV AH,9	INT 21H
INT 21H	LEA DX,MSG3
LEA DX,MSG13	MOV AH,9
MOV AH,9	INT 21H
INT 21H	MOV AH,1
LEA DX,CLRF	INT 21H
MOV AH,9	MOV AL,89H
INT 21H	MOV DX,0303H
LEA DX,MSG9	OUT DX,AL
MOV AH,9	
INT 21H	MOV AL,11001100B
MOV AH,1	MOV DX,0300H
INT 21H	OUT DX,AL
MOV AL,11001100B	
MOV DX,0300H	LEA DX,CLRF
OUT DX,AL	MOV AH,9
	INT 21H
LEA DX,CLRF	LEA DX,MSG13
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG11	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,MSG4
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG10	MOV AH,1
MOV AH,9	INT 21H
INT 21H	MOV AL,11001100B
MOV AH,1	MOV DX,0300H
INT 21H	OUT DX,AL
MOV AL,DAT	LEA DX,CLRF
MOV DX,0300H	MOV AH,9
OUT DX,AL	INT 21H
LEA DX,CLRF	LEA DX,MSG13
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG12	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
MOV AH,1	LEA DX,MSG5
INT 21H	MOV AH,9
JMP EXIT	INT 21H
	MOV AH,1
	INT 21H
F1_X: LEA DX,CLRF	MOV AL,00000000B
MOV AH,9	MOV DX,0300H
INT 21H	OUT DX,AL
LEA DX,MSG13	
MOV AH,9	LEA DX,CLRF
INT 21H	MOV AH,9
LEA DX,CLRF	INT 21H
MOV AH,9	LEA DX,MSG13

MOV AH,1
INT 21H

MOV AL,89H
MOV DX,0303H
OUT DX,AL

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG4
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG5
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00001111B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9

INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11110000B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00000000B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11001100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9

INT 21H	MOV DX,0303H
LEA DX,MSG9	OUT DX,AL
MOV AH,9	
INT 21H	MOV AL,00110011B
MOV AH,1	MOV DX,0300H
INT 21H	OUT DX,AL
MOV AL,11001100B	LEA DX,CLRF
MOV DX,0300H	MOV AH,9
OUT DX,AL	INT 21H
LEA DX,CLRF	LEA DX,MSG13
MOV AH,9	MOV AH,9
INT 21H	INT 21H
	LEA DX,CLRF
LEA DX,MSG11	MOV AH,9
MOV AH,9	INT 21H
INT 21H	LEA DX,MSG4
LEA DX,CLRF	MOV AH,9
MOV AH,9	INT 21H
INT 21H	MOV AH,1
LEA DX,MSG10	INT 21H
MOV AH,9	
INT 21H	MOV AL,00110011B
MOV AH,1	MOV DX,0300H
INT 21H	OUT DX,AL
MOV AL,DAT	LEA DX,CLRF
MOV DX,0300H	MOV AH,9
OUT DX,AL	INT 21H
LEA DX,CLRF	LEA DX,MSG13
MOV AH,9	MOV AH,9
INT 21H	INT 21H
	LEA DX,CLRF
LEA DX,MSG12	MOV AH,9
MOV AH,9	INT 21H
INT 21H	LEA DX,MSG5
	MOV AH,9
MOV AH,1	INT 21H
INT 21H	MOV AH,1
JMP EXIT	INT 21H
F3_X: LEA DX,CLRF	MOV AL,00001111B
MOV AH,9	MOV DX,0300H
INT 21H	OUT DX,AL
LEA DX,MSG13	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	
MOV AH,9	LEA DX,MSG13
INT 21H	MOV AH,9
LEA DX,MSG3	INT 21H
MOV AH,9	LEA DX,CLRF
INT 21H	MOV AH,9
MOV AH,1	INT 21H
INT 21H	LEA DX,MSG6
	MOV AH,9
MOV AL,89H	INT 21H

MOV AH,1
INT 21H

MOV AL,11110000B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00001111B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG9
MOV AH,9
INT 21H

MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG11
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG10
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,DAT
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG12
MOV AH,9
INT 21H
MOV AH,1
INT 21H
JMP EXIT

F4_X: LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG3
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,89H
MOV DX,0303H
OUT DX,AL

MOV AL,00110011B

MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG4
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG5
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00001111B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11111111B

MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00000000B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11001100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG9
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11001100B

MOV DX,0300H OUT DX,AL	MOV AH,9 INT 21H
LEA DX,CLRF MOV AH,9 INT 21H	LEA DX,MSG13 MOV AH,9 INT 21H LEA DX,CLRF MOV AH,9 INT 21H LEA DX,MSG4 MOV AH,9 INT 21H MOV AH,1 INT 21H
LEA DX,MSG11 MOV AH,9 INT 21H LEA DX,CLRF MOV AH,9 INT 21H LEA DX,MSG10 MOV AH,9 INT 21H MOV AH,1 INT 21H	MOV AL,00110011B MOV DX,0300H OUT DX,AL
MOV AL,DAT MOV DX,0300H OUT DX,AL	LEA DX,CLRF MOV AH,9 INT 21H
LEA DX,CLRF MOV AH,9 INT 21H	LEA DX,MSG13 MOV AH,9 INT 21H LEA DX,CLRF MOV AH,9 INT 21H LEA DX,MSG5 MOV AH,9 INT 21H MOV AH,1 INT 21H
LEA DX,MSG12 MOV AH,9 INT 21H	
MOV AH,1 INT 21H JMP EXIT	
S1_X: LEA DX,CLRF MOV AH,9 INT 21H	MOV AL,10100011B MOV DX,0300H OUT DX,AL
LEA DX,MSG13 MOV AH,9 INT 21H LEA DX,CLRF MOV AH,9 INT 21H LEA DX,MSG3 MOV AH,9 INT 21H MOV AH,1 INT 21H	LEA DX,CLRF MOV AH,9 INT 21H
MOV AL,89H MOV DX,0303H OUT DX,AL	LEA DX,MSG13 MOV AH,9 INT 21H LEA DX,CLRF MOV AH,9 INT 21H LEA DX,MSG6 MOV AH,9 INT 21H MOV AH,1 INT 21H
MOV AL,11001100B MOV DX,0300H OUT DX,AL	MOV AL,10011010B MOV DX,0300H OUT DX,AL
LEA DX,CLRF	LEA DX,CLRF

MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00000101B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11000011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG9
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11000011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF

MOV AH,9
INT 21H

LEA DX,MSG11
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG10
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,DAT
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG12
MOV AH,9
INT 21H

MOV AH,1
INT 21H
JMP EXIT

S2_X: LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG3
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,89H
MOV DX,0303H
OUT DX,AL

MOV AL,11000011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13

MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG4
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11000011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG5
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,10010101B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,10101010B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13

MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00000011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG9
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11001100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG11

```
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG10
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,DAT
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG12
MOV AH,9
INT 21H
MOV AH,1
INT 21H
JMP EXIT

EXIT: MOV DX,0300H
MOV AL,00
OUT DX,AL

MOV AX,4C00H
INT 21H

CODE ENDS
END START
```



second set of
third set of the
third set of the
forth set of the
e data inputs.\$'
the data to
atch the data
by 1 position.\$'
by 2

second set of
third set of the
third set of the
forth set of the
e data inputs.\$'
the data to
atch the data
by 1 position.\$'
by 2

second set of
third set of the
third set of the
forth set of the
e data inputs.\$'
the data to
atch the data
by 1 position.\$'
by 2

INT 21H
 LEA DX,CLRF
 MOV AH,9
 INT 21H
 LEA DX,CLRF
 MOV AH,9
 INT 21H
 LEA DX,CLRF
 MOV AH,9
 INT 21H
 LEA DX,CLRF
 MOV AH,9
 INT 21H
 LEA DX,CLRF
 MOV AH,9
 INT 21H
 LEA DX,CLRF
 MOV AH,9
 INT 21H
 LEA DX,CLRF
 MOV AH,9
 INT 21H

LEA DX,MSG13
 MOV AH,9
 INT 21H
 LEA DX,CLRF
 MOV AH,9
 INT 21H
 LEA DX,MSG3
 MOV AH,9
 INT 21H
 MOV AH,1
 INT 21H

MOV AL,89H
 MOV DX,0303H
 OUT DX,AL

MOV AL,00110011B
 MOV DX,0300H
 OUT DX,AL

LEA DX,CLRF
 MOV AH,9
 INT 21H

LEA DX,MSG13
 MOV AH,9
 INT 21H
 LEA DX,CLRF
 MOV AH,9
 INT 21H
 LEA DX,MSG4
 MOV AH,9
 INT 21H
 MOV AH,1

INT 21H

MOV AL,00110011B
 MOV DX,0300H
 OUT DX,AL

LEA DX,CLRF
 MOV AH,9
 INT 21H

LEA DX,MSG13
 MOV AH,9
 INT 21H
 LEA DX,CLRF
 MOV AH,9
 INT 21H
 LEA DX,MSG5
 MOV AH,9
 INT 21H
 MOV AH,1
 INT 21H

MOV AL,10101100B
 MOV DX,0300H
 OUT DX,AL

LEA DX,CLRF
 MOV AH,9
 INT 21H

LEA DX,MSG13
 MOV AH,9
 INT 21H
 LEA DX,CLRF
 MOV AH,9
 INT 21H
 LEA DX,MSG6
 MOV AH,9
 INT 21H
 MOV AH,1
 INT 21H

MOV AL,01101010B
 MOV DX,0300H
 OUT DX,AL

LEA DX,CLRF
 MOV AH,9
 INT 21H

LEA DX,MSG13
 MOV AH,9
 INT 21H
 LEA DX,CLRF
 MOV AH,9
 INT 21H
 LEA DX,MSG7
 MOV AH,9
 INT 21H
 MOV AH,1

INT 21H	INT 21H
MOV AL,00001010B	MOV AL,DAT
MOV DX,0300H	MOV DX,0300H
OUT DX,AL	OUT DX,AL
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG13	LEA DX,MSG12
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG8	LEA DX,MSG21
MOV AH,9	MOV AH,9
INT 21H	INT 21H
MOV AH,1	MOV AH,1
INT 21H	INT 21H
MOV AL,00110011B	LEA DX,CLRF
MOV DX,0300H	MOV AH,9
OUT DX,AL	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG13	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG9	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
MOV AH,1	LEA DX,CLRF
INT 21H	MOV AH,9
MOV AL,00110011B	INT 21H
MOV DX,0300H	LEA DX,CLRF
OUT DX,AL	MOV AH,9
LEA DX,CLRF	INT 21H
MOV AH,9	LEA DX,CLRF
INT 21H	MOV AH,9
LEA DX,MSG11	INT 21H
MOV AH,9	LEA DX,CLRF
INT 21H	MOV AH,9
LEA DX,CLRF	INT 21H
MOV AH,9	LEA DX,CLRF
INT 21H	MOV AH,9
LEA DX,MSG10	INT 21H
MOV AH,9	LEA DX,CLRF
INT 21H	MOV AH,9
MOV AH,1	

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00000101B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG9
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG11
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG10
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,DAT
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG12
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG22
MOV AH,9
INT 21H

MOV AH,1
INT 21H
JMP EXIT

BI: LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H

INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,01001100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00001100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9

INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG9
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG11
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG10
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,DAT
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG12
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG21
MOV AH,9
INT 21H
MOV AH,1
INT 21H

LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H

INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG5
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00100011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00010011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00000011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9

INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG9
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG11
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG10
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,DAT
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG12
MOV AH,9

CMP AL,31H	MOV AH,9
JE F1	INT 21H
CMP AL,32H	LEA DX,CLRF
JE F22	MOV AH,9
CMP AL,33H	INT 21H
JE F33	LEA DX,CLRF
CMP AL,34H	MOV AH,9
JE F44	INT 21H
JMP EXIT	LEA DX,CLRF
	MOV AH,9
F22: JMP F2	INT 21H
F33: JMP F3	LEA DX,CLRF
F44: JMP F4	MOV AH,9
	INT 21H
F1: LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,MSG13
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,MSG3
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	MOV AH,1
MOV AH,9	INT 21H
INT 21H	
LEA DX,CLRF	
MOV AH,9	MOV AL,89H
INT 21H	MOV DX,0303H
LEA DX,CLRF	OUT DX,AL
MOV AH,9	
INT 21H	MOV AL,00110011B
LEA DX,CLRF	MOV DX,0300H
MOV AH,9	OUT DX,AL
INT 21H	
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	
MOV AH,9	LEA DX,MSG13
INT 21H	MOV AH,9
LEA DX,CLRF	INT 21H

LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG4
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG5
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00001111B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00001111B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H

LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00000000B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG9
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG11
MOV AH,9
INT 21H

LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG10
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,DAT
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG12
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG21
MOV AH,9
INT 21H

MOV AH,1
INT 21H

LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG3
MOV AH,9
INT 21H
MOV AH,1

INT 21H	LEA DX,MSG6
MOV AL,89H	MOV AH,9
MOV DX,0303H	INT 21H
OUT DX,AL	MOV AH,1
	INT 21H
MOV AL,00110011B	MOV AL,00001111B
MOV DX,0300H	MOV DX,0300H
OUT DX,AL	OUT DX,AL
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG13	LEA DX,MSG13
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG4	LEA DX,MSG7
MOV AH,9	MOV AH,9
INT 21H	INT 21H
MOV AH,1	MOV AH,1
INT 21H	INT 21H
MOV AL,00110011B	MOV AL,00001111B
MOV DX,0300H	MOV DX,0300H
OUT DX,AL	OUT DX,AL
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG13	LEA DX,MSG13
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG5	LEA DX,MSG8
MOV AH,9	MOV AH,9
INT 21H	INT 21H
MOV AH,1	MOV AH,1
INT 21H	INT 21H
MOV AL,00000000B	MOV AL,00110011B
MOV DX,0300H	MOV DX,0300H
OUT DX,AL	OUT DX,AL
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG13	LEA DX,MSG13
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H

LEA DX,MSG9	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
MOV AH,1	LEA DX,CLRF
INT 21H	MOV AH,9
	INT 21H
MOV AL,00110011B	LEA DX,CLRF
MOV DX,0300H	MOV AH,9
OUT DX,AL	INT 21H
	LEA DX,CLRF
LEA DX,CLRF	MOV AH,9
MOV AH,9	INT 21H
INT 21H	LEA DX,CLRF
	MOV AH,9
LEA DX,MSG11	INT 21H
MOV AH,9	LEA DX,CLRF
INT 21H	MOV AH,9
LEA DX,CLRF	INT 21H
MOV AH,9	LEA DX,CLRF
INT 21H	MOV AH,9
LEA DX,MSG10	INT 21H
MOV AH,9	LEA DX,CLRF
INT 21H	MOV AH,9
MOV AH,1	INT 21H
INT 21H	LEA DX,CLRF
	MOV AH,9
MOV AL,DAT	INT 21H
MOV DX,0300H	LEA DX,CLRF
OUT DX,AL	MOV AH,9
	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
	LEA DX,CLRF
LEA DX,MSG12	MOV AH,9
MOV AH,9	INT 21H
INT 21H	LEA DX,CLRF
LEA DX,CLRF	MOV AH,9
MOV AH,9	INT 21H
INT 21H	LEA DX,CLRF
LEA DX,MSG22	MOV AH,9
MOV AH,9	INT 21H
INT 21H	LEA DX,CLRF
	MOV AH,9
MOV AH,1	INT 21H
INT 21H	LEA DX,CLRF
JMP EXIT	MOV AH,9
	INT 21H
F2: LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H

LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG3
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,89H
MOV DX,0303H
OUT DX,AL

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG4
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG5
MOV AH,9
INT 21H

MOV AH,1
INT 21H

MOV AL,00000000B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11110000B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00001111B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H

INT 21H	MOV DX,0300H
LEA DX,CLRF	OUT DX,AL
MOV AH,9	
INT 21H	LEA DX,CLRF
LEA DX,CLRF	MOV AH,9
MOV AH,9	INT 21H
INT 21H	
LEA DX,CLRF	LEA DX,MSG13
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,MSG5
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	MOV AH,1
MOV AH,9	INT 21H
INT 21H	
LEA DX,CLRF	MOV AL,00001111B
MOV AH,9	MOV DX,0300H
INT 21H	OUT DX,AL
LEA DX,MSG13	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	
MOV AH,9	LEA DX,MSG13
INT 21H	MOV AH,9
LEA DX,MSG3	INT 21H
MOV AH,9	LEA DX,CLRF
INT 21H	MOV AH,9
MOV AH,1	INT 21H
INT 21H	LEA DX,MSG6
	MOV AH,9
MOV AL,89H	INT 21H
MOV DX,0303H	MOV AH,1
OUT DX,AL*	INT 21H
MOV AL,00110011B	MOV AL,11110000B
MOV DX,0300H	MOV DX,0300H
OUT DX,AL	OUT DX,AL
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG13	LEA DX,MSG13
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG4	LEA DX,MSG7
MOV AH,9	MOV AH,9
INT 21H	INT 21H
MOV AH,1	MOV AH,1
INT 21H	INT 21H
MOV AL,00110011B	MOV AL,00000000B

```
MOV DX,0300H
OUT DX,AL
```

```
LEA DX,CLRF
MOV AH,9
INT 21H
```

```
LEA DX,MSG12
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG22
MOV AH,9
INT 21H
```

```
MOV AH,1
INT 21H
JMP EXIT
```

```
MOV AL,00110011B
MOV DX,0300H
OUT DX,AL
```

F3: LEA DX,CLRF

```
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
```

```
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
```

```
MOV AL,00110011B
MOV DX,0300H
OUT DX,AL
```

```
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
```

```
LEA DX,CLRF
MOV AH,9
INT 21H
```

```
LEA DX,CLRF
MOV AH,9
INT 21H
```

```
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
```

MOV AL,DAT

LEA DX,MSG13	LEA DX,MSG13
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG6	LEA DX,MSG9
MOV AH,9	MOV AH,9
INT 21H	INT 21H
MOV AH,1	MOV AH,1
INT 21H	INT 21H
MOV AL,11110000B	MOV AL,00110011B
MOV DX,0300H	MOV DX,0300H
OUT DX,AL	OUT DX,AL
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG13	LEA DX,MSG11
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG7	LEA DX,MSG10
MOV AH,9	MOV AH,9
INT 21H	INT 21H
MOV AH,1	MOV AH,1
INT 21H	INT 21H
MOV AL,00001111B	MOV AL,DAT
MOV DX,0300H	MOV DX,0300H
OUT DX,AL	OUT DX,AL
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG13	LEA DX,MSG12
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,CLRF	LEA DX,CLRF
MOV AH,9	MOV AH,9
INT 21H	INT 21H
LEA DX,MSG8	LEA DX,MSG22
MOV AH,9	MOV AH,9
INT 21H	INT 21H
MOV AH,1	
INT 21H	MOV AH,1
 	INT 21H
MOV AL,00110011B	JMP EXIT
MOV DX,0300H	
OUT DX,AL	F4: LEA DX,CLRF
 	MOV AH,9
LEA DX,CLRF	INT 21H
MOV AH,9	LEA DX,CLRF
INT 21H	MOV AH,9
	INT 21H

LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG5
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00000000B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11111111B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00001111B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H

LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG9
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG11
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG10
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,DAT
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG12
MOV AH,9
INT 21H

MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG5
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00001111B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,11111111B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7

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MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00000000B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

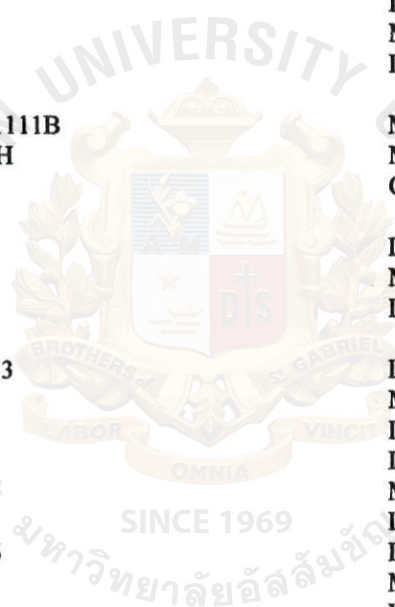
LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG9
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG11
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG10



INT 21H
LEA DX,MSG4
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG5
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,10101100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,01101010B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9

INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00001010B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG9
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG11
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9

[illegible][illegible]

```
LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG3
MOV AH,9
INT 21H
MOV AH,1
INT 21H
```

MOV AL,89H

MOV DX,0303H
OUT DX,AL

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG4
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG5
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,10100011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H

MOV AH,1
INT 21H

MOV AL,10011010B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00000101B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG9
MOV AH,9
INT 21H

```
S2:  LEA DX,CLRF
      MOV AH,9
      INT 21H
      LEA DX,CLRF
      MOV AH,9
      INT 21H
      LEA DX,CLRF
      MOV AH,9
      INT 21H
      LEA DX,CLRF
      MOV AH,9
      INT 21H
      LEA DX,CLRF
      MOV AH,9
      INT 21H
```

[illegible]

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG3
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,89H
MOV DX,0303H
OUT DX,AL

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG4
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG5
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,01101010B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,10101010B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00001100B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

[illegible]

INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG3
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,89H
MOV DX,0303H
OUT DX,AL

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG4
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG5
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,10010101B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG6
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,10101010B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG7
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00000011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG8
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG13
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG9
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,00110011B
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG11
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG10
MOV AH,9
INT 21H
MOV AH,1
INT 21H

MOV AL,DAT
MOV DX,0300H
OUT DX,AL

LEA DX,CLRF
MOV AH,9
INT 21H

LEA DX,MSG12
MOV AH,9
INT 21H
LEA DX,CLRF
MOV AH,9
INT 21H
LEA DX,MSG22
MOV AH,9
INT 21H

MOV AH,1
INT 21H
JMP EXIT

EXIT: MOV DX,0300H
MOV AL,00
OUT DX,AL

MOV AX,4C00H
INT 21H

CODE ENDS
END START

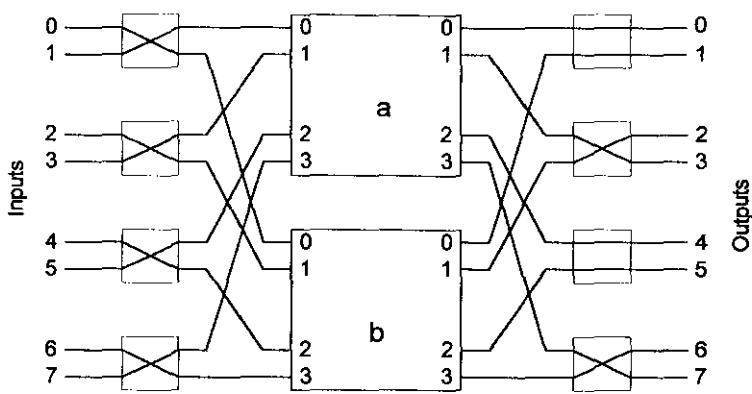
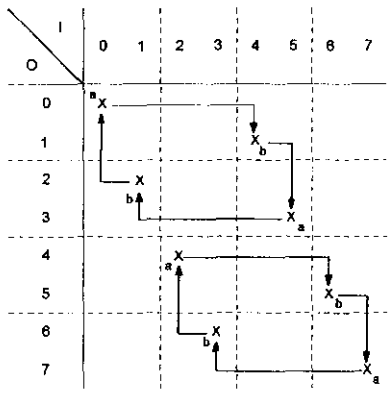
CHAPTER 4 :

TEST, EXPERIMENTS AND EQUIPMENT

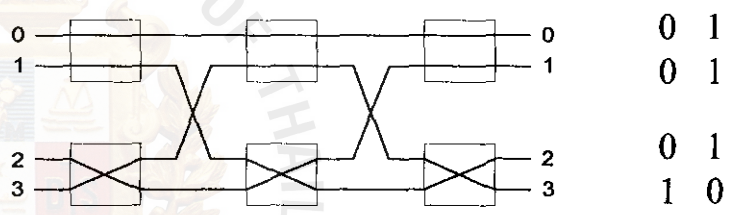
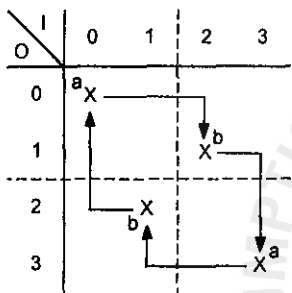


Perfect Shuffle

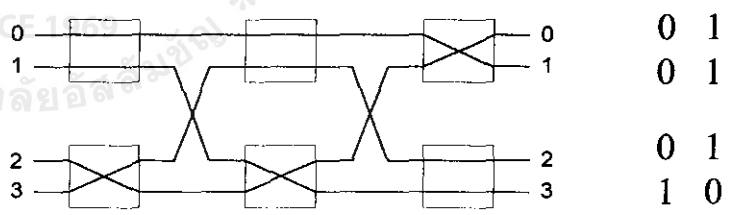
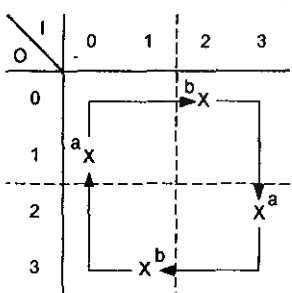
0 1 2 3 4 5 6 7
0 2 4 6 1 3 5 7



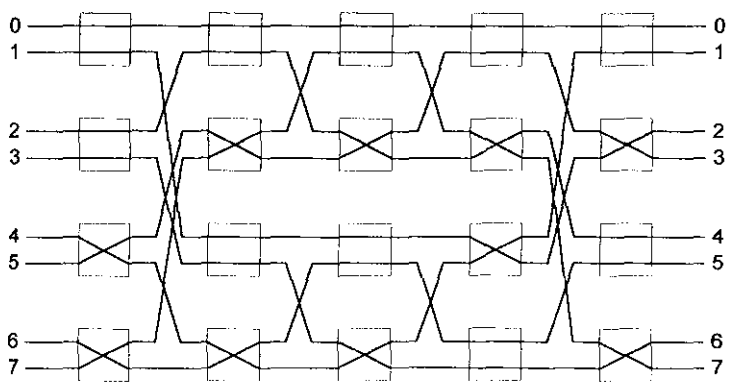
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0 2 1 3



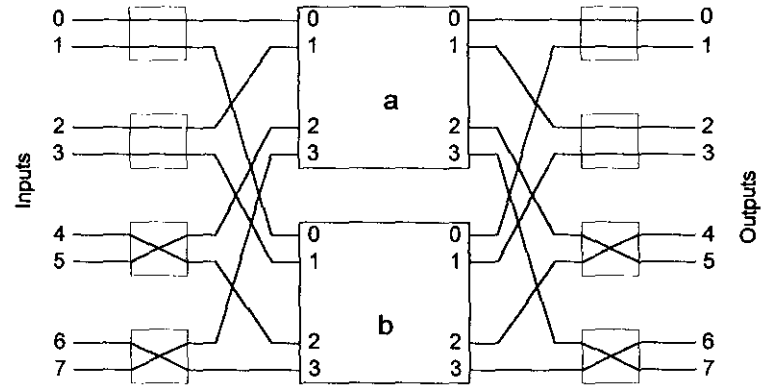
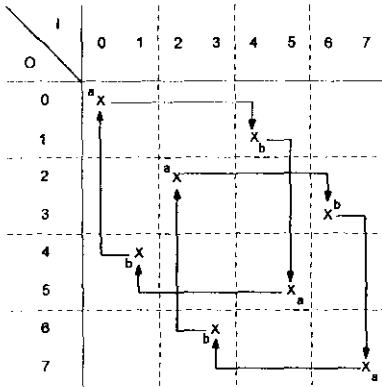
0 1 2 3
1 3 0 2



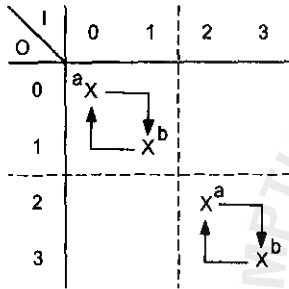
0	0	0	0	0
0	1	1	1	1
1	0	0	1	0
1	1	1	0	1



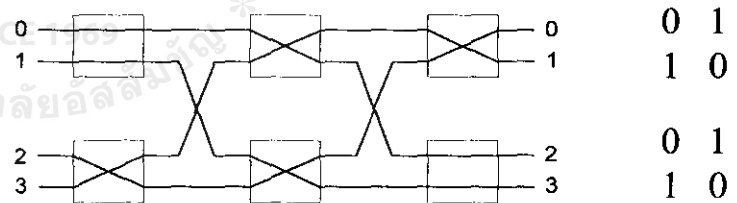
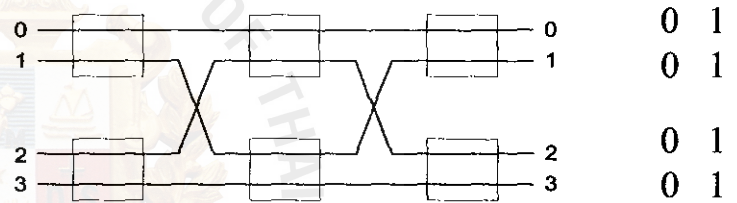
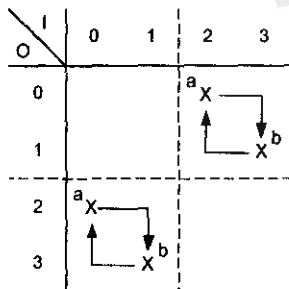
Bit Reversal
 0 1 2 3 4 5 6 7
 0 4 2 6 1 5 3 7



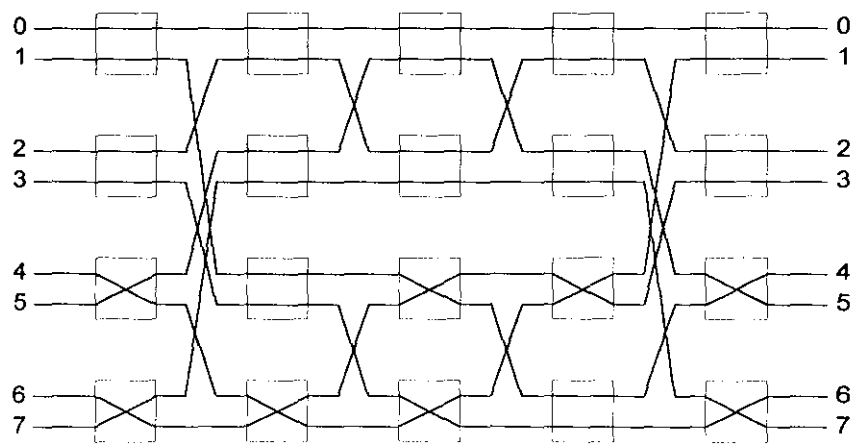
0 1 2 3
 0 1 2 3



0 1 2 3
 2 3 0 1



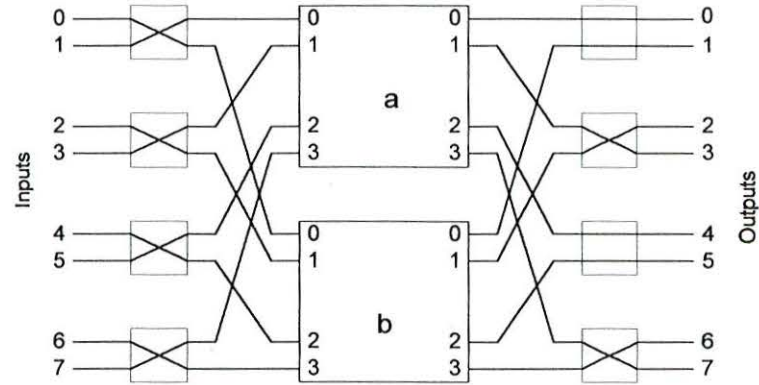
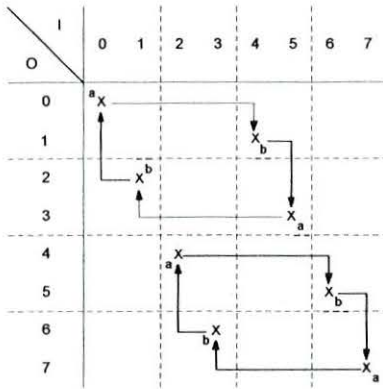
0 0 0 0 0
 0 0 0 0 0
 1 0 1 1 1
 1 1 1 0 1



SHIFT 1

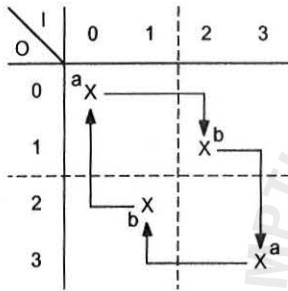
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0 2 4 6 1 3 5 7



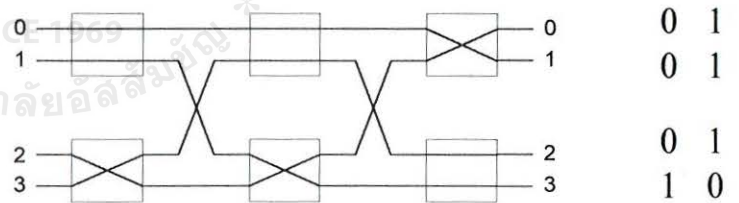
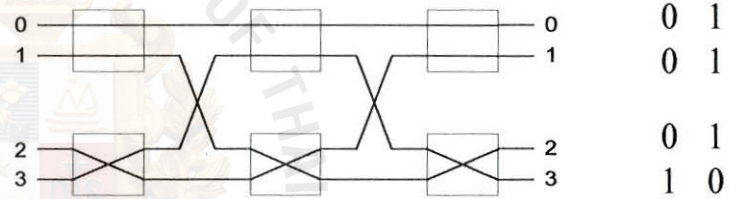
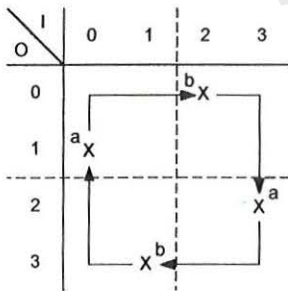
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0 2 1 3

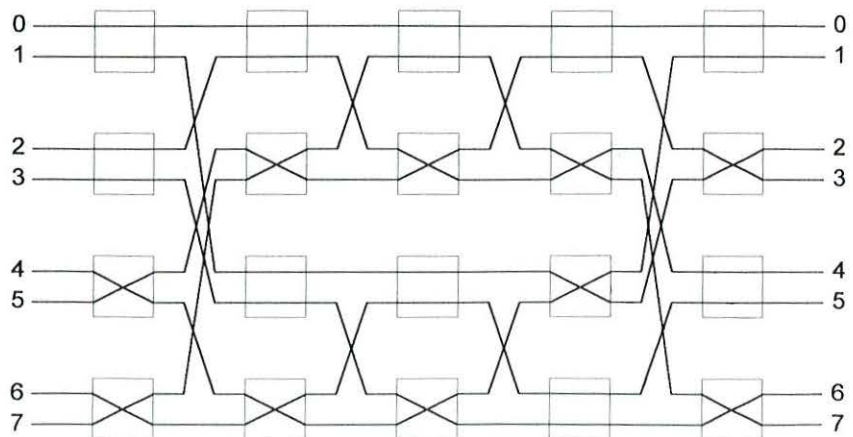


0 1 2 3

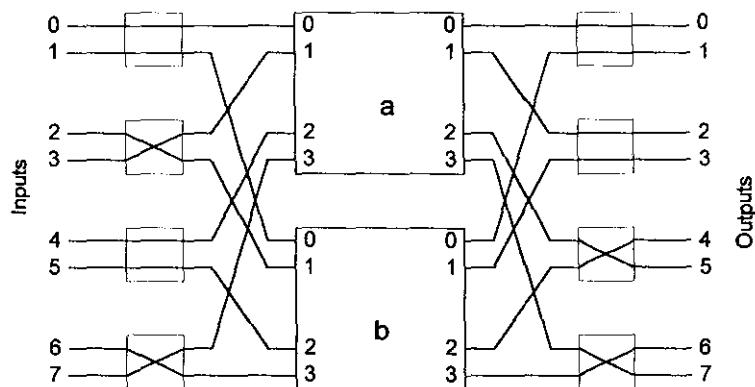
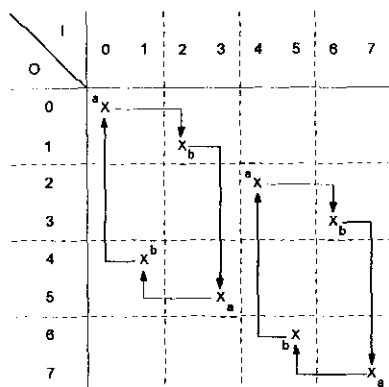
1 3 0 2



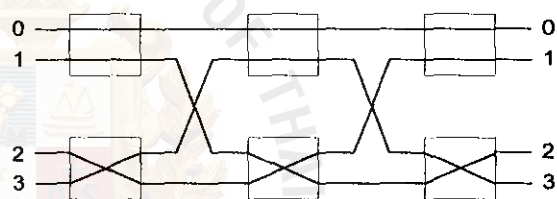
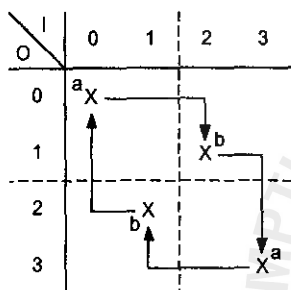
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1	1	1	0	1



SHIFT 2
0 1 2 3 4 5 6 7
0 4 1 5 2 6 3 7

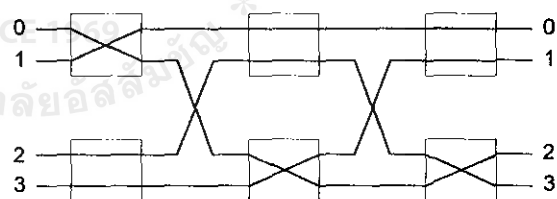
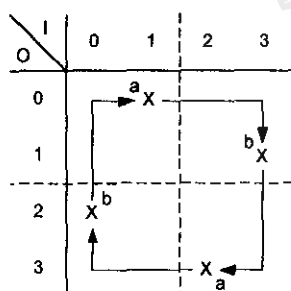


0 1 2 3
0 2 1 3



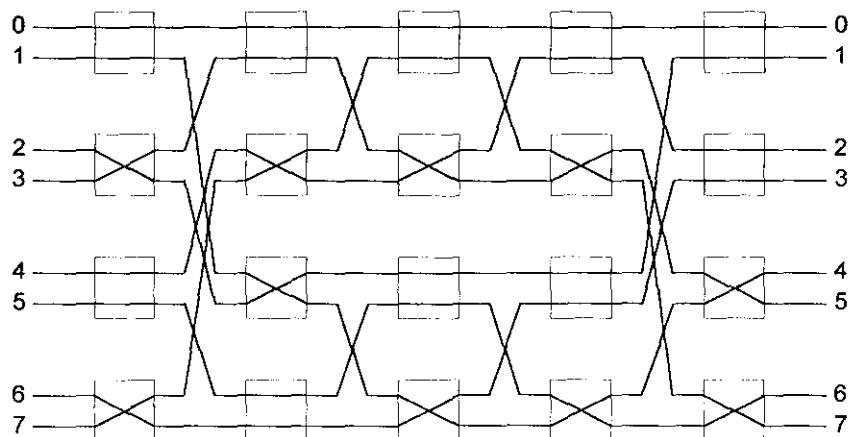
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0 1
0 1
1 0

0 1 2 3
2 0 3 1

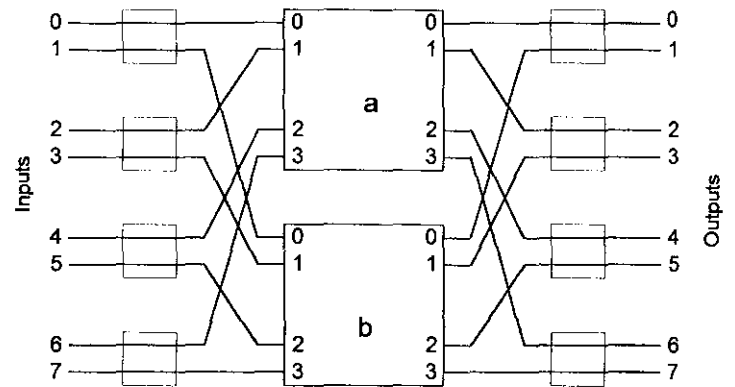
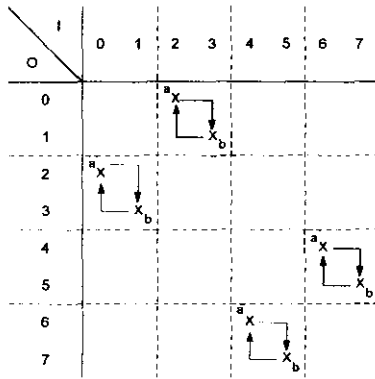


0 1
0 1
0 1
1 0

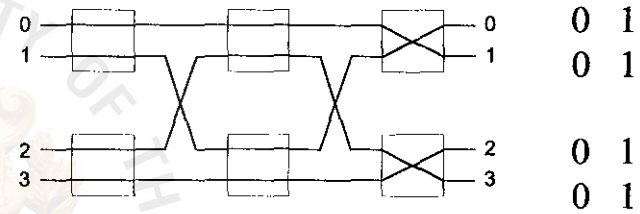
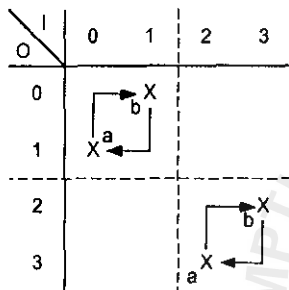
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1 1 1 1 0
0 1 0 0 1
1 0 1 1 1



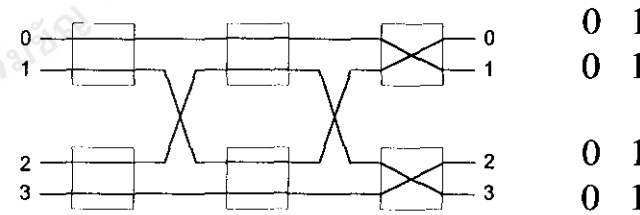
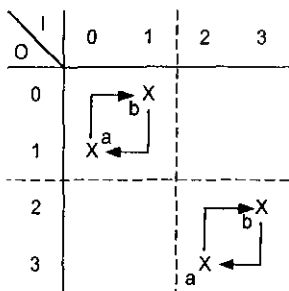
FLIP (010)
 0 1 2 3 4 5 6 7
 2 3 0 1 6 7 4 5



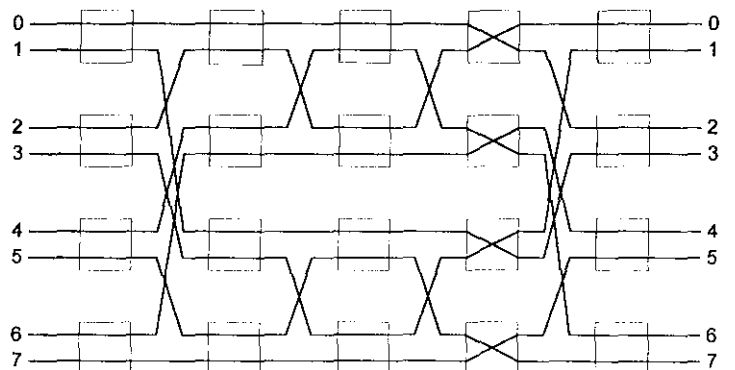
0 1 2 3
 1 0 3 2



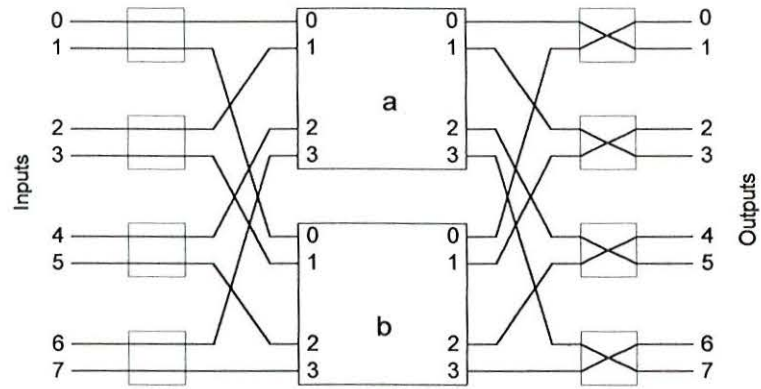
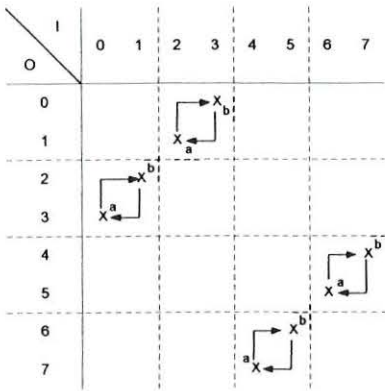
0 1 2 3
 1 0 3 2



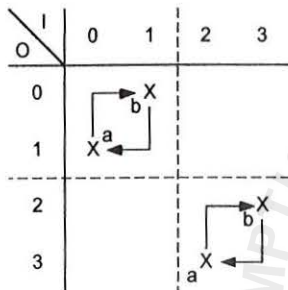
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 0 0 0 1 0



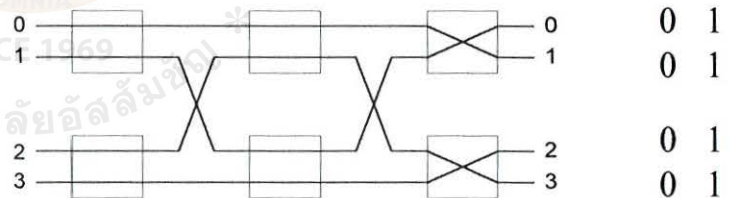
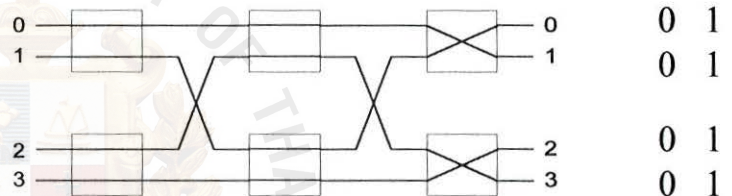
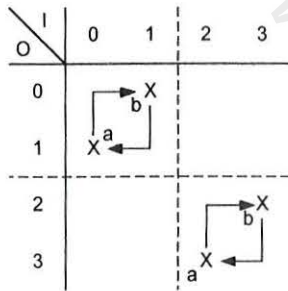
FLIP (011)
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 3 2 1 0 7 6 5 4



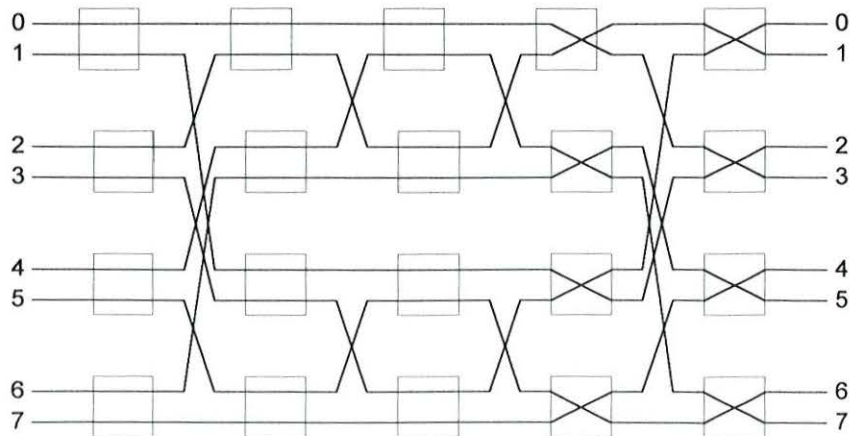
0 1 2 3
 1 0 3 2



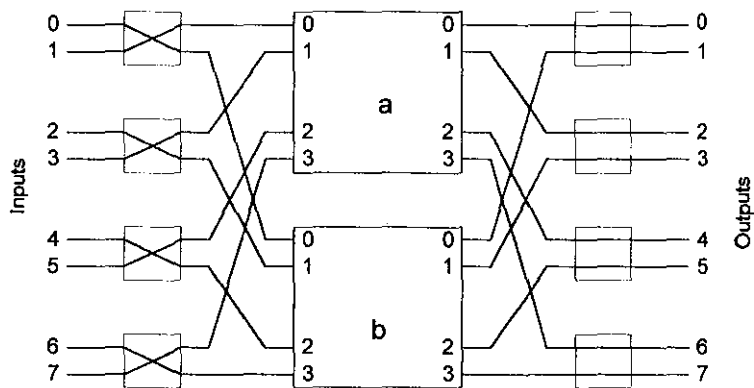
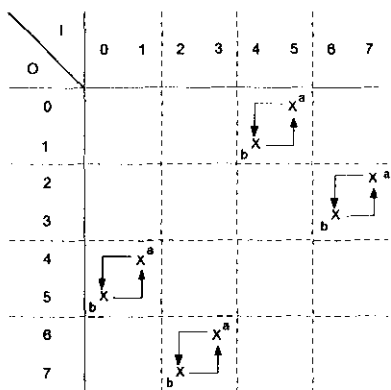
0 1 2 3
 1 0 3 2



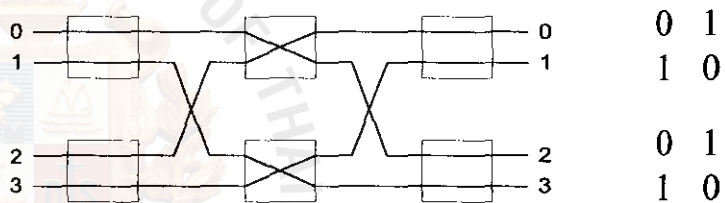
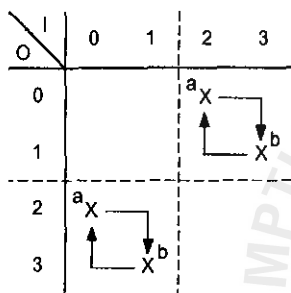
0 0 0 1 1
 0 0 0 1 1
 0 0 0 1 1
 0 0 0 1 1



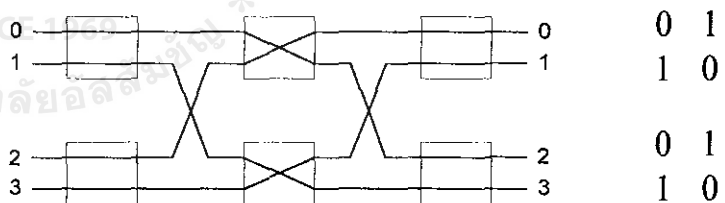
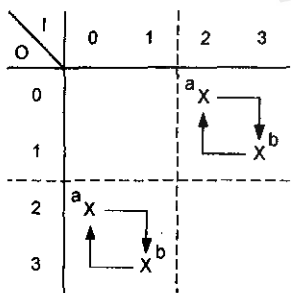
FLIP (101)
 0 1 2 3 4 5 6 7
 5 4 7 6 1 0 3 2



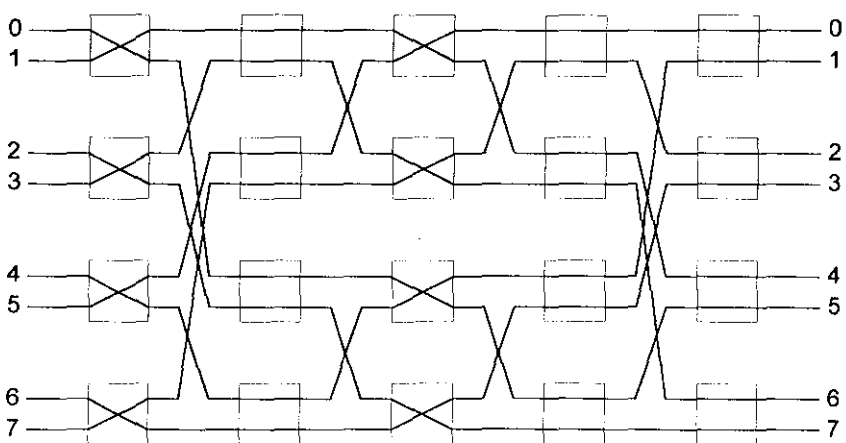
0 1 2 3
 2 3 0 1



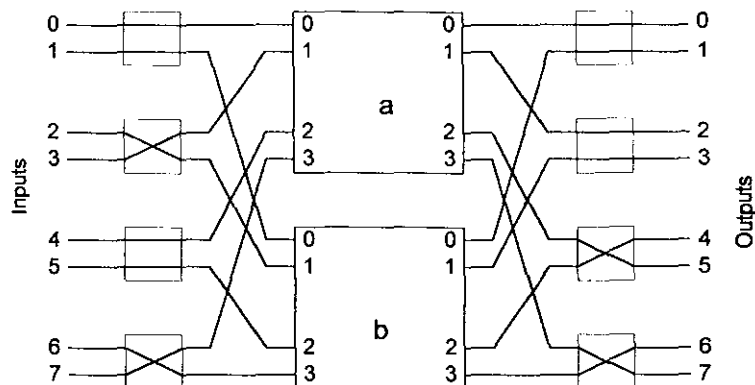
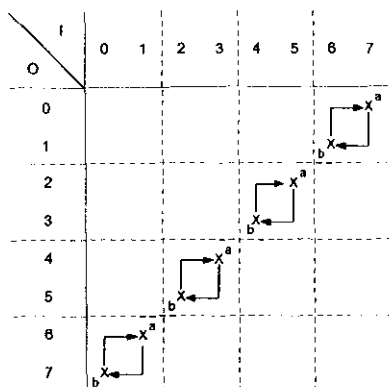
0 1 2 3
 2 3 0 1



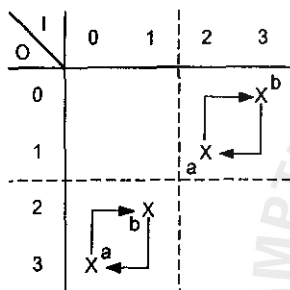
1	0	1	0	0
1	0	1	0	0
1	0	1	0	0
1	0	1	0	0



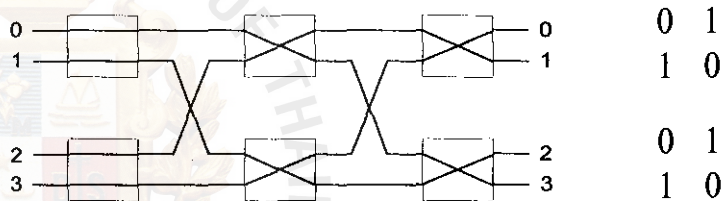
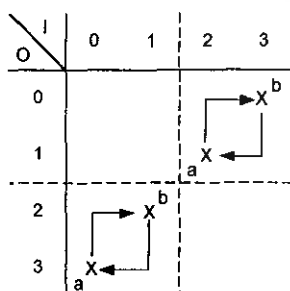
FLIP (111)
 0 1 2 3 4 5 6 7
 7 6 5 4 3 2 1 0



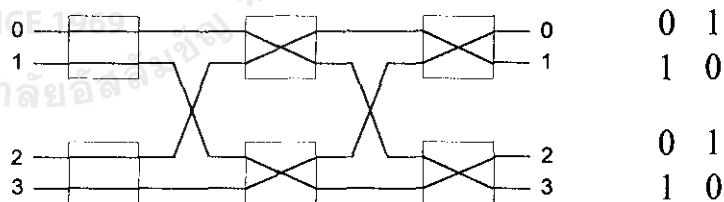
0 1 2 3
 3 2 1 0



0 1 2 3
 3 2 1 0

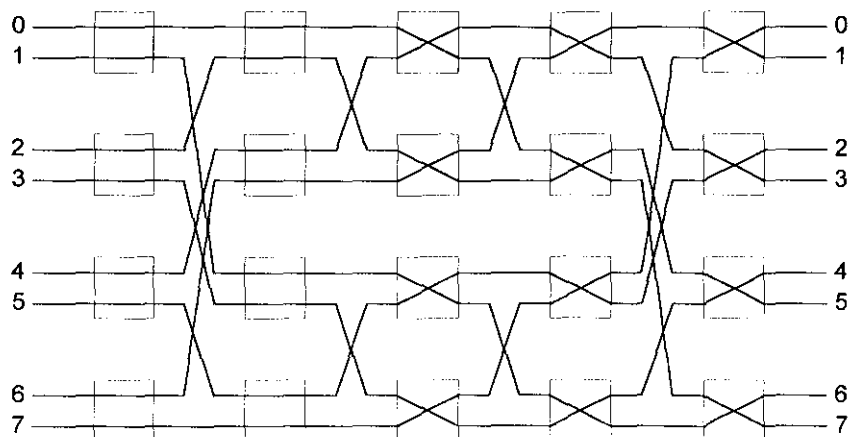


0 1
 1 0
 0 1
 1 0



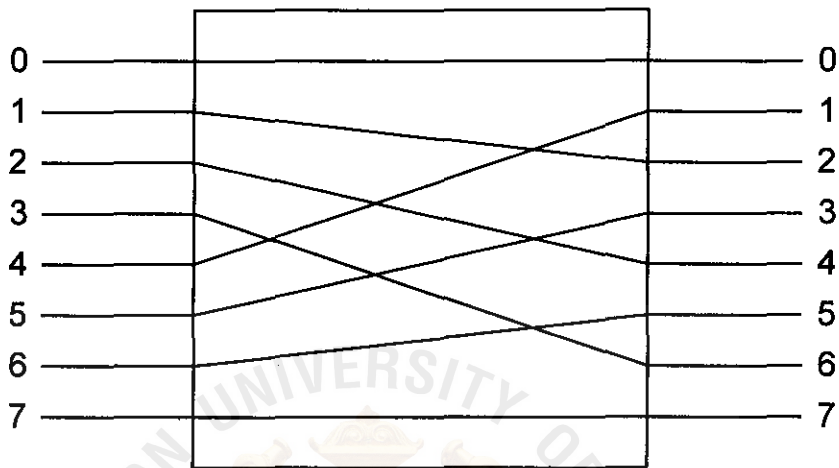
0 1
 1 0
 0 1
 1 0

0 0 1 1 1
 0 0 1 1 1
 0 0 1 1 1
 0 0 1 1 1



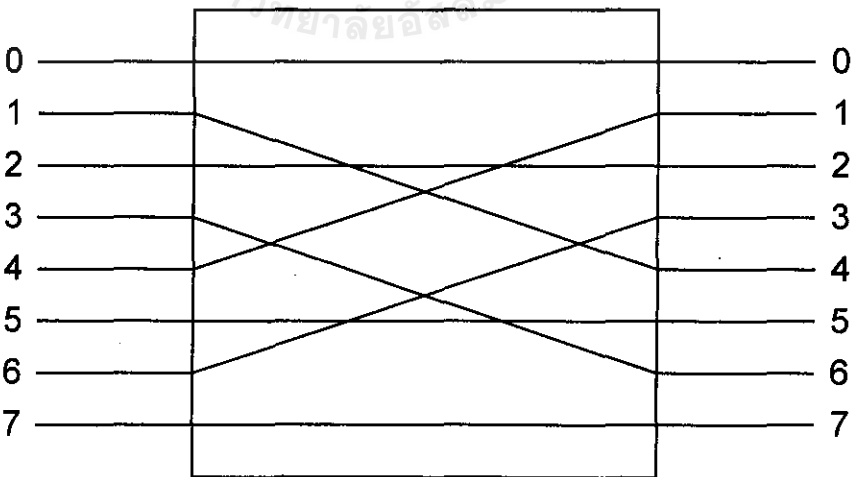
Perfect Shuffle

0 1 2 3 4 5 6 7
0 2 4 6 1 3 5 7



Bit Reversal

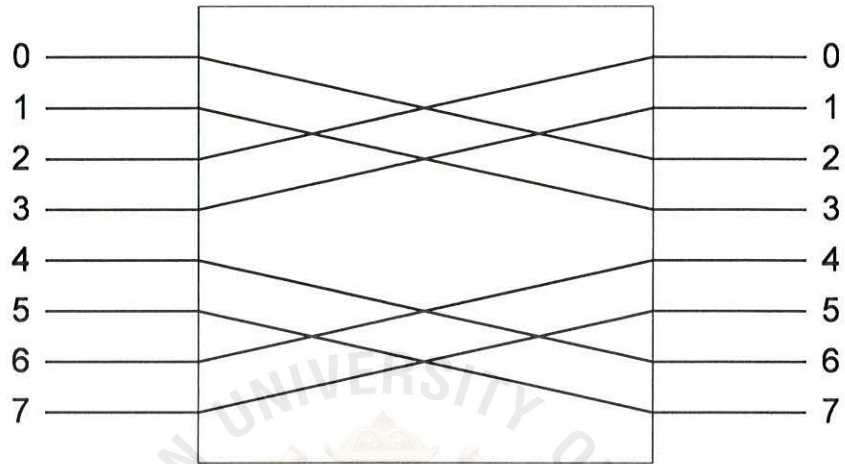
0 1 2 3 4 5 6 7
0 4 2 6 1 5 3 7



Flip Permutation (010)

0 1 2 3 4 5 6 7

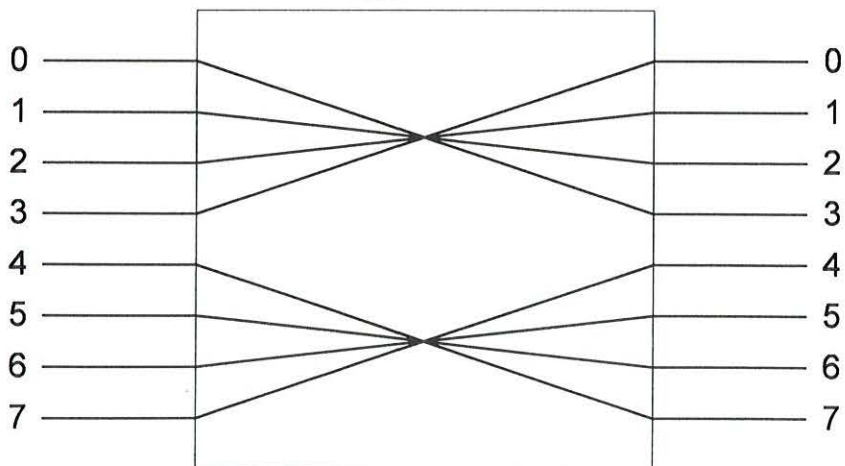
2 3 0 1 6 7 4 5



Flip Permutation (011)

0 1 2 3 4 5 6 7

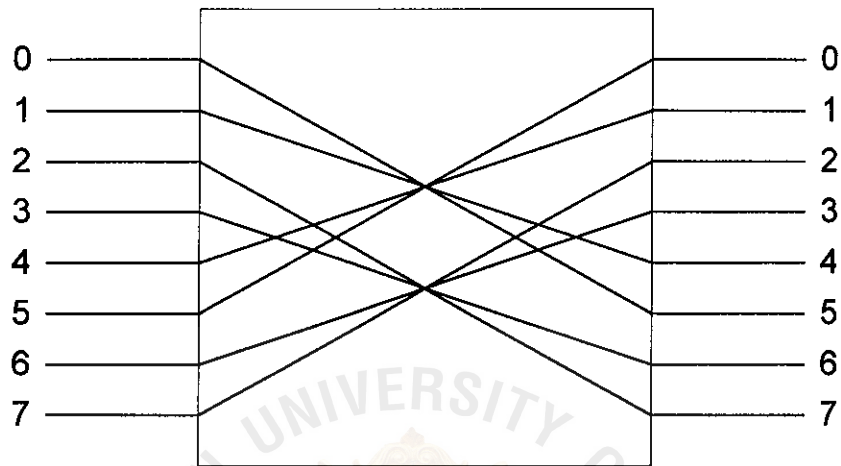
3 2 1 0 7 6 5 4



Flip Permutation (101)

0 1 2 3 4 5 6 7

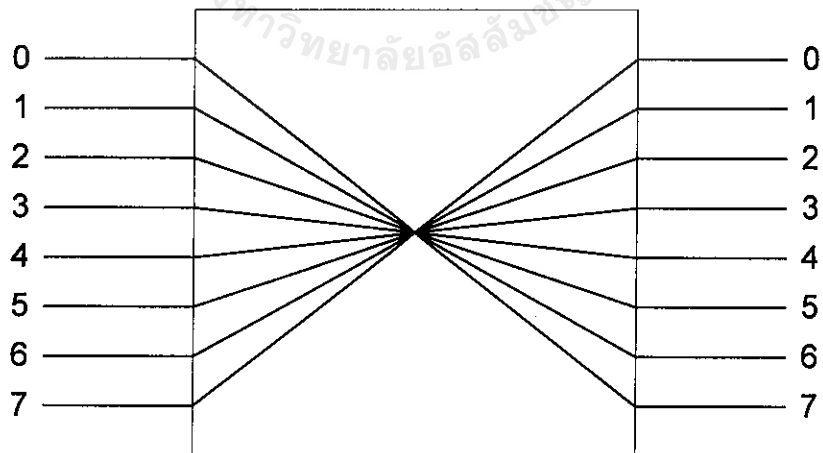
5 4 7 6 1 0 3 2



Flip Permutation (111)

0 1 2 3 4 5 6 7

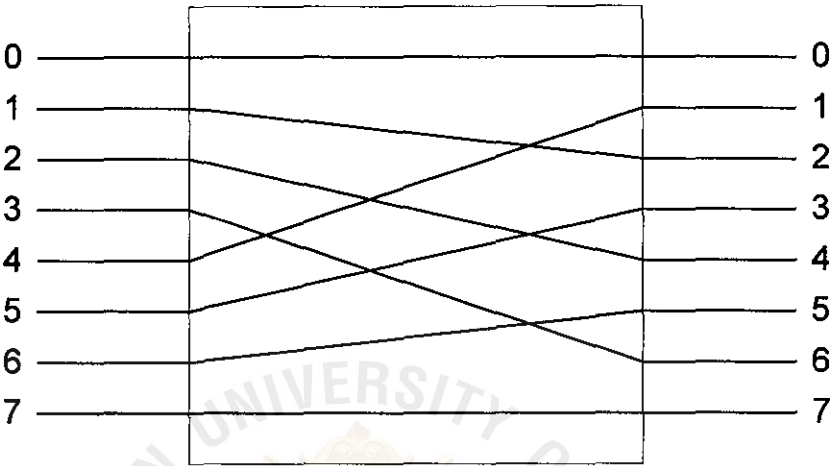
7 6 5 4 3 2 1 0



Cyclic Shift 1

0 1 2 3 4 5 6 7

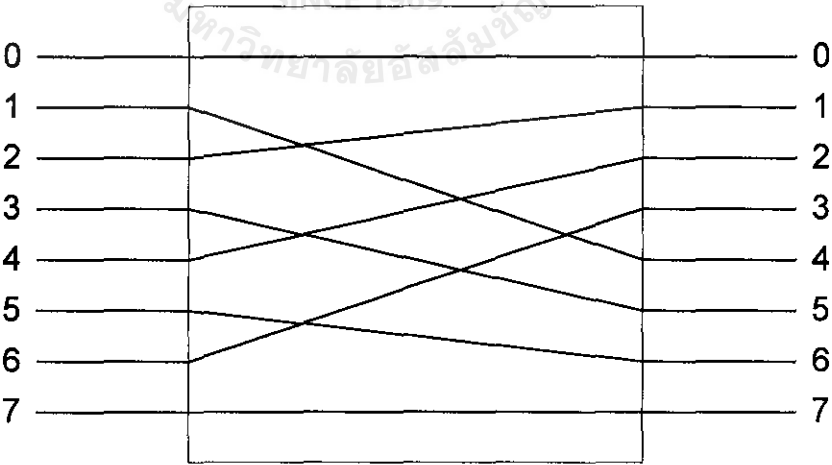
0 2 4 6 1 3 5 7



Cyclic Shift 2

0 1 2 3 4 5 6 7

0 4 1 5 2 6 3 7



The Equipment

1. 8255a Programmable Parallel Port	1
2. DIP Switches	6
3. 74LS04 Inverter gates	23
4. 74LS08 AND gates	20
5. 74LS32 OR gates	21
6. 74LS688 Comparators	4
7. 74LS373 Data Latches (8 bits)	9
8. 74LS155 Demultiplexers	9
9. 74LS157 Multiplexers	8
10. LEDs	16
11. Resistors 330 Ω	16
12. Resistors pack 10k Ω	6
13. ISA Card (for computer interface)	1



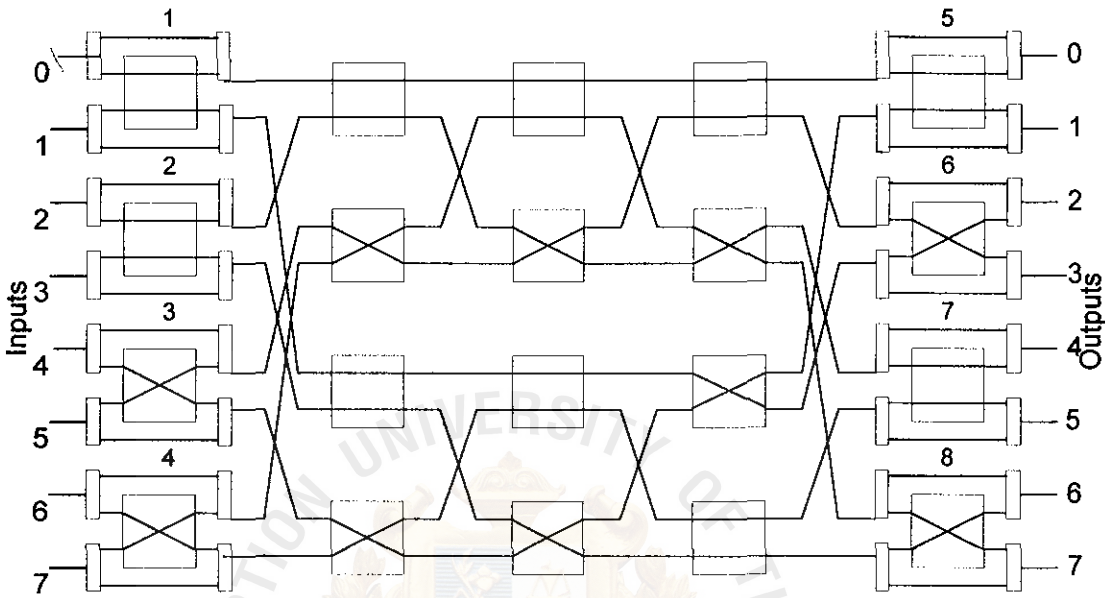
Fault – Tolerant in First and Last Stage



Perfect Shuffle

0 1 2 3 4 5 6 7

0 2 4 6 1 3 5 7

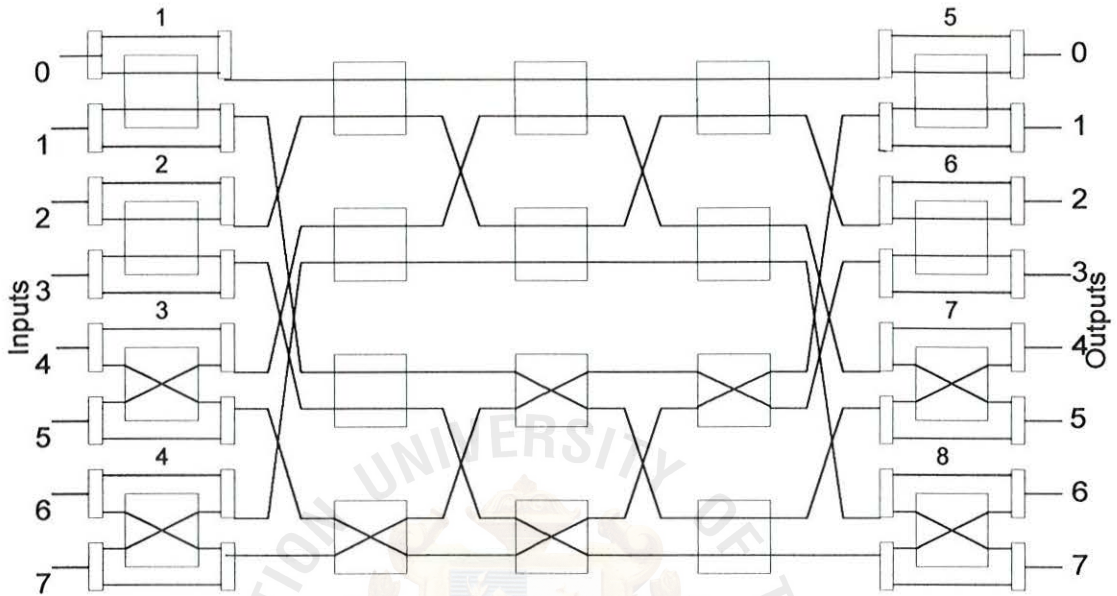


Switch No.	State
1	Straight
2	Straight
3	Exchange
4	Exchange
5	Straight
6	Exchange
7	Straight
8	exchange

Bit Reversal

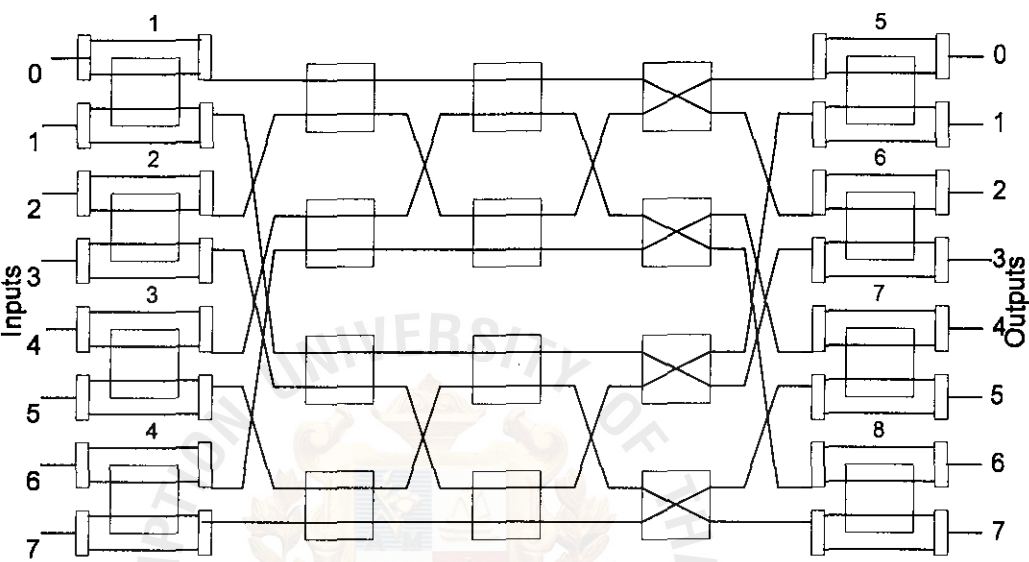
0 1 2 3 4 5 6 7

0 4 2 6 1 5 3 7



Switch No.	State
* 1	Straight
2	Straight
3	Exchange
4	Exchange
5	Straight
6	Straight
7	Exchange
8	Exchange

FLIP (010)
0 1 2 3 4 5 6 7
2 3 0 1 6 7 4 5

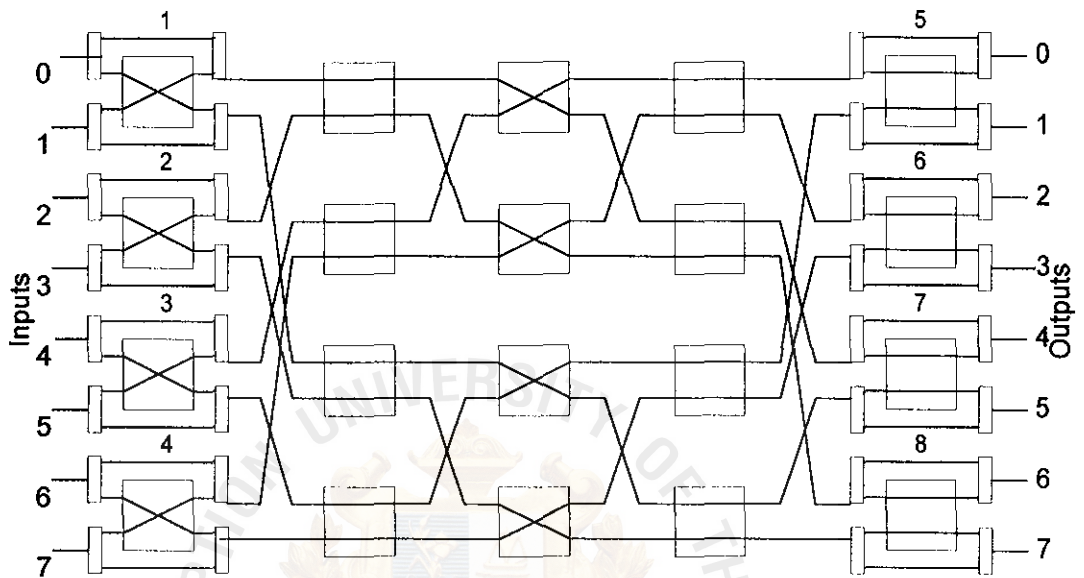


Switch No.	State
1	Straight
2	Straight
3	Straight
4	Straight
5	Straight
6	Straight
7	Straight
8	Straight

FLIP (101)

0 1 2 3 4 5 6 7

5 4 7 6 1 0 3 2

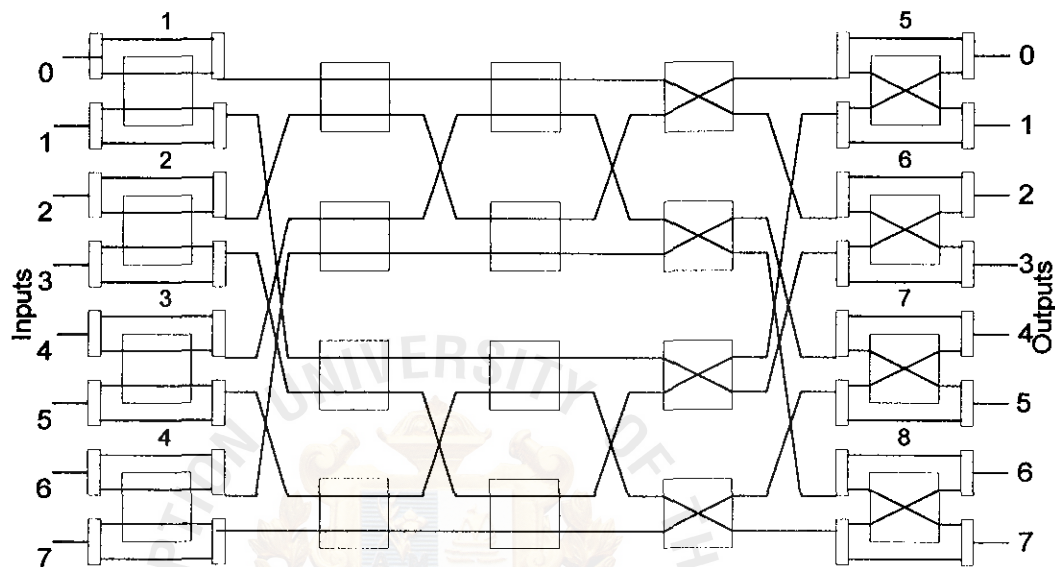


Switch No.	State
1	Exchange
2	Exchange
3	Exchange
4	Exchange
5	Straight
6	Straight
7	Straight
8	Straight

FLIP (011)

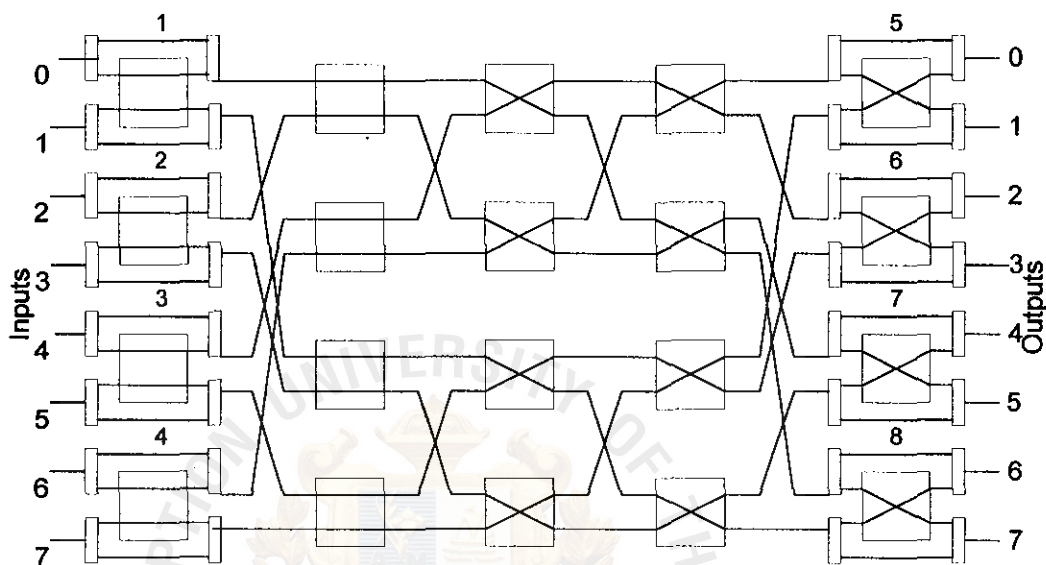
0 1 2 3 4 5 6 7

3 2 1 0 7 6 5 4



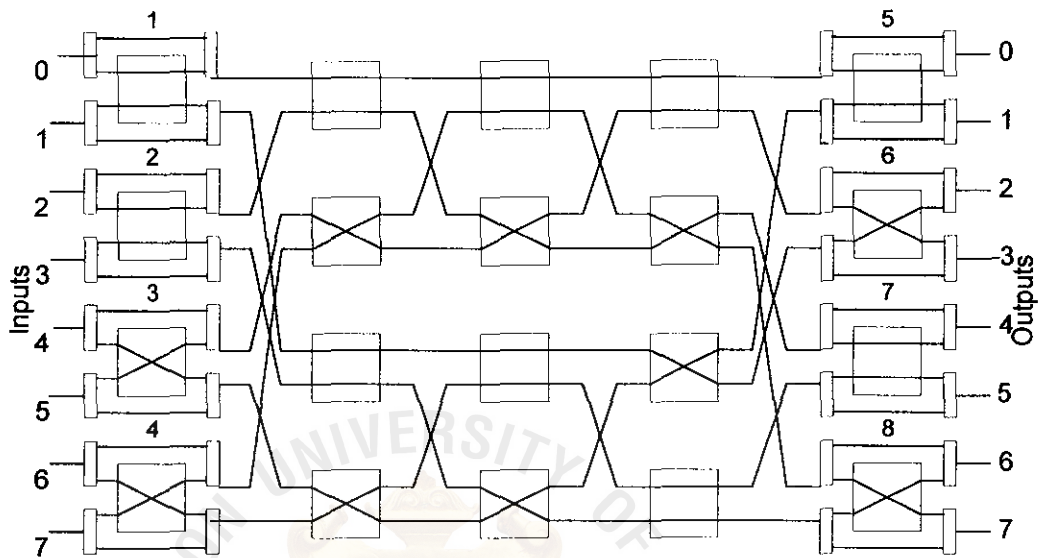
Switch No.	State
1	Straight
2	Straight
3	Straight
4	Straight
5	Exchange
6	Exchange
7	Exchange
8	Exchange

FLIP (111)
0 1 2 3 4 5 6 7
7 6 5 4 3 2 1 0



Switch No.	State
1	Straight
2	Straight
3	Straight
4	Straight
5	Exchange
6	Exchange
7	Exchange
8	Exchange

SHIFT 1
0 1 2 3 4 5 6 7
0 2 4 6 1 3 5 7

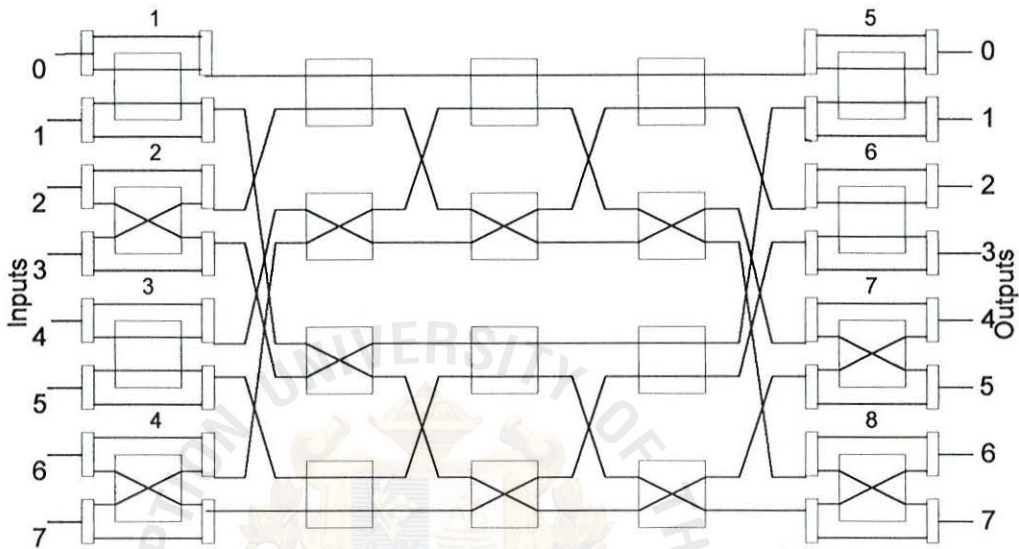


Switch No.	State
1	Straight
2	Straight
3	Exchange
4	Exchange
5	Straight
6	Exchange
7	Straight
8	Exchange

SHIFT 2

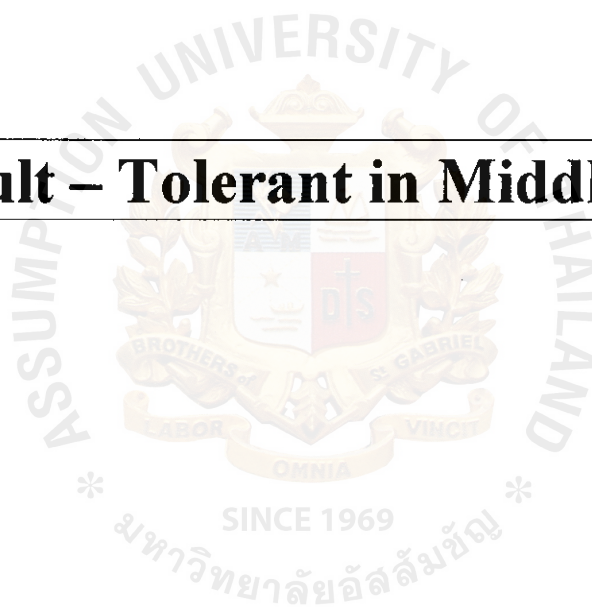
0 1 2 3 4 5 6 7

0 4 1 5 2 6 3 7



Switch No.	State
1	Straight
2	Exchange
3	Straight
4	Exchange
5	Straight
6	Straight
7	Exchange
8	Exchange

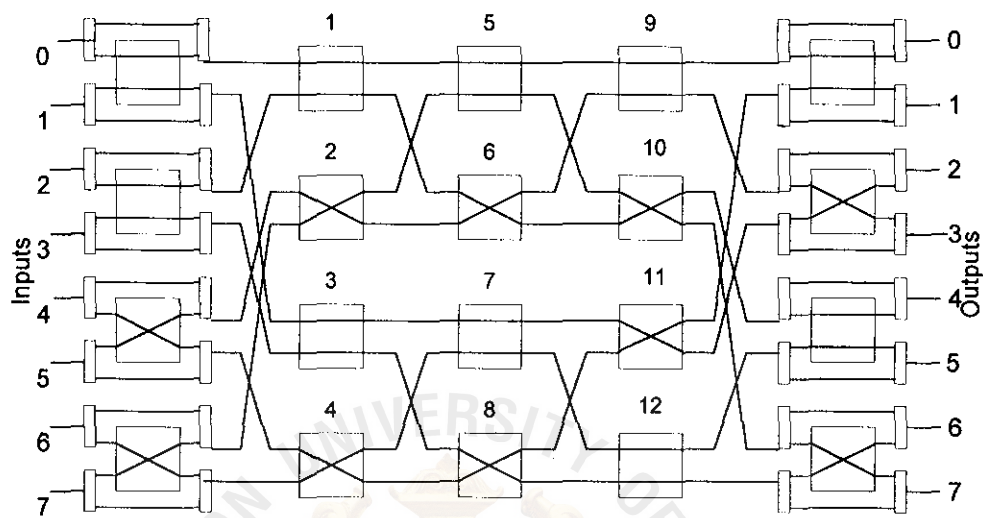
Fault – Tolerant in Middle Stage



Perfect Shuffle

0 1 2 3 4 5 6 7

0 2 4 6 1 3 5 7

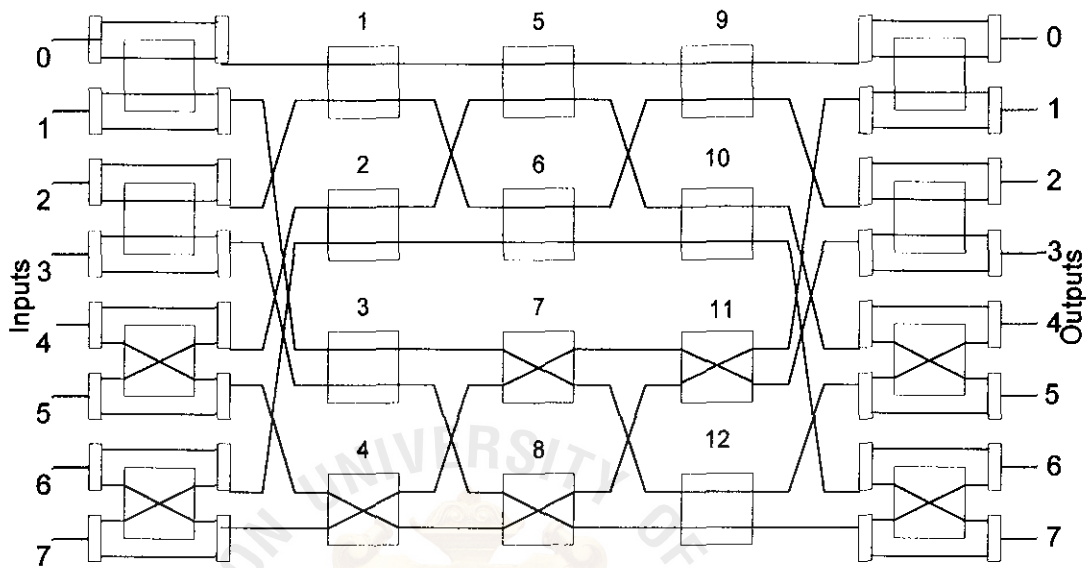


Fault on switch No.	Error on outputs
1	0, 4
2	3, 7
3	2, 6
4	1, 5
5	0, 7
6	3, 4
7	2, 5
8	6, 1
9	0, 3
10	4, 7
11	2, 1
12	5, 6

Bit Reversal

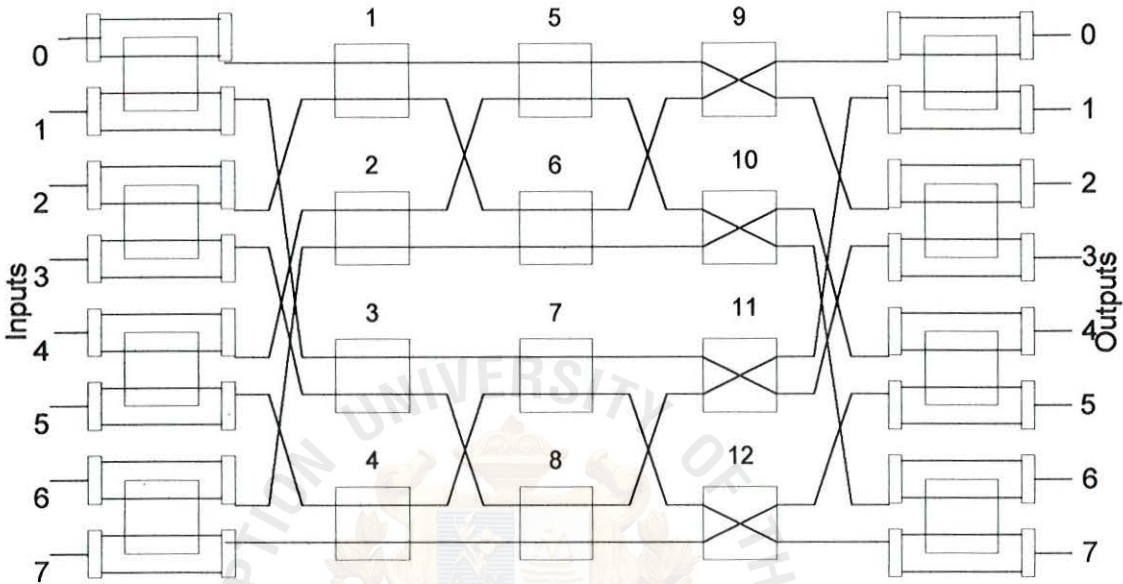
0 1 2 3 4 5 6 7

0 4 2 6 1 5 3 7



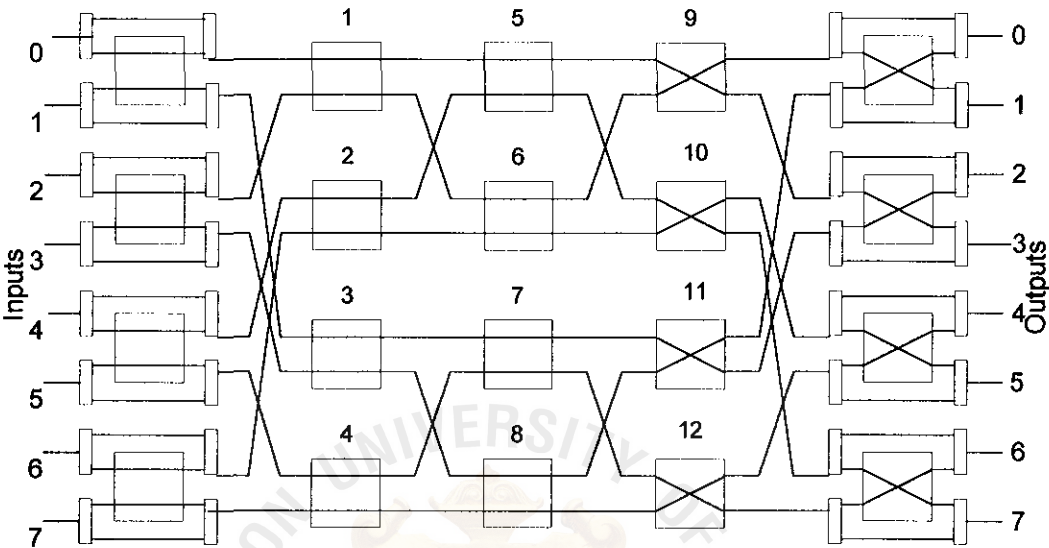
Fault on switch No.	Error on outputs
* 1	* 0, 2
2	5, 7
3	4, 6
4	1, 3
5	0, 5
6	2, 7
7	3, 4
8	1, 6
9	0, 2
10	5, 7
11	1, 3
12	4, 6

FLIP (010)
0 1 2 3 4 5 6 7
2 3 0 1 6 7 4 5



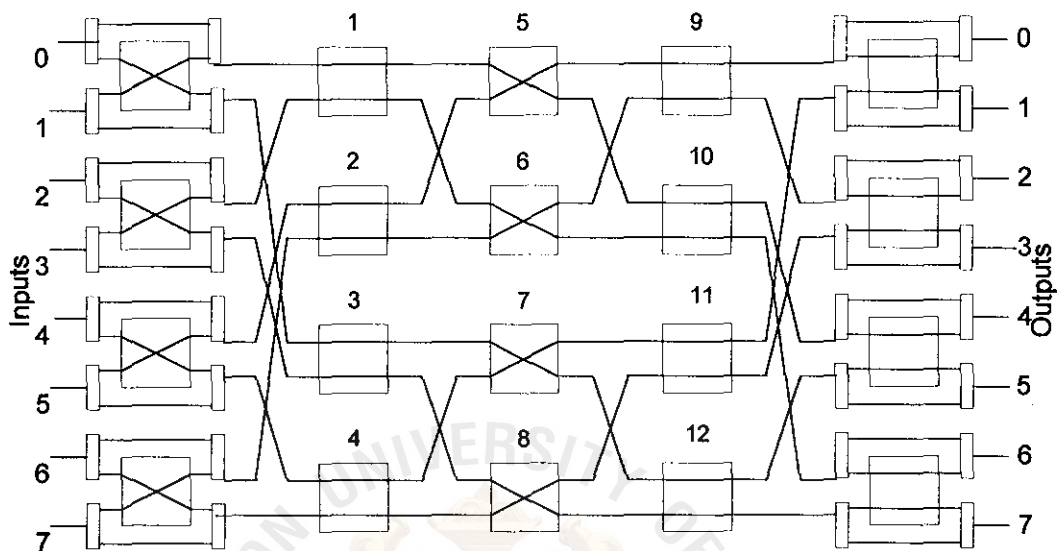
Fault on switch No.	Error on outputs
* 1	* 0, 2
2	4, 6
3	1, 3
4	5, 7
5	2, 6
6	0, 4
7	3, 7
8	1, 5
9	0, 2
10	4, 6
11	1, 3
12	5, 7

FLIP (011)
 0 1 2 3 4 5 6 7
 3 2 1 0 7 6 5 4



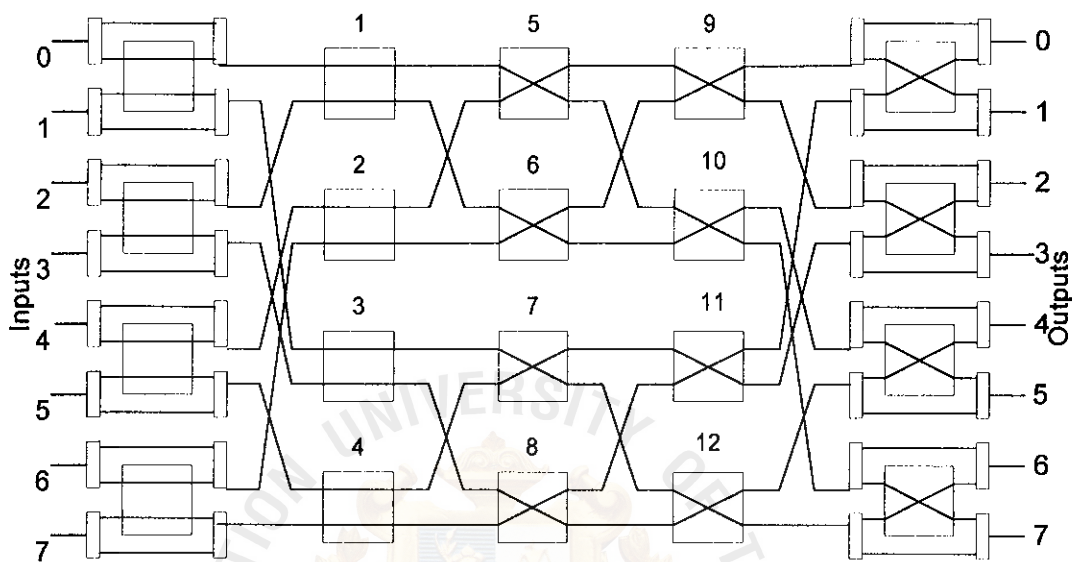
Fault on switch No.	Error on outputs
1	1, 3
2	5, 7
3	0, 2
4	4, 6
5	3, 7
6	1, 5
7	2, 6
8	0, 4
9	1, 3
10	5, 7
11	0, 2
12	4, 6

FLIP (101)
0 1 2 3 4 5 6 7
5 4 7 6 1 0 3 2



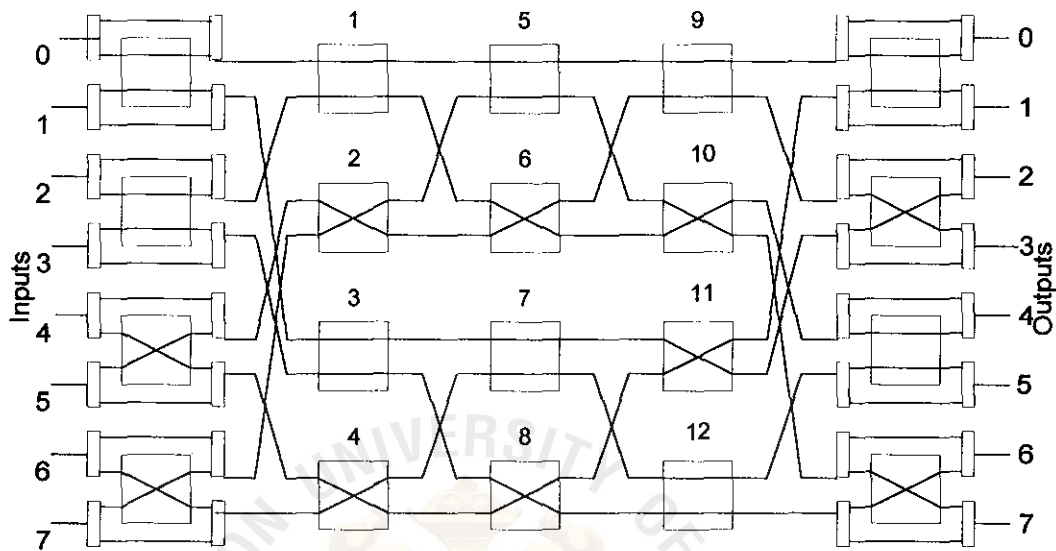
Fault on switch No.	Error on outputs
1	4, 6
2	0, 2
3	5, 7
4	1, 3
5	0, 4
6	2, 6
7	1, 5
8	3, 7
9	0, 2
10	4, 6
11	1, 3
12	5, 7

FLIP (111)
0 1 2 3 4 5 6 7
7 6 5 4 3 2 1 0



Fault on switch No.	Error on outputs
1	5, 7
2	1, 3
3	4, 6
4	0, 2
5	3, 7
6	1, 5
7	2, 6
8	0, 4
9	1, 3
10	5, 7
11	0, 2
12	4, 6

SHIFT 1
0 1 2 3 4 5 6 7
0 2 4 6 1 3 5 7

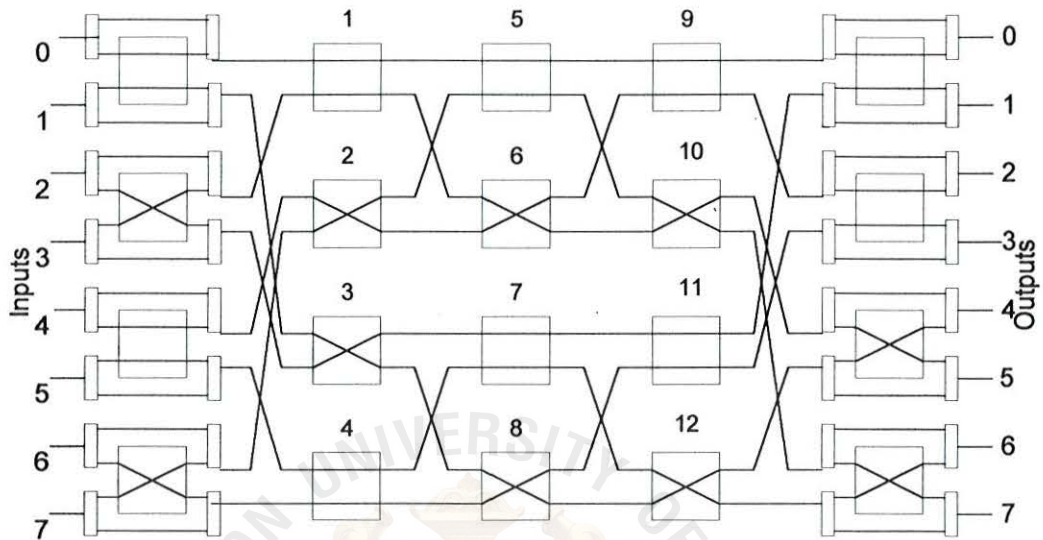


Fault on switch No.	Error on outputs
1	0, 4
* 2	* 3, 7
3	2, 6
4	1, 5
5	0, 7
6	3, 4
7	2, 5
8	1, 6
9	0, 3
10	4, 7
11	1, 2
12	5, 6

SHIFT 2

0 1 2 3 4 5 6 7

0 4 1 5 2 6 3 7



Fault on switch No.	Error on outputs
1	0, 5
2	2, 7
3	1, 4
4	3, 6
5	0, 7
6	2, 5
7	1, 6
8	3, 4
9	0, 2
10	5, 7
11	1, 3
12	4, 6

CHAPTER 5 :

CONCLUSION AND RECOMMENDATION



Conclusion and Recommendations

Conclusion:

In this project, we have successfully constructed a fault tolerant Benes network. The network is able to recover from not only the faulty switch, but also the wire connection in the network. The input data was able to reach the destination according to the chosen permutation request with and without inserting the fault.

The calculation program was able to function correctly according to the chosen permutation request and also the input data and shown the correct output. Also the programs written in assembly was able to control all the bypassing circuits and the switches which then produce the correct output with and without inserting the fault.

The eight bits of data which we assume that each bit represents a data packet were able to reach their destinations without blocking one another. There is always an alternate path for each data bits in case that one of the switch went down or broken, or there is an error in the link between two switches.

Recommendations:

After constructed the first Benes network (without the circuit on the ISA card) and tested the controls, we find that the latches (74LS373) can't latch the data inputting to it. We knew from A.Voraport that the wires we used to connect the addresses from the ISA card to the address decoder circuit have produced a lot of resistance and delay, so the chip select signal arrived slower than the data inputs which cause the data latches unable to latch the data inputs.

We have solved the problems by design a 8255a Programmable Parallel Port circuit as our data outputs, so the outputs will be latched on the 8255a output port. And we used two DIP Switches as our 16 bits addresses instead of the addresses from the ISA card. So each time we want to send controls to each latch, we have to manually set the DIP Switches to the address corespondent to the latch address.

After we connected the whole circuit to the computer and switch on, the computer hangs and shows the word "Divide overflow". We knew from Dr.Kittiphan that the output latch of the network has something wrong, and it outputs something to the computer and make the computer hang.

We have solved this problem by connected the outputs from the latch to the 8255a Programmable Parallel Port and wish to input the data to the computer via this IC. But for some reasons, the 8255a won't take the data into it's port although the data was there. So, we have to disconnect it from the 8255a and show the output on the Leds.

We have tested our programs and found out that when we use the program of the fault tolerant in the middle stage, we will get two outputs since we have to pass the data for two passes. So the correct output will not appear on the Leds. We have written a program to ask for the two outputs and the error bits, then calculate and show the correct output on the computer screen instead.

In this project, we didn't have time to write another program to check for the faulty switch on it own without asking the user. It is possible to do so, if we send first the testing data through the network with a certain permutation request and then check the output data to find the faulty switch. But in the real world, each switch will have a protocol, and when one switch is broken, the switches connected to it will know that there is a fault, and it will automatically send the data packet through an alternate path.

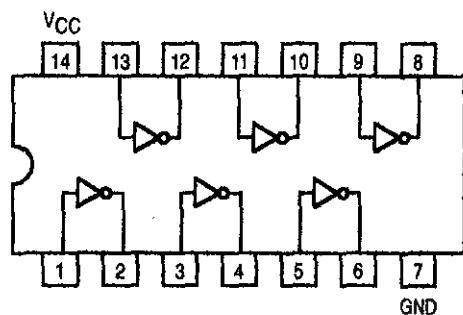
The program written in assembly is very long since we didn't write it in looped form, but we use copy/paste method instead.

APPENDIX



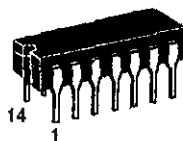


HEX INVERTER



SN54/74LS04

HEX INVERTER
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
IOH	Output Current — High	54, 74			-0.4	mA
IOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	$V_{CC} = \text{MIN}$, $I_{IN} = -18 \text{ mA}$
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	$V_{CC} = \text{MIN}$, $I_{OH} = \text{MAX}$, $V_{IN} = V_{IH}$ or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = V_{CC \text{ MIN}}$, $V_{IN} = V_{IL}$ or V_{IH} per Truth Table
		74		0.35	0.5	V	$I_{OL} = 8.0 \text{ mA}$
I_{IH}	Input HIGH Current				20	μA	$V_{CC} = \text{MAX}$, $V_{IN} = 2.7 \text{ V}$
					0.1	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 7.0 \text{ V}$
I_{IL}	Input LOW Current				-0.4	mA	$V_{CC} = \text{MAX}$, $V_{IN} = 0.4 \text{ V}$
I_{OS}	Short Circuit Current (Note 1)		-20		-100	mA	$V_{CC} = \text{MAX}$
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW				2.4	mA	$V_{CC} = \text{MAX}$
					6.6		

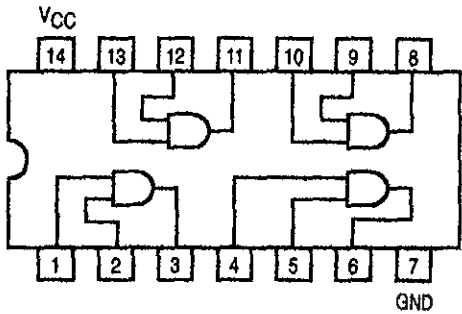
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{LH}	Turn-Off Delay, Input to Output		9.0	15	ns	$V_{CC} = 5.0 \text{ V}$ $C_L = 15 \text{ pF}$
t_{HL}	Turn-On Delay, Input to Output		10	15	ns	



QUAD 2-INPUT AND GATE

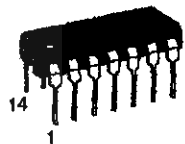


SN54/74LS08

QUAD 2-INPUT AND GATE
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ Ceramic
SN74LSXXN Plastic
SN74LSXXD SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
VCC	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
TA	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
IOH	Output Current — High	54, 74			-0.4	mA
IOL	Output Current — Low	54			4.0	mA
		74			8.0	

SN54/74LS08

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions
			Min	Typ	Max		
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table
		74	2.7	3.5		V	
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA
		74		0.35	0.5	V	I _{OL} = 8.0 mA
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _L	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
OS	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX
I _{CC}	Power Supply Current Total, Output HIGH				4.8	mA	V _{CC} = MAX
	Total, Output LOW				8.8		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{LH}	Turn-Off Delay, Input to Output		8.0	15	ns	V _{CC} = 5.0 V C _L = 15 pF
t _{HL}	Turn-On Delay, Input to Output		10	20	ns	

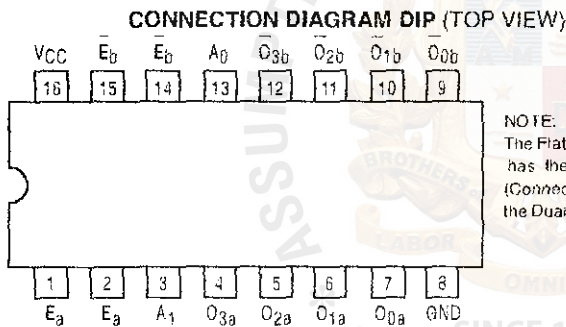


DUAL 1-OF-4 DECODER/ DEMULTIPLEXER

The SN54/74LS155 and SN54/74LS156 are high speed Dual 1-of-4 Decoder/Demultiplexers. These devices have two decoders with common 2-bit Address inputs and separate gated Enable inputs. Decoder "a" has an Enable gate with one active HIGH and one active LOW input. Decoder "b" has two active LOW Enable inputs. If the Enable functions are satisfied, one output of each decoder will be LOW as selected by the address inputs. The LS156 has open collector outputs for wired-OR (DOT-AND) decoding and function generator applications.

The LS155 and LS156 are fabricated with the Schottky barrier diode process for high speed and are completely compatible with all Motorola TTL families.

- Schottky Process for High Speed
- Multifunction Capability
- Common Address Inputs
- True or Complement Data Demultiplexing
- Input Clamp Diodes Limit High Speed Termination Effects
- ESD > 3500 Volts



PIN NAMES

A ₀ , A ₁	Address Inputs
E _a , E _b	Enable (Active LOW) Inputs
E _a	Enable (Active HIGH) Input
O ₀ -O ₃	Active LOW Outputs (Note b)

NOTES:

a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The HIGH level drive for the LS156 must be established by an external resistor.

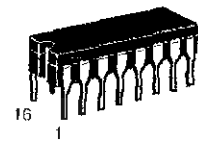
LOADING (Note a)

HIGH	LOW
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
10 U.L.	5 (2.5) U.L.

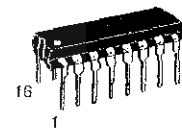
**SN54/74LS155
SN54/74LS156**

**DUAL 1-OF-4 DECODER/
DEMULTIPLEXER**

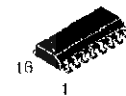
**LS156-OPEN-COLLECTOR
LOW POWER SCHOTTKY**



**J SUFFIX
CERAMIC
CASE 620-09**



**N SUFFIX
PLASTIC
CASE 648-08**

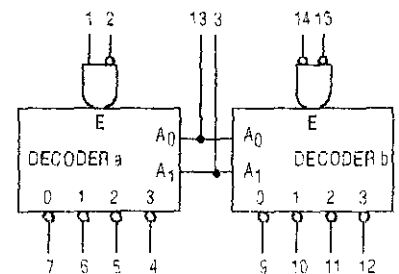


**D SUFFIX
SOIC
CASE 751B-03**

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

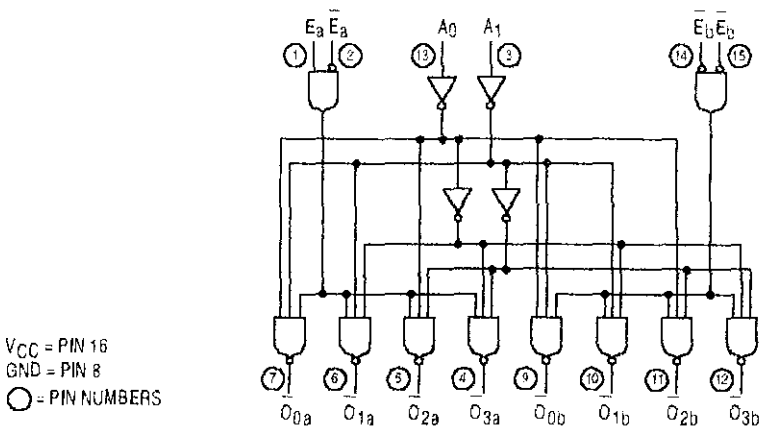
LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

SN54/74LS155 • SN54/74LS156

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The LS155 and LS156 are Dual 1-of-4 Decoder/Demultiplexers with common Address inputs and separate gated Enable inputs. When enabled, each decoder section accepts the binary weighted Address inputs (A_0, A_1) and provides four mutually exclusive active LOW outputs (O_0-O_3). If the Enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

Each decoder section has a 2-input enable gate. The enable gate for Decoder "a" requires one active HIGH input and one active LOW input ($E_a \cdot \bar{E}_a$). In demultiplexing applications, Decoder "a" can accept either true or complemented data by using the E_a or $\bar{E}_a$ inputs respectively. The enable gate for Decoder "b" requires two active LOW inputs ($\bar{E}_b \cdot E_b$). The LS155 or LS156 can be used as a 1-of-8 Decoder/Demultiplexer by tying E_a to E_b and relabeling the common connection as (A_2). The other E_b and E_a are connected together to form the common enable.

The LS155 and LS156 can be used to generate all four minterms of two variables. These four minterms are useful in some applications replacing multiple gate functions as shown in Fig. a. The LS156 has the further advantage of being able to

AND the minterm functions by tying outputs together. Any number of terms can be wired-AND as shown below.

$$f = (E_a + A_0 + A_1) \cdot (E_a + A_0 + A_1) \cdot (E_a + A_0 + A_1) \cdot (E_a + A_0 + A_1)$$

$$\text{where } E = E_a + E_a; E = E_b + E_b$$

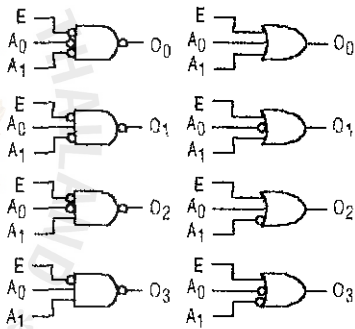


Figure a

TRUTH TABLE

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A_0	A_1	E_a	$\bar{E}_a$	O_0	O_1	O_2	O_3	E_b	$\bar{E}_b$	O_0	O_1	O_2	O_3
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

SN54/74LS155

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
VCC	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
TA	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
IOH	Output Current — High	54, 74			-0.4	mA
IOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
VIH	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
VIL	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
VIK	Input Clamp Diode Voltage		-0.65	-1.5	V	VCC = MIN, IIN = -18 mA
VOH	Output HIGH Voltage	54	2.5	3.5	V	VCC = MIN, IOH = MAX, VIN = VIH or VIL per Truth Table
		74	2.7	3.5	V	
VOL	Output LOW Voltage	54, 74	0.25	0.4	V	IOL = 4.0 mA
		74	0.35	0.5	V	IOL = 8.0 mA
IIH	Input HIGH Current			20	µA	VCC = MAX, VIN = 2.7 V
				0.1	mA	VCC = MAX, VIN = 7.0 V
IIL	Input LOW Current			-0.4	mA	VCC = MAX, VIN = 0.4 V
IOS	Short Circuit Current (Note 1)	-20		-100	mA	VCC = MAX
ICC	Power Supply Current			10	mA	VCC = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (TA = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
tPLH tPHL	Propagation Delay Address, Ea or Eb to Output		10 19	15 30	ns	VCC = 5.0 V CL = 15 pF
tPLH tPHL	Propagation Delay Address to Output		17 19	26 30	ns	
tPLH tPHL	Propagation Delay Ea to Output		18 18	27 27	ns	

AC WAVEFORMS

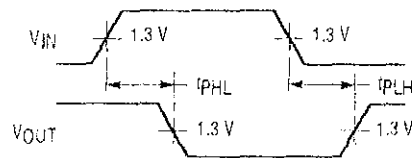


Figure 1

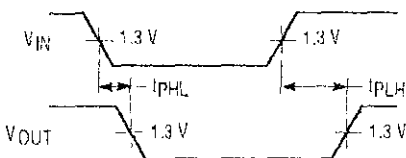


Figure 2

SN54/74LS156

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
V _{OH}	Output Voltage — High	54, 74			5.5	V
I _{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA
I _{OH}	Output HIGH Current	54, 74		100	μA	V _{CC} = MIN, V _{OH} = MAX
V _{OL}	Output LOW Voltage	54, 74	0.25	0.4	V	I _{OL} = 4.0 mA V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74	0.35	0.5	V	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current			-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V
I _{CC}	Power Supply Current			10	mA	V _{CC} = MAX

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay Address, E _A or E _B to Output		25 34	40 51	ns	Figure 1
t _{PLH} t _{PHL}	Propagation Delay Address to Output		31 34	46 51	ns	Figure 2
t _{PLH} t _{PHL}	Propagation Delay E _A to Output		32 32	48 48	ns	Figure 1

AC WAVEFORMS

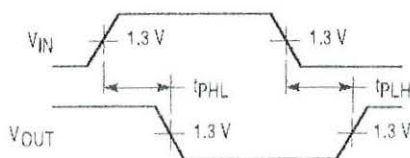


Figure 1

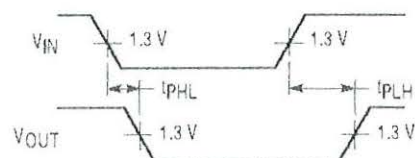


Figure 2

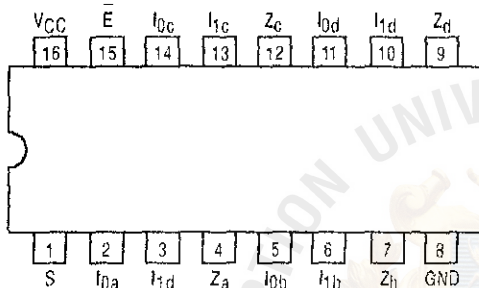


QUAD 2-INPUT MULTIPLEXER

The LSTTL/MSI SN54/74LS157 is a high speed Quad 2-Input Multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four buffered outputs present the selected data in the true (non-inverted) form. The LS157 can also be used to generate any four of the 16 different functions of two variables. The LS157 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Schottky Process for High Speed
- Multifunction Capability
- Non-Inverting Outputs
- Input Clamp Diodes Limit High Speed Termination Effects
- Special Circuitry Ensures Glitch Free Multiplexing
- ESD > 3500 Volts

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

S	Common Select Input
E	Enable (Active LOW) Input
I0a-I0d	Data Inputs from Source 0
I1a-I1d	Data Inputs from Source 1
Za-Zd	Multiplexer Outputs (Note b)

LOADING (Note a)

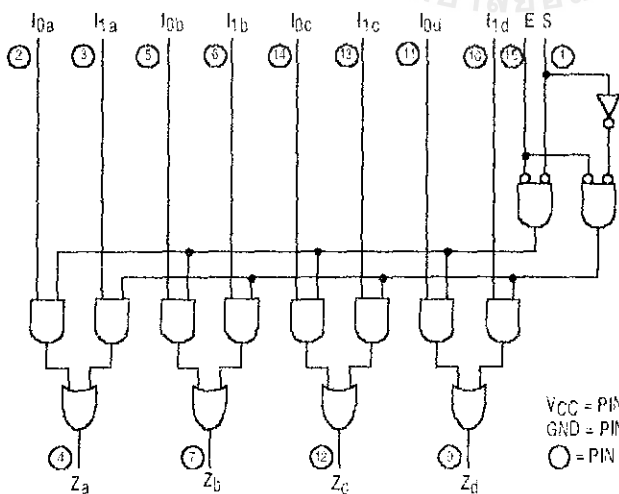
	HIGH	LOW
I0a-I0d	1.0 U.L.	0.5 U.L.
I1a-I1d	1.0 U.L.	0.5 U.L.
I0a-I0d	0.5 U.L.	0.25 U.L.
I1a-I1d	0.5 U.L.	0.25 U.L.
Za-Zd	10 U.L.	5 (2.5) U.L.

NOTES:

a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.

b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

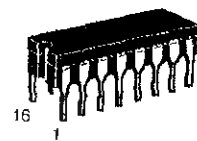
LOGIC DIAGRAM



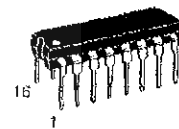
VCC = PIN 16
GND = PIN 8
○ = PIN NUMBERS

SN54/74LS157

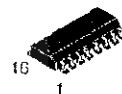
QUAD 2-INPUT MULTIPLEXER LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

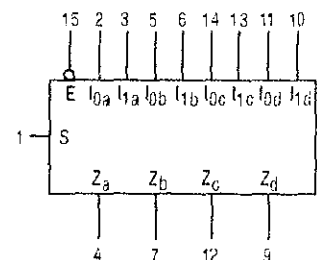


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

SN54/74LS157

FUNCTIONAL DESCRIPTION

The LS157 is a Quad 2-Input Multiplexer fabricated with the Schottky barrier diode process for high speed. It selects four bits of data from two sources under the control of a common Select Input (S). The Enable Input (E) is active LOW. When E is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs.

The LS157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select Input. The logic equations for the outputs are:

$$Z_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S}) \quad Z_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$Z_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S}) \quad Z_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

A common use of the LS157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select Input. A less obvious use is as a function generator. The LS157 can generate any four of the 16 different functions of two variables with one variable common. This is useful for implementing highly irregular logic.

TRUTH TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
E	S	I ₀	I ₁	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current --- High	54, 74			-0.4	mA
I _{OL}	Output Current --- Low	54 74			4.0 8.0	mA

SN54/74LS157

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5		V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 8.0 mA	
I _{IH}	Input HIGH Current I _Q , I ₁ E, S				20 40	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
	I _Q , I ₁ E, S				0.1 0.2	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current I _Q , I ₁ E, S				-0.4 -0.8	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)		-20		-100	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current				16	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
t _{PLH} t _{PHL}	Propagation Delay Data to Output			9.0 9.0	14 14	ns	Figure 2	V _{CC} = 5.0 V C _L = 15 pF
t _{PLH} t _{PHL}	Propagation Delay Enable to Output			13 14	20 21	ns	Figure 1	
t _{PLH} t _{PHL}	Propagation Delay Select to Output			15 18	23 27	ns	Figure 2	

AC WAVEFORMS

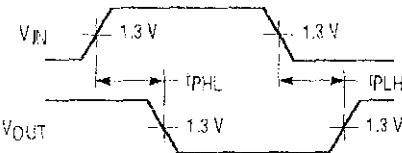


Figure 1

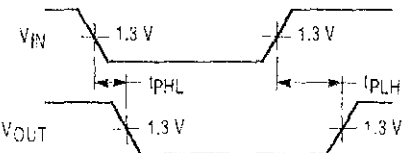


Figure 2



MOTOROLA

OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS; OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

The SN54/74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH the bus output is in the high impedance state.

The SN54/74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) is common to all flip-flops. The SN54/74LS374 is manufactured using advanced Low Power Schottky technology and is compatible with all Motorola TTL families.

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Hysteresis on Latch Enable
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Hysteresis on Clock Input to Improve Noise Margin
- Input Clamp Diodes Limit High Speed Termination Effects

PIN NAMES

D ₀ -D ₇	Data Inputs
LE	Latch Enable (Active HIGH) Input
CP	Clock (Active HIGH going edge) Input
OE	Output Enable (Active LOW) Input
O ₀ -O ₇	Outputs (Note b)

LOADING (Note a)

HIGH	LOW
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
65 (25) U.L.	15 (7.5) U.L.

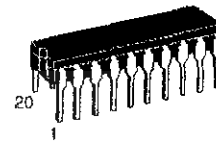
NOTES:

- a) 1 TTL Units Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 7.5 U.L. for Military (54) and 25 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

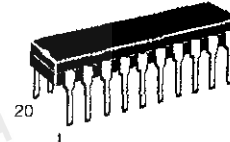
SN54/74LS373
SN54/74LS374

OCTAL TRANSPARENT LATCH
WITH 3-STATE OUTPUTS;
OCTAL D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUT

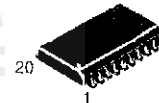
LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03



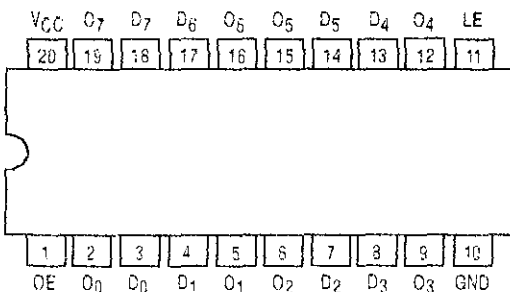
DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

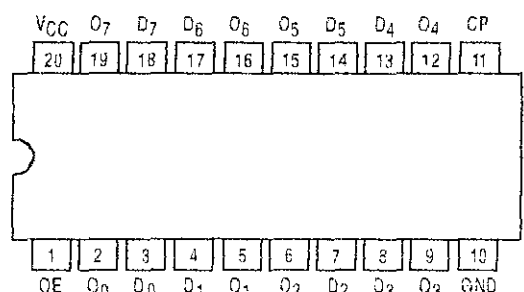
SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXDW SOIC

CONNECTION DIAGRAM DIP (TOP VIEW)

SN54/74LS373



SN54/74LS374



NOTE:
The Flatpak version
has the same pinouts
(Connection Diagram) as
the Dual In Line Package.

FAST AND LS TTL DATA

SN54/74LS373 • SN54/74LS374

TRUTH TABLE

LS373			
D _n	LE	OE	O _n
H	H	L	H
L	H	L	L
X	L	L	Q ₀
X	X	H	Z [*]

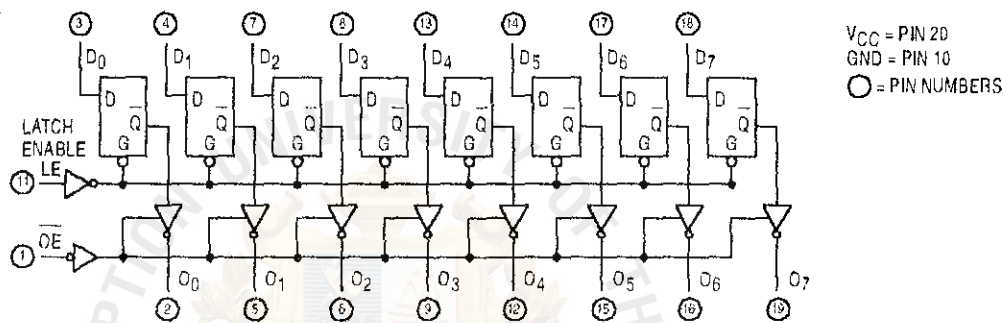
LS374			
D _n	LE	OE	O _n
H		L	H
L		L	L
X	X	H	Z [*]

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

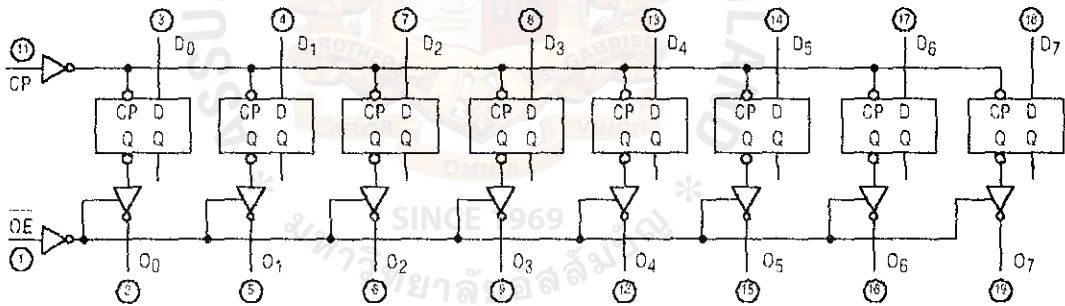
* Note: Contents of flip-flops unaffected by the state of the Output Enable input (OE).

LOGIC DIAGRAMS

SN54LS/74LS373



SN54LS/74LS374



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54 74			-1.0 -2.6	mA
I _{OL}	Output Current — Low	54 74			12 24	mA

SN54/74LS373 • SN54/74LS374

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions	
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V _{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.4	3.4		V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.4	3.1		V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	V	I _{OL} = 24 mA	
I _{OZH}	Output Off Current HIGH				20	μA	V _{CC} = MAX, V _{OUT} = 2.7 V	
I _{OZL}	Output Off Current LOW				-20	μA	V _{CC} = MAX, V _{OUT} = 0.4 V	
I _{IH}	Input HIGH Current				20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
					0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current				-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
I _{OS}	Short Circuit Current (Note 1)		-30		-130	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current				40	mA	V _{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits						Unit	Test Conditions
		LS373			LS374				
		Min	Typ	Max	Min	Typ	Max		
f _{MAX}	Maximum Clock Frequency				35	50		MHz	C _L = 45 pF R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay, Data to Output		12 12	18 18				ns	
t _{PLH} t _{PHL}	Clock or Enable to Output		20 18	30 30		15 19	28 28	ns	
t _{PZH} t _{PZL}	Output Enable Time		15 25	28 36		20 21	28 28	ns	
t _{PHZ} t _{PLZ}	Output Disable Time		12 15	20 25		12 15	20 25	ns	C _L = 5.0 pF

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits				Unit
		LS373		LS374		
		Min	Max	Min	Max	
t _W	Clock Pulse Width	15		15		ns
t _S	Setup Time	5.0		20		ns
t _H	Hold Time	20		0		ns

DEFINITION OF TERMS

SETUP TIME (t_S) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to LE transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_H) — is defined as the minimum time following the LE transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition.

SN54/74LS373

AC WAVEFORMS

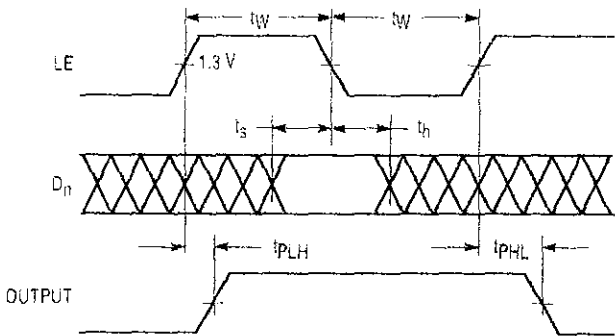


Figure 1

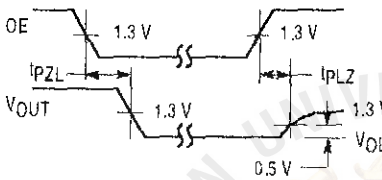


Figure 2

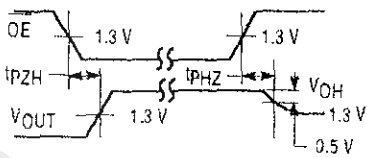
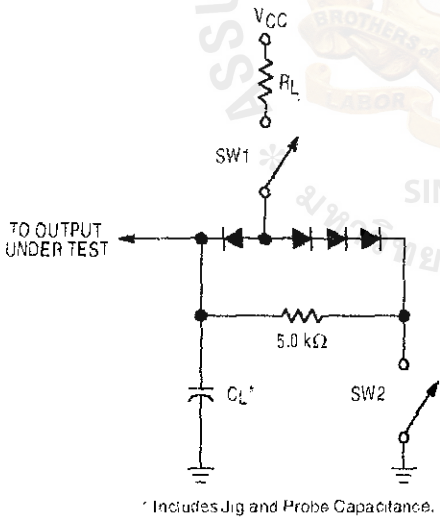


Figure 3

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

Figure 4

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

SN54/74LS374

AC WAVEFORMS

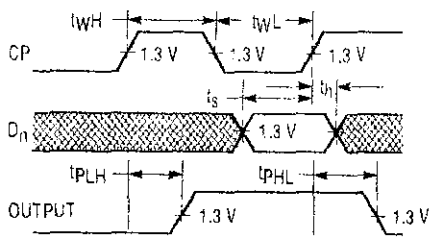


Figure 5

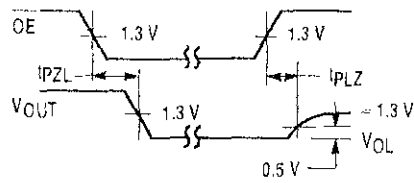


Figure 6

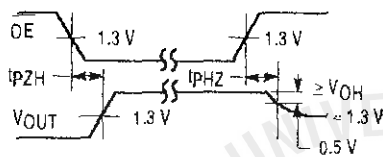
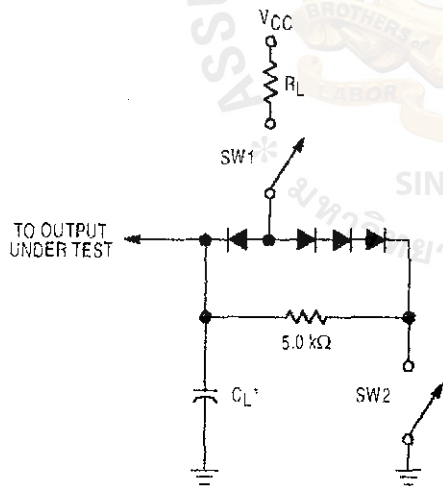


Figure 7

AC LOAD CIRCUIT



* Includes Jig and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Figure 8

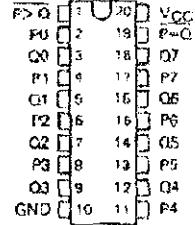
SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688,
SN74LS682, SN74LS684 THRU SN74LS688
8-BIT MAGNITUDE/IDENTITY COMPARATORS

D2617, JANUARY 1981—(REVISED MARCH 1988)

SDLS008

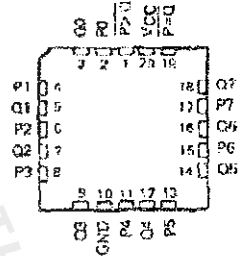
- Compares Two-8-Bit Words
- Choice of Totem-Pole or Open-Collector Outputs
- Hysteresis at P and Q Inputs
- 'LS682 has 20-k Ω Pullup Resistors on the Q Inputs
- SN74LS686 and 'LS687 ... JT and NT 24-Pin, 300-Mil Packages

SN54LS682, SN54LS684, SN54LS685 ... J PACKAGE
SN74LS682, SN74LS684, SN74LS685 ... DW OR N PACKAGE
(TOP VIEW)

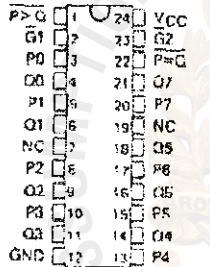


TYPE	P = Q	P > Q	OUTPUT ENABLE	OUTPUT CONFIGURATION	20-k Ω PULLUP
'LS682	yes	yes	no	totem-pole	yes
'LS684	yes	yes	no	totem-pole	no
'LS685	yes	yes	no	open-collector	no
SN74LS686	yes	yes	yes	totem-pole	no
'LS687	yes	yes	yes	open collector	no
'LS688	yes	no	yes	totem-pole	no

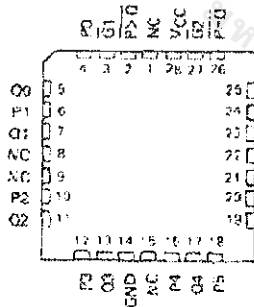
SN54LS682, SN54LS684, SN54LS685 ... FK PACKAGE
(TOP VIEW)



SN54LS687 ... JT PACKAGE
SN74LS686, SN74LS687 ... DW OR NT PACKAGE
(TOP VIEW)

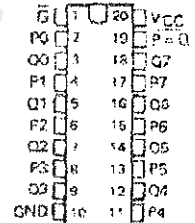


SN54LS687 ... FK PACKAGE
(TOP VIEW)

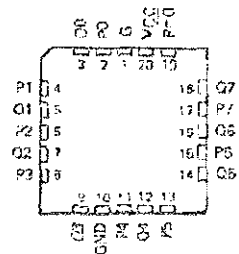


NC—No internal connection

SN54LS688 ... J PACKAGE
SN74LS688 ... DW OR N PACKAGE
(TOP VIEW)



SN54LS688 ... FK PACKAGE
(TOP VIEW)



PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655912 • DALLAS, TEXAS 75265

SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688
SN74LS682, SN74LS684 THRU SN74LS688
8-BIT MAGNITUDE/IDENTITY COMPARATORS

description

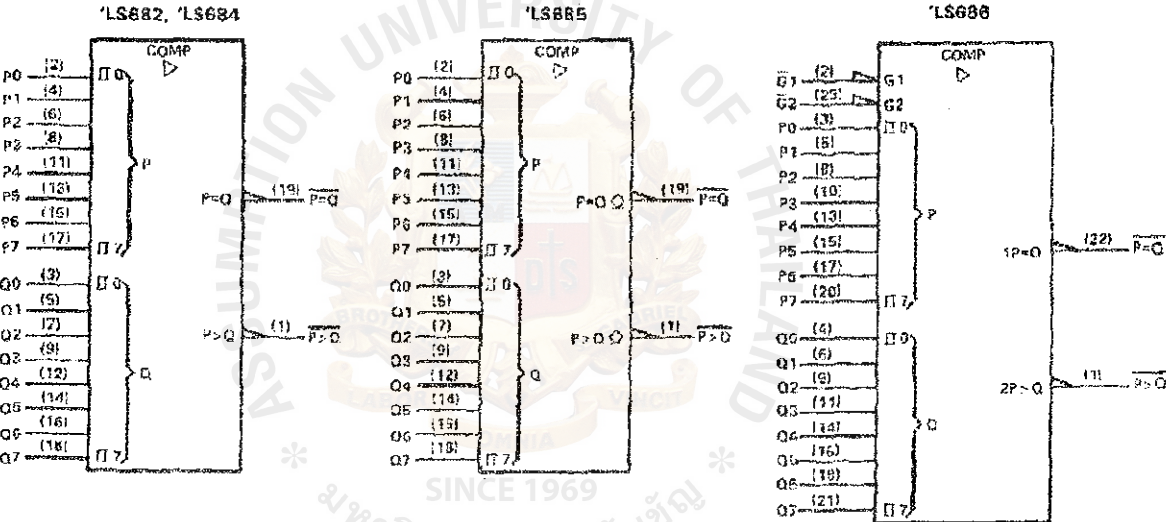
These magnitude comparators perform comparisons of two eight-bit binary or BCD words. All types provide $P = Q$ outputs and all except 'LS688 provide $P > Q$ outputs as well. The 'LS682, 'LS684, 'LS686, and 'LS688 have totem-pole outputs, while the 'LS685 and 'LS687 have open-collector outputs. The 'LS682 features 20-k Ω pullup termination resistors on the Q inputs for analog or switch data.

FUNCTION TABLE

INPUTS			OUTPUTS	
DATA	ENABLES		$P = Q$	$P > Q$
P, Q	$\overline{G}_1, \overline{G}_2$	$\overline{G}_2$		
$P = Q$	L	X	L	H
$P > Q$	X	L	H	L
$P < Q$	X	X	H	H
$P = Q$	H	X	H	H
$P > Q$	X	H	H	H
X	H	H	H	H

- NOTES: 1. The last three lines of the function table apply only to the devices having enable inputs, i.e., 'LS686 thru 'LS688.
2. The $P < Q$ function can be generated by applying the $P = Q$ and $P > Q$ outputs to a 2-input NAND gate.
3. For 'LS686 and 'LS687, $\overline{G}_1$ enables $P = Q$ and $\overline{G}_2$ enables $P > Q$.

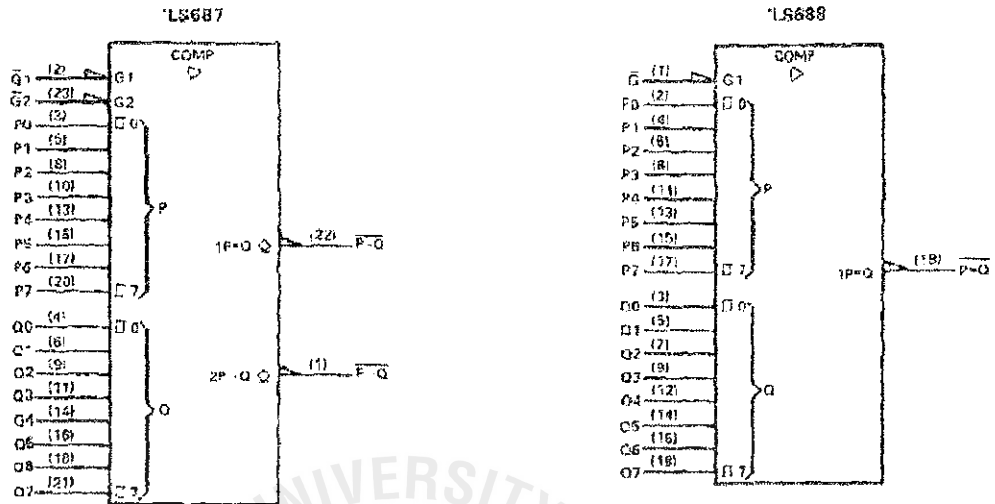
logic symbols†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, JT, N, and NT packages.

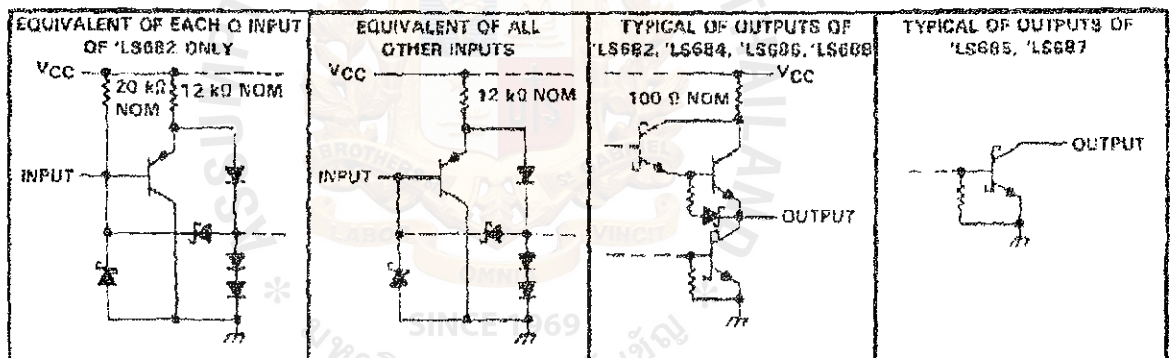
SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688,
SN74LS682, SN74LS684 THRU SN74LS688
8-BIT MAGNITUDE/IDENTITY COMPARATORS

logic symbols[†] (continued)



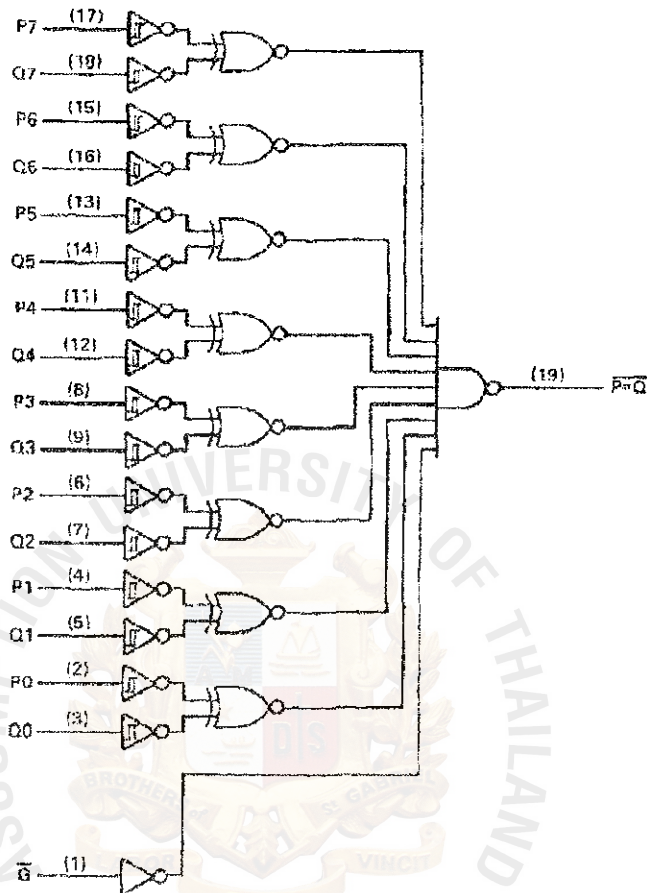
[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, JT, N, and NT packages.

schematics of inputs and outputs



**SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688
SN74LS682, SN74LS684 THRU SN74LS688
8-BIT IDENTITY COMPARATORS**

'LS688 logic diagram (positive logic)



Pin numbers shown are for DW, J, and N packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: Q inputs of 'LS682	5.5 V
All other inputs	7 V
Off-state output voltage: 'LS685, 'LS687	7 V
Operating free-air temperature range:	
SN54LS682, SN54LS684, SN54LS685, SN54LS687, SN54LS688	-65°C to 125°C
SN74LS682, SN74LS684 thru SN74LS688	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

SN54LS682, SN54LS684, SN54LS688
SN74LS682, SN74LS684, SN74LS686, SN74LS688
8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH TOTEM-POLE OUTPUTS

recommended operating conditions

	SN54LS ¹			SN74LS ¹			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.85	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	-65		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS ¹	SN54LS ¹			SN74LS ¹			UNIT
			MIN	TYP ²	MAX	MIN	TYP ²	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage			0.7			0.8		V
$V_T+ - V_T-$	Hysteresis	P or Q inputs	0.4			0.4			V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$ $V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$	-1.5			-1.5			V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5			2.7			V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN},$ $V_{IH} = 2 \text{ V},$ $V_{IL} = V_{IL \text{ max}}, I_{OL} = 12 \text{ mA}$	0.25 0.4			0.25 0.4			V
		$I_{OL} = 24 \text{ mA}$				0.35 0.5			
I_I	Input current at maximum	Q inputs, 'LS682	$V_{CC} = \text{MAX}, V_I = 8.5 \text{ V}$			0.1			mA
	Input voltage	All other inputs	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$	20			20			μA
I_{IL}	Low-level	Q inputs, 'LS682	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			mA
	Input current	All other inputs				-0.2			
I_{OS}^5	Short-circuit output current	$V_{CC} = \text{MAX}, V_O = 0$	-20 -100			-20 -100			mA
I_{CC}	Supply current	'LS682	42 70			42 70			mA
		'LS684	40 65			40 65			
		'LS686	44 75			44 75			
		'LS688	40 65			40 65			

¹ For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

² All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

⁵ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 1: I_{CC} is measured with any Q inputs grounded, all other inputs at 4.5 V, and all outputs open.

SN54LS682, SN54LS684, SN54LS688
SN74LS682, SN74LS684, SN74LS686, SN74LS688
8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH TOTEM-POLE OUTPUTS

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER†	FROM (INPUTS)	TO (OUTPUT)	TEST CONDITIONS	'LS682			'LS684			'LS686			'LS688			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	P	$P=Q$	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$, All other Inputs low, See Note 2	13	25		15	25		13	25		12	18	ns	
t_{PHL}				15	25		17	25		20	30		17	23		
t_{PLH}	Q	$P=Q$		14	25		16	25		13	25		12	18	ns	
t_{PHL}				15	25		15	25		21	30		17	23		
t_{PLH}	$\bar{Q}, \bar{Q}_1$	$P=\bar{Q}$								11	20		12	18	ns	
t_{PHL}										19	30		13	20		
t_{PLH}	P	$P>Q$		20	30		22	30		19	30				ns	
t_{PHL}				15	30		17	30		15	30					
t_{PLH}	Q	$P>Q$		21	30		24	30		18	30				ns	
t_{PHL}				19	30		20	30		19	30					
t_{PLH}	$\bar{Q}_2$	$P>Q$								21	30				ns	
t_{PHL}										18	25					

† t_{PLH} = propagation delay time, low-to-high-level outputs; t_{PHL} = propagation delay time, high-to-low-level output.
NOTE 2: Load circuits and voltage waveforms are shown in Section 1.



SN54LS685, SN54LS687
SN74LS685, SN74LS687, SN74LS688

8-BIT MAGNITUDE/IDENTITY COMPARATORS WITH TOTEM-POLE OUTPUTS

recommended operating conditions

	SN54LS*			SN74LS*			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS ¹	SN54LS*			SN74LS*			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
$V_{T+} - V_{T-}$	Hysteresis	P or Q inputs			0.4			0.4	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
I_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{ILmax}$, $V_{OH} = 5.5 \text{ V}$			250			100	μA
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = V_{ILmax}$, $I_{OL} = 12 \text{ mA}$		0.25	0.4		0.25	0.4	V
		$I_{OL} = 24 \text{ mA}$					0.35	0.5	
I_I		$V_{CC} = \text{MAX}$, $V_I = 2 \text{ V}$			0.1			0.1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.7 \text{ V}$			20			20	μA
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-0.2			-0.2	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, See Note 1			40			40	mA
					85			85	
					44			44	75

¹For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

*All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

NOTE 1: I_{CC} is measure with any $\bar{G}$ inputs grounded, all other inputs at 4.5 V, and all outputs open.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655812 • DALLAS, TEXAS 75265

Programmable Peripheral Interface Adapter

September 1997

Features

- ✱ a8255 MegaCore function implementing a programmable peripheral interface adapter
- ✱ Optimized for FLEX[®] and MAX[®] architectures
- ✱ 24 programmable inputs/outputs
- ✱ Static read/write or handshaking modes
- ✱ Direct bit set/reset capability
- ✱ Synchronous design
- ✱ Uses approximately 194 FLEX logic elements (LEs)
- ✱ Functionally based on the Intel 8255A and Harris 82C55A devices, except as noted in the "Variations & Clarifications" section on page 56

General Description

The a8255 MegaCore function implements a programmable peripheral interface adapter (see Figure 1). The a8255 has 24 I/O signals that can be programmed in two groups of 12. This MegaCore function operates in the following three modes:

- ✱ *Mode 0: Basic Input/Output*—Port A, port B, and port C (upper and lower) can be independently configured as inputs or outputs to read or hold static data. Outputs are registered; inputs are not registered.
- ✱ *Mode 1: Strobed Input/Output*—Port A and port B can be independently configured as strobed input or output buses. Signals from port C are dedicated as control signals for data handshaking.
- ✱ *Mode 2: Bidirectional Bus*—Port A can be configured as a bidirectional bus with the majority of port C providing the control signals. In this configuration, port B can still implement mode 0 or mode 1.

Figure 1. a8255 Symbol

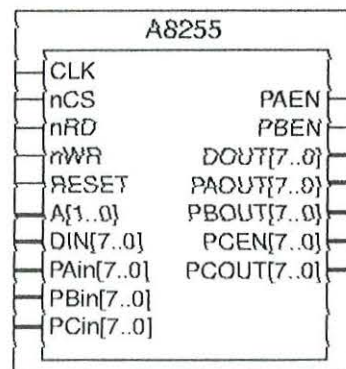


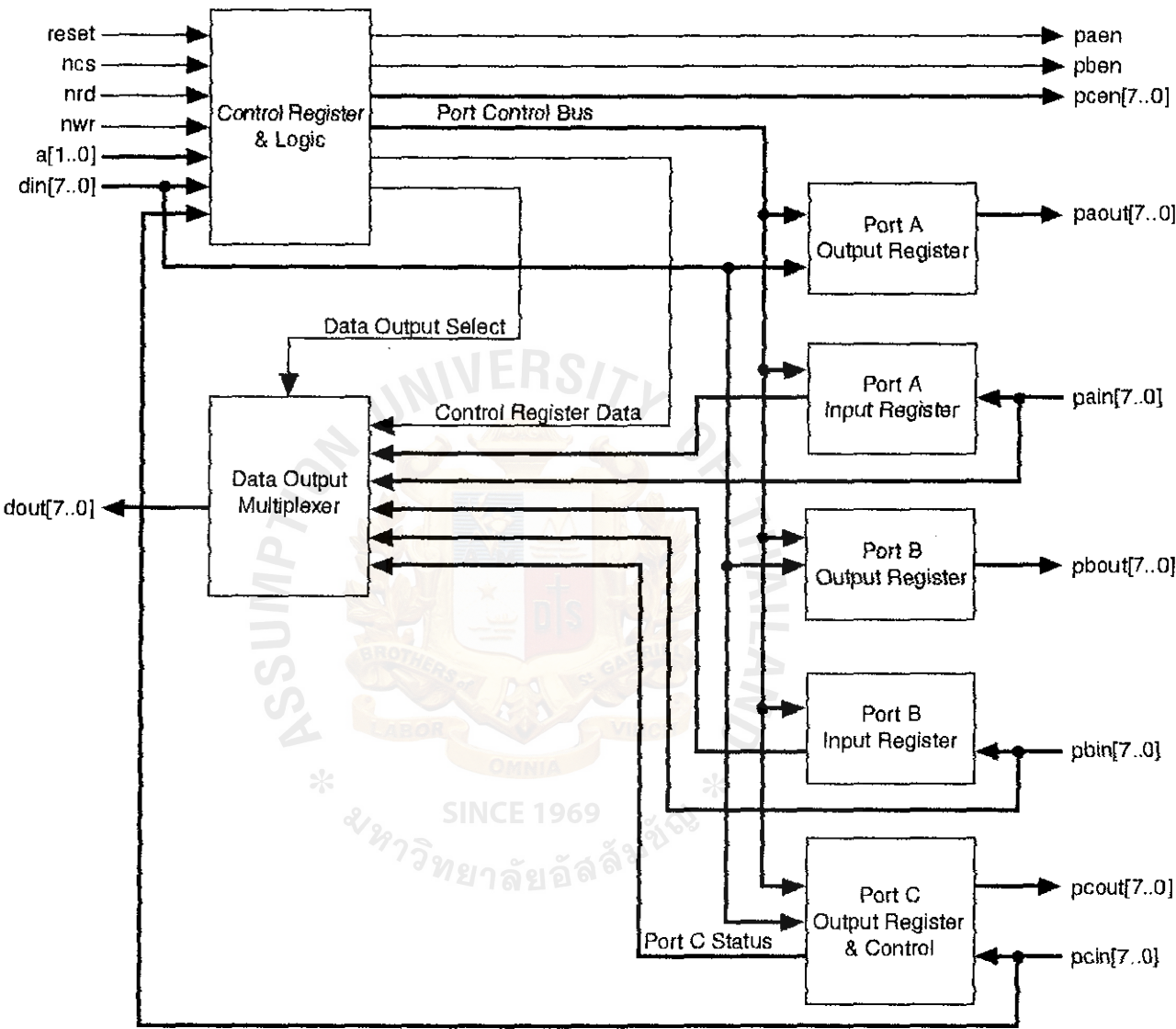
Table 1 describes the input and output ports of the a8255.

Table 1. a8255 Ports			
Name	Type	Polarity	Description
clk	Input	–	Clock.
ncs	Input	Low	Chip select. When ncs is asserted, the a8255 is selected and read and write transactions to internal registers are possible.
nrd	Input	Low	Read control. When nrd is asserted and the a8255 is selected, read transactions from internal registers are possible.
nwr	Input	Low	Write control. When nwr is asserted and the a8255 is selected, write transactions to internal registers are possible.
reset	Input	High	Reset. Initializes the control and port C output registers, and sets the port A, B, and C registers to input mode.
a[1..0]	Input	High	Register address bus. This bus selects one of the internal registers.
din[7..0]	Input	High	Data input bus. The CPU writes data to the internal control, port A, port B, or port C register via the din[7..0] bus.
pain[7..0]	Input	High	Port A input data bus.
pbin[7..0]	Input	High	Port B input data bus.
pcin[7..0]	Input	High	Port C input data bus.
paen	Output	High	Port A data enable. Output enable for the port A output data bus.
pben	Output	High	Port B data enable. Output enable for the port B output data bus.
dout[7..0]	Output	High	Data output bus. The CPU reads data from the internal control, port A, port B, or port C register via the dout[7..0] bus.
paout[7..0]	Output	High	Port A output data bus.
pbout[7..0]	Output	High	Port B output data bus.
pcen[7..0]	Output	High	Port C data enable bus. Output enable for each bit of the port C output data bus.
pcout[7..0]	Output	High	Port C output data bus.

Functional Description

Figure 2 shows a block diagram of the a8255.

Figure 2. a8255 Block Diagram



Register Address Map

Table 2 shows the register address map for the a8255.

<i>Table 2. Register Address Map</i>		
a1	a0	Register
0	0	Port A data (all modes)
0	1	Port B data (all modes)
1	0	Port C data (mode 0) and status (modes 1 and 2)
1	1	Control register mode definition and port C bit set/reset

Registers

This section describes the following a8255 registers:

- ✘ Control
- ✘ Port A, B & C

Control Register

The control register sets the mode and signal direction for the three 8-bit I/O ports. Control of the I/O ports is split into two groups. Group A consists of port A and the upper four bits of port C; group B consists of port B and the lower four bits of port C. Group A can be set to mode 0, mode 1, or mode 2, but group B can be set to only mode 0 or mode 1.

Writing to the control register address with bit 7 set is the mode definition format, which allows control of the mode and direction of the three I/O ports (see Table 3). Writing to the control register address with bit 7 reset is the port C bit set/reset format, which allows single-bit control of port C (see Table 4). The CPU reads the control register using the mode definition format.

Table 3. Control Register Mode Definition Format

Bit	Description
0	Port C (lower) I/O direction: 1 = input 0 = output
1	Port B I/O direction: 1 = input 0 = output
2	Group B mode select: 1 = mode 1 0 = mode 0
3	Port C (upper) I/O direction: 1 = input 0 = output
4	Port A I/O direction: 1 = input 0 = output
6..5	Group A mode select: 00 = mode 0 01 = mode 1 1X = mode 2, <i>Note (1)</i>
7	1 when writing = mode definition format Always 1 when reading the control register

Note:

- (1) The X indicates "don't care."

Table 4. Port C Bit Set/Reset Format *Note (1)*

Bit	Description
0	Bit set/reset: 1 = set 0 = reset
3..1	Bit select address
6..4	XXX, <i>Note (2)</i>
7	0 when writing = port C bit set/reset format

Notes:

- (1) For example, to reset bit 3 of port C, bit 7 is reset to indicate that the write is in the port C bit set/reset format. Bits 6 through 4 are "don't care." Bits 3 through 1 are 011 to address bit 3, and bit 0 is 0 to indicate a reset operation. The complete data word is 0XXX0110.
- (2) The X indicates "don't care."

Port A, B & C Registers

Depending on the configured input and output directions that are set in the control register, the microprocessor either reads or writes data to/from the port A, B, or C registers. Ports A and B have separate input and output registers.

In mode 0, the port C register functions identically to the port A and B registers. In modes 1 and 2, the port C register has a specialized role; a write to port C has no effect—the register bits must be altered individually using the port C bit set/reset format. Reading the port C status bits in modes 1 or 2 provides the CPU with the status of the control signals and flags, as shown in Tables 5 through 7. However, the modes and port directions can be mixed in more combinations than these tables illustrate.

Table 5. Port C Status Bits with Ports A & B in Mode 1 Input <i>Note (1)</i>		
Bit	Signal	Description
0	intrb	Port B interrupt request
1	ibfb	Port B input buffer full flag
2	inteb	Port B interrupt enable
3	intra	Port A interrupt request
4	intea	Port A interrupt enable
5	ibfa	Port A input buffer full flag
6	I/O	<i>Note (2)</i>
7	I/O	<i>Note (2)</i>

- Notes:
- (1) These bits are defined in Table 9.
 - (2) Bits 6 and 7 effectively operate in mode 0. The I/O direction is dependent on bit 3 of the control register.

Table 6. Port C Status Bits with Ports A & B in Mode 1 Output *Note (1)*

Bit	Signal	Description
0	intrb	Port B interrupt request
1	nobfb	Port B output buffer full flag
2	inteb	Port B interrupt enable
3	intra	Port A interrupt request
4	I/O	<i>Note (2)</i>
5	I/O	<i>Note (2)</i>
6	intea	Port A interrupt enable
7	nobfa	Port A output buffer full flag

Notes:

- (1) These bits are defined in Table 3.
 (2) Bits 4 and 5 effectively operate in mode 0. The I/O direction is dependent on bit 3 of the control register.

Table 7. Port C Status Bits with Port A in Mode 2 *Note (1)*

Bit	Signal	Description
0	—	<i>Note (2)</i>
1	—	<i>Note (2)</i>
2	—	<i>Note (2)</i>
3	intra	Port A interrupt request
4	inte2	Interrupt enable 2
5	ibfa	Port A input buffer full flag
6	intel	Interrupt enable 1
7	nobfa	Port A output buffer full flag

Notes:

- (1) These bits are defined in Table 11.
 (2) Depending on the lower three bits of the control register, bits 0 through 2 either operate in mode 0 or function as status bits for port B in mode 1.

peration

The a8255 operates in the following three modes:

- ☒ Mode 0: basic input/output
- ☒ Mode 1: strobed input/output
- ☒ Mode 2: strobed bidirectional bus

Mode 0: Basic Input/Output

Mode 0 is used to perform simple reads or writes of relatively static signals, such as switches or status displays. Port A, port B, port C (upper), and port C (lower) can be independently configured as inputs or outputs without requiring handshake signals. Data written by the CPU to a port configured as an output is registered; data read by the CPU from a port configured as an input is not registered.

Mode 1: Strobed Input/Output

Mode 1 is used to perform reads or writes of data controlled by handshake signals. Ports A and B are the data ports, configured independently as either inputs or outputs. Port C provides the three handshaking signals for each of the data ports. Both input and output data are registered.

Table 8 shows how the handshaking signals are configured for mode 1 input.

Table 8. Handshaking Signal Configuration (Mode 1 Input)		
Name	Signal Type	Description
nstb	Input	Strobe. Enable for input register.
ibf	Output	Input buffer full flag. When set, indicates that data has been loaded into the input register. Set by nstb going low, and reset by the rising edge of the nrd input.
intr	Output	Interrupt request. Can be used as the interrupt signal to the CPU. Set on the rising edge of nstb when inte is high. Reset by the falling edge of nrd.
inte	Internal control bit	Interrupt enable. Set by bit set to PC4 for port A and PC2 for port B.

Table 9 shows how the handshaking signals are configured for mode 1 output.

Table 9. Handshaking Signal Configuration (Mode 1 Output)		
Name	Signal Type	Description
nobf	Output	Output buffer full flag. Indicates that data has been written to the port. Goes low on the rising edge of <i>nwr</i> , and returns high when <i>nack</i> is asserted. The rising edge of <i>nobf</i> should be used to latch data into the peripheral.
nack	Input	Acknowledge. Indicates the peripheral is ready to latch the output data.
intr	Output	Interrupt request. Can be used as the interrupt signal to the CPU, which indicates that the peripheral device has latched the data. Reset on the falling edge of <i>nwr</i> ; set on the rising edge of <i>nack</i> when <i>inte</i> is high.
inte	Internal control bit	Interrupt enable. Set by bit set to PC6 for port A and PC2 for port B.

Table 10 summarizes the configuration of port C when both port A and port B are configured as mode 1.

Table 10. Port C with Port A & Port B Both Configured as Mode 1			Note (1)
Bit	Mode 1 Input	Mode 1 Output	Description
PC0	intrb	intrb	Always output.
PC1	ibfb	nobfb	Always output.
PC2	nstbb	nackb	Always input.
PC3	intra	intra	Always output.
PC4	nstba	I/O	I/O direction configured by bit 3 of the control register in "mode 1 output."
PC5	ibfa	I/O	I/O direction configured by bit 3 of the control register in "mode 1 output."
PC6	I/O	nacka	I/O direction configured by bit 3 of the control register in "mode 1 input."
PC7	I/O	nobfa	I/O direction configured by bit 3 of the control register in "mode 1 input."

te:

The interrupt enable control bits (*intea* and *inteb*) are stored in the output register bits PC2, PC4, and PC6.

Mode 2: Strobed Bidirectional Bus

Mode 2 is used to perform reads and writes of data over a bidirectional bus controlled by handshake signals. Port A is the only data port capable of mode 2 operation, while port C provides the five control signals for this data port. Both input and output data are registered. Table 11 shows the configuration for the bidirectional bus.

Table 11. Bidirectional Bus Configuration

Name	Signal Type	Description
nstb	Input	Strobe. Enable for input register.
nack	Input	Acknowledge. Indicates that the peripheral is ready to latch the output data. Acts as the tri-state enable for port A.
ibf	Output	Input buffer full flag. When set, indicates data has been loaded into the input register. Set by nstb going low, and reset by the rising edge of the nrd input.
nobf	Output	Output buffer full flag. Indicates that data has been written to port A. Reset on the rising edge of nwr, and set when nack goes low.
intr	Output	Interrupt request. Can be used as the interrupt signal to the CPU that indicates the peripheral has latched the data. Reset on the falling edge of nwr or falling edge of nrd. Set on the rising edge of nack when inte1 is high, or on the rising edge of nstb when inte2 is high.
inte1	Internal control bit	Interrupt enable 1. Set by bit set to PC6.
inte2	Internal control bit	Interrupt enable 2. Set by bit set to PC4.

Table 12 summarizes the configuration of port C in mode 2.

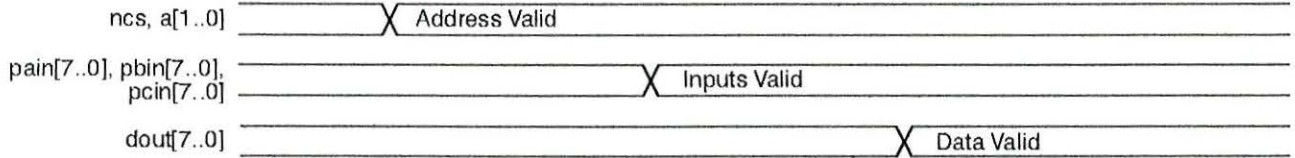
Table 12. Port C Configuration in Mode 2		
I/O	Mode 2	Description
PC0	I/O	Dependent on group B configuration
PC1	I/O	Dependent on group B configuration
PC2	I/O	Dependent on group B configuration
PC3	intra	Output
PC4	nstba	Input
PC5	ibfa	Output
PC6	nacka	Input
PC7	nobfa	Output

Timing Waveforms

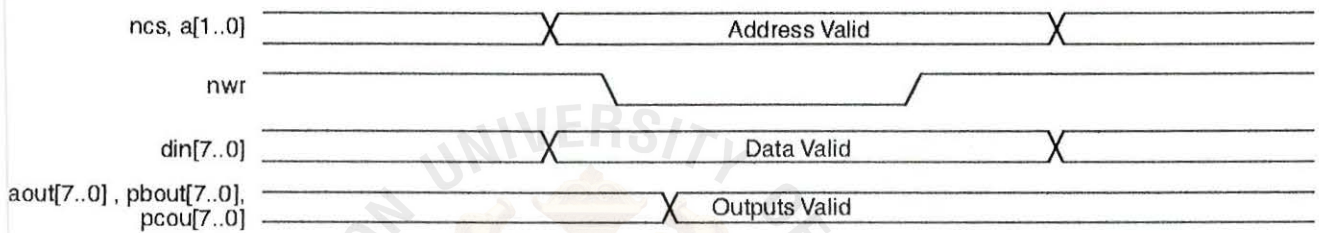
Figures 3 and 4 shows the functional timing waveforms for the a8255.

Figure 3. a8255 Mode 0 and Mode 1 Functional Timing Waveforms

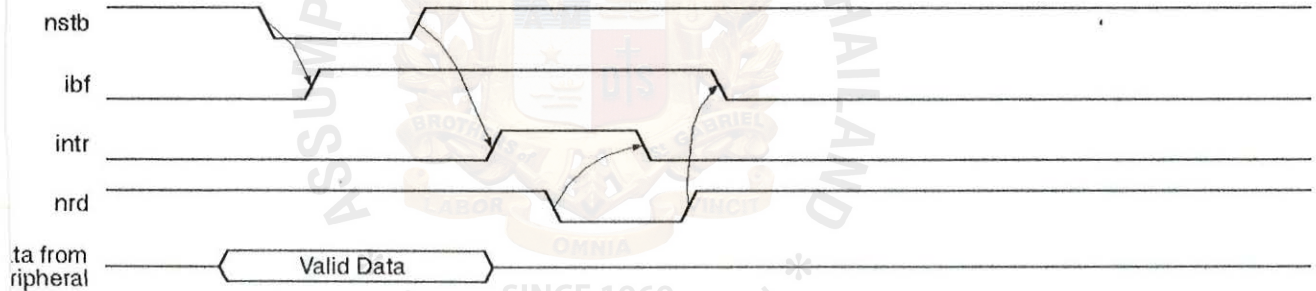
Mode 0: Basic Input



Mode 0: Basic Output



Mode 1: Strobed Input



Mode 1: Strobed Output

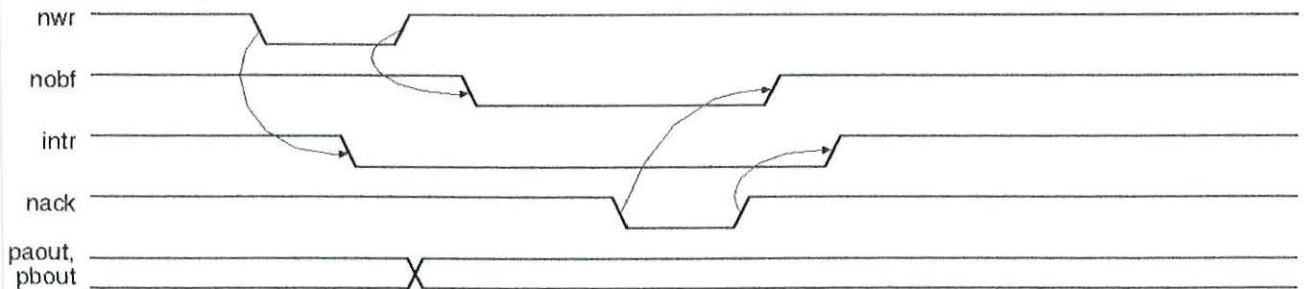
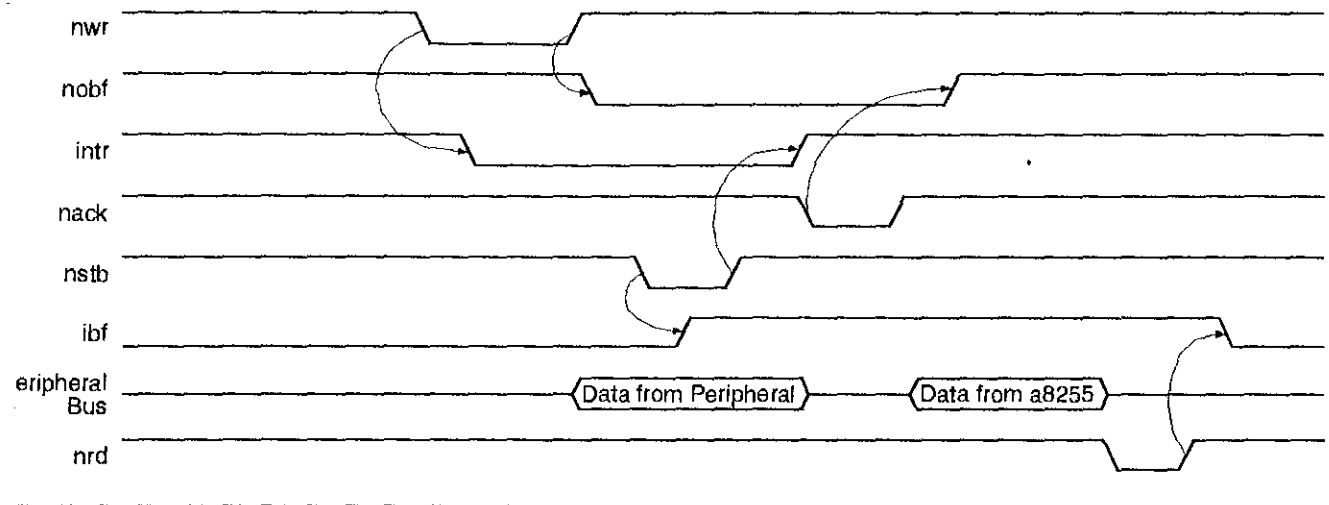


Figure 4. a8255 Mode 2 Functional Timing Waveforms

Mode 2: Bidirectional Bus



Variations & Clarifications

The following characteristics distinguish the Altera a8255 from the Intel 8255A and Harris 82C55A devices:

- ✖ To allow synchronous design, a `clk` input was added as a system clock to the a8255. This capability requires that all strobes (`nrd`, `nwr`, `nstb`, and `nack`) have a minimum pulse width of one `clk` cycle.
- ✖ In the a8255, the reset input resets the port A, B, and C registers. In the Intel 8255A and Harris 82C55A devices, the port A, B, and C registers are unaffected by the reset input.
- ✖ The bidirectional buses in the Intel 8255A and Harris 82C55A devices (`d`, `pa`, `pb`, and `pc`) are split into input, output, and enable signals in the Altera a8255.
- ✖ The a8255 has no "bus hold" passive pull-ups on port signals. Because the port I/O signal is usually tied to the I/O of the Altera device, pull-ups or pull-downs can be added.
- ✖ In the a8255, the control register can be read. The control register can be read on the Harris 82C55A device, but the Intel 8255A device does not have this capability.
- ✖ In the a8255, the reset signal initializes the control register such that all ports are set to mode 0 inputs. Reading the control register after initialization will return the value of 9B in hexadecimal.
- ✖ After initialization in mode 1, the pertinent control signals in the port C register should be configured via the port C bit set/reset commands.
- ✖ In mode 2, every read or write of port A resets the `intra` interrupt signal.
- ✖ The Intel and Harris data sheets state that output registers and status flipflops should be reset in the event of a mode change. This feature was not included in the a8255.

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VITA

Name : Taminee Shinasharkey
Birth date : May 18, 1979
Place of birth : Bangkok
Religion : Buddhism
Nationality : Thai
Present address : 77/26 Soi Punnavithee 27
Sukhumvit 101 Road
Bangjak Prakanong Bangkok 10260

Education Background

Primary School : Saint Joseph Convent School
(1984-1989)
Secondary School : Saint Joseph Convent School
(1990-1994)
University : Assumption University
Computer Engineering
(1995-1998)

VITA

Name : Montai Settapokin
Birth date : December 15, 1976
Place of birth : Bangkok
Religion : Buddhism
Nationality : Thai
Present address : 1692/221 Kumthong Villa
Teparak rd., Samutprakarn 10270
Thailand

Education Background

Primary School : Holy Innocent Primary School, Singapore
(1981-1984)
Xian Jia Primary School, China
(1984-1986)
Secondary School : Shi Si Zhong Secondary School, China
(1987-1988)
PrakanongPitayalai Secondary School, Thailand
(1989-1994)
University : Assumption University
Computer Engineering
(1995-1998)

