

Data Communication On Electric Line

Cherdchai Jungsathitkul (361 - 6310)

Data Communication On Electric Line

Presented To Dr. Pharon Sanguanbhokai

BY

1. Cherdchai Jungsathitkul (361-6310)
2. Suvir Kumar (361-6898)

This project is a part of the requirement of the courses
EN4902 and EE4902
Electronics and Electrical Engineering Project II

Faculty Of Electronics Engineering
Faculty Of Electrical Engineering

ABAC School Of Engineering
Assumption University
March 16th, 1998

Table of Contents

<i>Acknowledgment</i>	4
<i>Abstract</i>	6

Chapter 1 Introduction

<i>Introduction To Power Line Communication</i>	9
<i>Short Description Of Project</i>	10
<i>Main Block Diagram</i>	11
<i>Summary Of Various Parts Of The Block Diagram</i>	11
<i>Existing Power Line Communications Standards</i>	12
<i>Forecasted Problems Using The Carrier Current System</i>	12

Chapter 2 Theory & Design

<i>The PC Parallel Port</i>	14
<i>Introduction and Background of Parallel Ports</i>	14
<i>Brief History On The Development Of The Parallel Port</i>	15
<i>Hardware Properties</i>	15
<i>Address Notes</i>	17
<i>Start Address Function</i>	18
<i>Modulation and Demodulation</i>	18
<i>FSK Modulation Theory</i>	19
<i>Theory of LM1893</i>	22
<i>Theory of UM3750 Decoder / Encoder Chip</i>	23
<i>Theory of Microcontroller Timer and Display</i>	24
<i>Timer Circuit Description</i>	27

Chapter 3 Fabrication & Construction

<i>Schematic Diagram AT89C51 and ICM7217 Unit</i>	30
<i>Schematic Diagram Receiver</i>	31
<i>Schematic Diagram Transmitter</i>	32

Chapter 4 Program Source Codes

<i>Pascal & The PC Parallel Port</i>	33
<i>Foxpro Program Source Code</i>	33
<i>AT89C51 Assembly Program</i>	62

Chapter 5 Test Experiments, Equipment

<i>First Experimental Tests</i>	67
<i>Equipment Used In Experiment and Fabrication</i>	69
<i>Electronic Component Used</i>	70

Chapter 6 Conclusion & Recommendation

<i>Conclusion</i>	71
<i>Recommendation</i>	72

Project Information

<i>Bibliographies & References</i>	73
<i>Vita & Photograph Suvir Kumar (361-6898)</i>	74
<i>Vita & Photograph Cherdchai Jungsathitkul (361-6310)</i>	75
<i>Project Photographs</i>	76

Appendix

<i>PCB Foil Pattern Microcontroller Based Timer</i>
<i>PCB Foil Pattern Rx and Tx Modules</i>
<i>Data Sheet UM 3750 Encoder/Decoder</i>
<i>Data Sheet AT89C51</i>
<i>Data Sheet LM1893N</i>
<i>Data Sheet ICM71217</i>

Acknowledgment

This project is a part of the requirement of the course EN4902 and EE4901 (Electronics and Electrical Engineering Project II) as required by the Faculty of Engineering Assumption University. This project report is a compilation of data from many sources such as projects of others whom have graduated before us, many textbooks, various web sites, data sheets downloaded from the internet and most important of all our knowledge which we have gained here at Assumption University as a result of our years of professional training here.

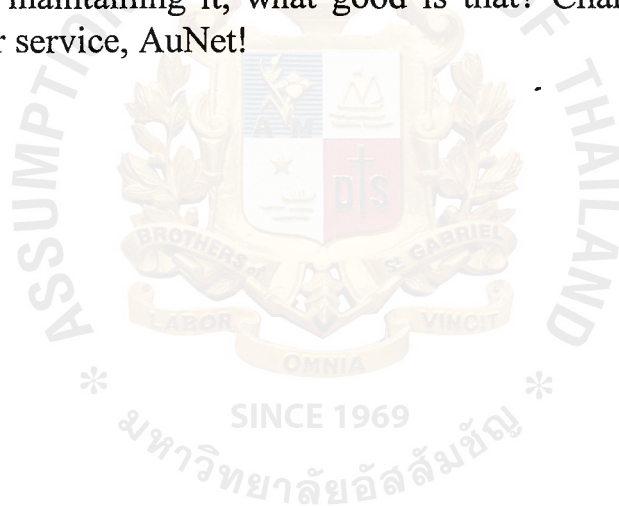
Our project is a combination of the suggestions and previous works of those whom we consider our Mentors. This is our chance to acknowledge others for their great influence and contribution. We must thank particularly, Dr. Pharon Sanguanbhokai our project adviser, who suggested many topics on which we could work on and how to go about working and researching on each particular project. We would also like to thank Dr. Win Tin and Dr. Seshanna for opening our eyes to the interesting modern world of Electronics and Microprocessors. We would also like to thank all our other instructors for all the knowledge that they have passed on to us which has enabled us to come this far in the academic world.

We would like to thank The President of Assumption University Brother Martin for without his great management skills Assumption University would not be half of what it is today. The Dean Of The Faculty Of Engineering and Associate Dean Of The Faculty Of Engineering Dr. Suttiporn and Dr. Win Tin for their support and funding for the Network Research Center where we used all the tools and equipment in the fabrication of our project.

Thank you Rodney Simon (362-6105) for the great data books from National Semiconductor. Zaw Tin Oo for the knowledge of using the LM1893 Carrier Current transceiver and your advice in using Pascal Language for the control of The PC Parallel Port. Poltat Sirvattanalak for his help in designing the foil pattern of our Printed Circuit Board and

helping our with the drilling, soldering, spray painting and all other labour intensive jobs that were a part of building up this project. Lester Protacio (362-1871) for his help and advice in the use of Microsoft Word and organizing this project report. Ursa Major International for their generous supply of reporting resources and the use of their Laser Printer. Thank you Pittaya Achriyasilp of Siam Hardware Industry for your generous loan of a Laptop Computer that was required in the Demonstration of this project which will take place in front of the Project Committee Office of The Faculty of Engineering Assumption University. Thank you Malcolm C. Rubel for your wonderful book Title Foxpro Power Tools. Thank you for making Foxpro programming so easy!

We would also like to take this opportunity to thank all our friends those future Engineers who gave us advice and new ideas. Lastly, we would like to say that Aunet is really a hopeless Internet Service Provider. Aunet you have all the equipment, all the phone lines, all the latest equipment but you don't bother maintaining it, what good is that? Change your attitude and improve your service, AuNet!



Abstract

In this present day of high technology and competition we must be more productive and cost conscious. The projects which we design as Electrical and Electronic Engineers must be cheaper and more efficient. With less time on our hands because of our busy schedules new products must be designed to be easier to use than ever before. More than that these products must be easy to install, upgrade and repair. The ideal system should be able to be broken into many small identical pieces, so that in the event of a failure in some part of the system, replacements can be made almost instantly.

Technically using the AC Electric line as a medium of communication is called The Current Carrier System. Our Computerized remote control system using the Carrier Current System as a medium is a very efficient way of controlling electronic and electrical devices within a local area that utilizes the same mains transformer. The advantages and disadvantages of this type of system will be discussed later in this project. We will use the FSK method of modulation because it is less error prone, in a noisy environment such as the Electric line.

This device can be used to build your own home, office or factory automation system where you can control lights, relays, timers and other transducers in your environment. Turn things on/off or control devices like stereos, etc. This project is Uni-Directional. It utilises Open Loop Control because of its simplicity and reasons due to lack of funding and time.

Below is a short list of some doable things with this type of system. Just to spark your imagination...some example applications are

- Control lights and other devices
- Security systems
- Energy control and management
- Process control
- Environmental control
- Heating and air condition control
- Sprinkler/watering systems
- Connect your whole home to Internet
- Help for elderly and disabled people
- Close blinds if sunlight is too strong
- Let your PC control your home
- Stage control in home theatres

There are many advantages of using the carrier current system as a system of communication. Once a node is configured using a simple, software driven process, it is instantly connected to the network and no further technical intervention is required. Users and non-technical personnel can move a node almost anywhere it is needed, even outdoors or into other environments where traditional cabled networks will not go.

The carrier current communication system is a network administrators dream. It's completely transparent in its operation, and there is no added administration or support required.

When the carrier current system of communication is compared to other communication systems it stands out with the following advantages...

- It eliminates cabling and construction costs.
- Its connections requires only minutes to install.

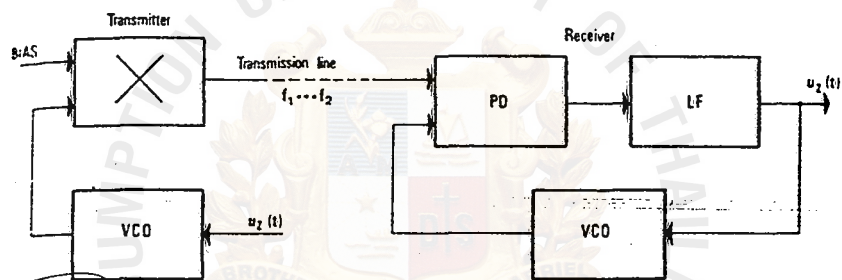


Fig. 7-26 Communication link using frequency modulation.

SINCE 1969
มหาวิทยาลัยอัสสัมชัญ

- It does not require added cost hubs or antennae.
- It does not require master stations or special ISA/PCMCIA cards.
- It does not disrupt staff or necessitate facility rearrangement.
- No special cabling.
- No special protocols.
- No special networking software.
- No special license.
- No special administrator or end-user training.
- Low-cost office / plant automation.
- Computer networking in historic buildings or cable-inaccessible areas.
- Mobile terminals and workstations
- Remote monitoring and access
- Energy management systems
- Remote Systems

Simply plug this device into your wall socket. Connect a PC, terminal or any other data device to the node and it's instantly connected.

This device uses a sophisticated technology that allows up to 7 bits of addressing which is 128 remote units to operate over the same power line system all with the same data integrity and reliability as a single two-node network. With the addition of a single modem and phone line you can link this device network to other LANs or WANs. Because it is not limited by line-of-sight restrictions, line infra-red, or broadcasting laws like radio frequency technology, power line networking is finding new applications all the time. Finally, anywhere you can run power, you can run our carrier current system.

Our other main concern is the safe use of our product, because our product uses the AC line as a medium, lethal voltages are present, which if not properly isolated within the circuit can cause serious damage not only to property but most important of to the life of the person using our product. We have used all the methods of safety isolation we know to make this circuit as safe and reliable to use as possible.

Chapter 1

Introduction To Power Line Communication

The term power line communications refers to a not quite so wireless form of wireless communications. Specifically, power line or "carrier-current" systems employ existing ac power lines to transfer information which would normally require additional hard wire installation. Carrier current systems are attractive because they re-use existing electrical connections within a building. Typical applications include remote control (which we are doing here), security systems, and low speed data networking. Due to the fact that power lines encounter very large inductances at the main transformers, a phenomenon that tends to attenuate all but very low frequencies, they are limited to a region within a local area which uses the same mains transformer.

Using the AC line as a medium is a better alternative than using radio frequency transmitted over the air because first of all we are interested only in a small particular building, we also do not want to cause any RFI or interfere with any other government or private agencies that may be transmitting over the air using the same or a frequency near to ours. In Thailand it is also illegal to transmit any signal over the air without proper permission from the Post and Telegraph Authority of Thailand. Because of the abundance and availability of the Electric Line we choose to take advantage of it.

In order to send intelligence, or in other words our signal into the AC line we must use a carrier signal which will transport our information to its destination. We will use the most reliable method of modulation that we have learned in our classes which is suited to our particular case. From our experience and gained knowledge all fingers point at FSK. We will discuss this type of modulation and its details in further detail later in this project.

We are lucky that National Semiconductor company has developed a special IC dedicated to the transmission and reception of signals

We are lucky that National Semiconductor company has developed a special IC dedicated to the transmission and reception of signals over the AC Electric line. UMC Semiconductors for their UM3750 Encoder/Decoder IC. Harris for their ICM7217CIPI real time clock Chip which very easily interfaced with the Atmel AT89C51 8-Bit Microcontroller of the MCS-51 family of Microcontrollers.

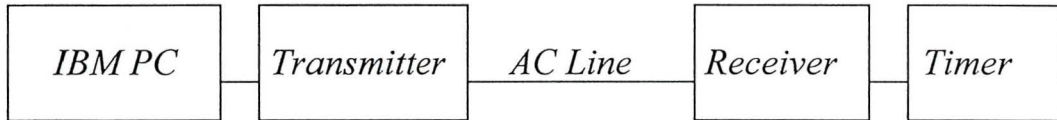
The Carrier Transmission System which we are going to use is not anything new. It has been used for many years in the electric industry. It is especially used when Electric Generating Plants communicate with each other. This means of communication is very reliable because it uses the high voltage AC transmission line instead of radio. This communication method also helps conserve Radio Spectrum Space. Another important factor is that through the utilization of this system of communication the electric power producing authorities can save a lot on communication costs.

The Carrier Current System does not generate RF which might cause interference with other communication systems. This method of transmission can be used for audio, data and even video type of modulation. The RF frequencies that it uses are in the range of 100 KHz till 500 KHz. Depending on the amount of accuracy or reproduction needed you can choose the type of modulation suited whether it be AM, FM or FSK to place information onto the carrier.

Short Description Of Project

This circuit interfaces the IBM PC Parallel Port with a Microcontroller based timer through the AC Line. The circuit consists of two main blocks. The transmitter which is a little circuit connected to the PC Parallel port. The next main part of the project is the receiver which is at some remote location within the same building utilizing the same mains transformer and within the same phase. The medium of data transmission is the AC line.

Main Block Diagram



Summary Of Various Parts Of The Block Diagram

1. This is the master controller. It is a microcomputer which will be at the center of control located in the central office. The Microcomputer is programmed in High Level Language. In our project we used Microsoft Foxpro and Borland's Turbo Pascal as the main languages. The computer operator will be able to turn on 128 timers located in remote locations within the operator's local area.

2. The transmitter is a circuit which comprises of the UM3750 encoder from UMC semiconductor company. This UMC chip will be instructed via the PC Parallel Port which of the 128 timers to turn on and for how long the timers should be turned on. The UMC chip will then send the data received from the PC Parallel Port which it has converted into serial form into the LM1893 Carrier Current Transceiver Chip. The LM1893 chip will then send this encoded data on to the AC line.

3. The AC line is the medium of data transfer.

4. The Receiver comprises of the LM1893 Carrier Current Transceiver and the UM3750 decoder chip. The LM1893 will receive the encoded signals of the ac line and send them over to the UM3750 chip which will see if it is the one out of the 128 addresses being called. If the address received and the preset addresses match the UM3750 will send a signal to interrupt the microcontroller based timer.

5. The microcontroller based timer will count the number of pulses sent by the receiver to determine how much time it should show on the display. The timer will then begin counting backwards from the time instructed by

the receiver. This microcontroller will then turn on a relay which will switch on some other electrical device within that remote location.

Existing Power Line Communications Standards

There are four major power line communication standards in use today: X-10, CEBus, LONWorks, and Smart House. It is important to note that while all of these standards support power line communications, most of them also support other communications media, such as Infrared (IR) and Radio Frequency (RF). Some of these standards are summarized in the table below.

- X-10
- CEBus (EIA IS-60)
- LONWorks
- Smart House
- Developer

X-10 (USA-Corp.) Electronics Industry Association (EIA).
Further developed by CEBusIndustry Council (CIC) Echelon Corp.
Testing and certification programs led by LONMark Inter operability Assoc. Smart House Limited Partnership (Smart House LP) for the National Association of Home Builders.

Mentioning these protocols and company names are just here for theoretical purposes and to acknowledge that such products already exist prior to the making to this project. In no way did we copy or use any of these existing protocols in our project.

Forecasted and Known Problems On Using This Carrier Current System

Since the transmitter operates in the 200-300 KHz range and is used to signals to a remote receiver via the AC power line. Either FM or AM modulation modes may be employed. FM is superior with regard to noise but AM modulation enables the use of simple low cost receivers. Effective

range depends mainly on the AC wiring and how it is connected in the building, the type of system employed (AM or FM) and the allowable signal to noise ratio, as well as the presence of any RF interference from sources such as motors, fluorescent lamps, triac and SCR operated devices (i.e. lamp dimmer switches), microprocessor devices, computer systems, and TV sets. The main culprit of line noise is the household television set which puts out a carrier of 15.7 KHz from the sweep circuits on to the ac line. All these devices can generate RF interference in the 200-300 KHz range. Another factor is the route the signal must take to the receiver, but most residential applications should experience no difficulty. In our project we use a low pass filter which we copied from a company that markets these readily available products to isolate the RF interference to our microcontroller based receiver.

Each factory, house or shop which might choose to use this product will have a different electrical lay out. This makes every electrical environment unique. We may not be able to expect the same results in two totally different electrical environments. Even the number and types of electrical devices connected up to the power line will be different in each situation providing us with another difficulty of varying impedance of the ac line. This varying impedance will make it difficult for us to have maximum power transfer at all times, since the impedance of the ac line is not constant. If we have many devices connected to the AC line at a present moment the impedance of the ac line may be very near short impedance.

Because of all this threat of noise on our ac line transmission medium we have agreed that we will use the FSK modulation method, which is much more reliable than other methods that we know of.

Chapter 2

The PC Parallel Port

We will attempt to describe interfacing to the IBM PC's parallel port in some detail here in this part of our report. The master controller is interfaced to the computer via its parallel port, so it is very essential that we define and understand properly the techniques of interfacing to the computer's parallel port. This information will be presented in a particular order in this report. First we will start with a description of the Standard Parallel Port (SPP), we will then advance on to hardware properties, giving the assigned port addresses. We will use the Parallel port to output 8 bits, which will also be covered. Before concluding we will list out how to use A Pascal Programming routine and a Foxpro program which will call upon the Pascal routine. I chose Foxpro because I am very familiar with it. The disadvantage of Foxpro is that it is not able to access the PC Parallel port. The Parallel Port is easily accessed in Pascal. Hence, I chose a combination of these two programming languages.

Introduction and Background of Parallel Ports

The Parallel Port is the most used port for interfacing home made projects. The reason behind is that The Parallel Port can be much more readily and easily interfaced than the PC RS-232 Port (The Serial Port). Writing software to control the parallel port is also much easier than using the serial port.

The Parallel Port will allow the output of 8 bits at any one given time. The port is composed of 4 control lines, 5 status lines and 8 data lines. We will only use the Output from the Data Lines in this project. The Parallel Port is found commonly on the back of your PC as a D-Type 25 Pin female connector. There may also be a D-Type 25 pin male connector. This will be a serial RS-232 port and is a totally different port, one which we will not even touch in the fabrication of this project.

Brief History On The Development Of The Parallel Port

Before 1994 there were no set standards as to how the Parallel Port should behave when connected to devices such as your humble printer, scanner, CD-ROM drive. Some may use TTL (Transistor to Transistor Logic) while others (more recent) may use CMOS (Complementary Metal Oxide Semiconductors) chips in their drivers.

The aim was to design new drivers and devices which were compatible with each other and also backwards compatible with the Standard Parallel Port (SPP). Compatibility, Nibble & Byte modes use just the standard hardware available on Parallel Port Cards while EPP & ECP modes require additional hardware which can run at faster speeds, while still being downwards compatible with the Standard Parallel Port.

Compatibility mode or "Centronics Mode" as it is commonly known, can only send data in the forward direction at a typical speed of 50 kbytes per second but can be as high as 150 kbytes a second. In order to receive data, you must change the mode to either Nibble or Byte Mode. Nibble Mode can input a nibble (4 bits) in the reverse direction. E.g. from device to computer. Byte mode uses the Parallel's bi-directional feature (found only on some cards) to input a byte (8 bits) of data in the reverse direction.

Hardware Properties

Below is a table of the "Pin Outs" of the D-Type 25 Pin Connector. The D-Type 25 pin connector is the most common connector found on the Parallel Port of the computer, while the Centronics Connector is commonly found on Printers. The IEEE 1284 standard however specifies 3 different connectors for use with the Parallel Port. The first one, 1284 Type A is the D-Type 25 connector found on the back of most computers. The 2nd is the 1284 Type B which is the 36 pin Centronics Connector found on most printers.

IEEE 1284 Type C is also a 36 conductor connector, like the Centronics, but smaller. This connector is claimed to have a better clip

latch, better electrical properties and is easier to assemble. It also contains two more pins for signals which can be used to see whether the other device connected, has power. 1284 Type C connectors are recommended for new designs, so we can look forward on seeing these new connectors in the near future.

Pin No (D-Type 25) Pin No (Centronics) SPP Signal Direction
In/out Register Hardware Inverted

- 1 Strobe In/Out Control
- 2 Data 0 Out Data
- 3 Data 1 Out Data
- 4 Data 2 Out Data
- 5 Data 3 Out Data
- 6 Data 4 Out Data
- 7 Data 5 Out Data
- 8 Data 6 Out Data
- 9 Data 7 Out Data
- 10 Ack In Status
- 11 Busy In Status
- 12 Paper-Out / Paper-End In Status
- 13 Select In Status
- 14 Auto-Line feed In/Out Control
- 15 Error / Fault In Status
- 16 Initialize In/Out Control
- 17 Select-Printer / Select-In In/Out Control
- 18 Gnd

Table 1. Pin Assignments of the D-Type 25 pin
Parallel Port Connector.

The Printer/Parallel Port has three commonly used addresses. These are listed in a Table below. The 3BCh base address is not typically used today, but was once used when the Parallel Port was contained on the video card. The address locations for LPT1 & LPT2 are typically 378h & 278h respectively. The lower case h denotes that it is in hexadecimal. These addresses may change from machine to machine, depending on what value is set up in the machined CMOS. you can also

change the address of your PC parallel port in the CMOS setting area of your computer before you boot up the system.

Address Notes:

3BCh - 3BFh Used for Parallel Ports which were incorporated on to Video Cards - Does not support ECP addresses
378h - 37Fh Usual Address For LPT 1
278h - 27Fh Usual Address For LPT 2 Table 2 Port Addresses

When the computer is first turned on, the BIOS (Basic Input/Output System) will determine the number of ports you have and assign device labels LPT1, LPT2 & LPT3 to them. BIOS first looks at address 3BCh. If a Parallel Port is found here, it is assigned as LPT1, then it searches at location 378h. If a Parallel card is found there, it is assigned the next free device label. This would be LPT1 if a card wasn't found at 3BCh or LPT2 if a card was found at 3BCh. The last port of call, is 278h and follows the same procedure than the other two ports. Therefore it is possible to have a LPT2 which is at 378h and not at the expected address 278h.

The assigned devices LPT1, LPT2 & LPT3 should not be a worry to people wishing to interface devices to their PC's. Most of the time the base address is used to interface the port rather than LPT1. However, should you want to find the address of LPT1 or any of the Line Printer Devices, you can use a look up table provided by BIOS. When BIOS assigns addresses to your printer devices, it stores the address at specific locations in memory, so we can find them.

Start Address Function

0000:0408 LPT1's Base Address

0000:040A LPT2's Base Address

0000:040C LPT3's Base Address

0000:040E LPT4's Base Address (Note 1) Table 3 - LPT Addresses in the BIOS Data Area;

Note 1 : Address 0000:040E in the BIOS Data Area may be used as the Extended Bios Data Area in PS/2 and newer Bioses.

The base address usually called the Data Port or Data register, is simply used for outputting data on the Parallel Port's data lines (Pins 2-9). This port is normally a write only port. If you read from the port, you should get the last byte sent. However if your port is bi-directional, you can receive data on this address. We will not present any information on the Bi-directional Ports here in this project.

Modulation & Demodulation

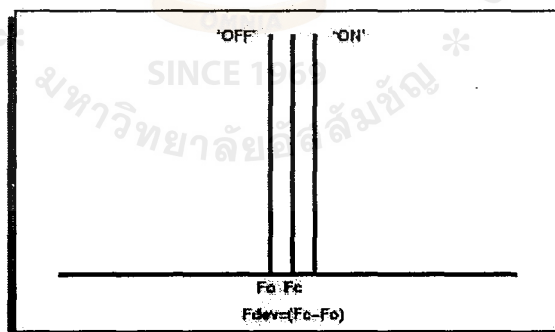
Modulation is the process of superimposing a low frequency such as audio or data content onto a high frequency. Modulation is used at the transmitting end, where as demodulation is used at the receiving end. Modulation helps us transmit information many times farther than it could have travelled by itself. For example sound, in the frequency range of 20 Hz till 20 KHz, can only travel a limited distance. Electromagnetic waves on the other hand can be transmitted through space and can travel great distances. We use this property of the Electromagnetic wave to our advantage. We attach our information on to this Electromagnetic wave. This process of attaching information on to the Electromagnetic wave is called modulation. We then transmit this Electromagnetic wave, which is called carrier, through to space and a receiver tuned to the same exact frequency will pick up this Electromagnetic wave. The receiver then works to separate out this carrier from the information. The carrier is filtered out and has completed it's function and is no longer of use. We then can process and use the information that we have received. The process of separating this carrier wave from the information is opposite to

the process of modulation, it is thus called demodulation. There are many methods of modulation available, we must however choose the cheapest and most suitable type of modulation to suit our particular need. We will not discuss modulation in greater detail because this subject is covered in many texts, any interested parties can refer to them.

FSK Modulation Theory

FSK modulation is a simplified form of FM. In true FM, an analog signal is represented by a linear frequency deviation from the center frequency. FSK is a binary form of FM that uses hard shifts between deviant frequencies to represent the data originally impressed on the carrier. The magnitude of frequency shift is directly related to the magnitude of the modulation source voltage.

The FSK modulation source is allowed two states: "on" and "off." When the modulation source is in an "off" state, the carrier frequency is shifted down from the center frequency. On the other hand, when the modulation source is in an "on" state, the carrier frequency is shifted up from the center frequency. The amount of carrier frequency shift is referred to as the frequency deviation.



In an FSK scheme, the amount of carrier frequency shift is referred to as the frequency deviation.

A carrier is always present with FSK modulation. This provides several benefits to the design engineer. First, the carrier will load the receiver at all

times--providing greatly increased noise immunity. Secondly, the strength (or amplitude) of the carrier can be used to determine the quality of the incoming signal. A received strength signal indicator (RSSI) circuit is used to make this determination. This circuit outputs a voltage that corresponds to signal strength and has a typical dynamic range of 70 to 90 dB.

But there are drawbacks to having a continuous carrier. One drawback is power consumption. Since the carrier is continuously operating, it will require high supply current to operate.

FSK is a non-return to zero modulation method. As a result, the carrier should never be at the center frequency when modulation is present.

The benefit of a non-return to zero approach is noise immunity. Hysteresis can be applied to the detector, eliminating the effect of spurious frequency modulation generated from sources other than the data stream.

Since FSK relies on frequency change, and not amplitude change, to indicate data states, an FSK-based receiver is inherently immune to amplitude noise. This is of great importance in bands that are extremely crowded and feature a high potential for near-band interference, such as the Industrial, Scientific, and Medical (ISM) bands. This increased noise immunity suggests a potential for higher data rates. In fact, data rates up to 100 kb/s can be readily achieved with FSK-based systems.

Although FSK systems are immune to amplitude noise, they are very sensitive to frequency noise. Unwanted frequency changes caused by in-circuit sources will ultimately lead to bit errors in the data stream.

As mentioned, simple hysteresis can be applied to the FSK detector to remove some of the frequency noise. But a stable frequency source must still be used to ensure good noise immunity. While SAW resonators work extremely well for low baud rate applications at lower frequencies, their inherent frequency inaccuracies make them poorly suited for FSK applications. Thus, a synthesized source based on a crystal reference must be used.

It is a well-known fact that crystals are superior to SAW resonators with regard to loaded Q and frequency accuracy. But crystals cannot be operated

in their fundamental mode at UHF. Instead, a crystal is used with a phase locked loop (PLL) to synthesize a high frequency. Although this technique is expensive and requires additional board space, it is the best method for attaining the tight frequency control necessary to achieve high data rates and noise immunity. It also provides the added benefit of channelization.

By using a divide-by-n PLL, the synthesized frequency can be set by changing the values of the internal counters. This allows an engineer to select a transmit or receive frequency from multiple channels. As a result, one transmitter or receiver can operate on many separate channels.



Theory of LM1893

The LM1893 Chip From National Semiconductor is the only chip the I know of that can send FSK or FM modulated signals on to the AC line using just a single chip. During the designing of this circuit while I was deciding to which chips to use I came across the LM1893 chip in the Maplin Electronics Catalog. This chip is designed to transfer data over the mains between two remote locations on site on the same phase. The chip performs as a power line interface for half-duplex (bi-directional) in transmission mode a sinusoidal carrier is FSK in modulated and impressed on almost any power line via a rugged on chip driver. In reception mode a PLL-based demodulator and impulse noise filter combined to give maximum range. Data speeds up to 4800 baud are possible with carrier frequencies in the range of 50 to 300 KHz.

A full data sheet downloaded from <http://www.national.com> has been made available for reference and can be found at the end of this report in the appendix section.

As for the design of the IF transformer was not necessary. We tried the commercially available IF BLACK 455 KHz transformer available from TOKO America.

In the Engineering Discipline as always, we will first start of with some calculations to determine the approximate value of the components which we will use during the experimental stage. The component values calculated will be different from the actual components we will use in our final design but they are necessary to establish some standard from where we can start experimenting.

Theory Of UM 3750 Decoder / Encoder Chip

The UM 3750 Decoder / Encoder chip is a chip with 12 address pins. Twelve pins gives 4096 addresses codes. Of the 12 pins we will use only 7 pins for addressing and 1 pin to trigger the UM 3750 chip to start transmitting. The reason for using this number of pins is that the PC parallel port can only output 8 data pins at one time. With a latch and other circuitry we could access all 12 address pins, by sending the data twice. In this circuit, however, for simplicity, lack of time and cost reduction sake we have chosen to use the 8 pins straight without any latching or any other fancy circuitry. The UM 3750 chip sends data serially on one line, this is exactly what we need to drive the LM1893 chip. It is also possible to design this same circuit without using this chip at all. Instead of using this chip we could have sent data from the PC serial port and at the decoding end we could have used a microcontroller to decode the serial data. Us being us, lazy and always looking for an easy way out chose this chip. The PC serial port involves a lot of interfacing experience and programming expertise to use. The Parallel port can be accessed in Pascal with using a 5 line source code program. Something that is an excuse for a data sheet can be found at the end of this project in the appendix section.

Theory of Microcontroller Timer and Display

You may ask why we choose to include and design our project around Microcontrollers. Well gone are the days when a complex project required a bag full of TTL chips, bread boards and millions of wires. The thing is that Hardware is expensive and software is cheap (only if you write it your self). Our project can then be easily modified by software without the need for extra hardware or soldering. Here we will use the AT89C51 chip which is a Microcontroller from the famous Intel family of microprocessors and microcontrollers. Here we will attempt to describe this MSC-51 family in some detail. The 8051 chip is also known as an embedded microcontroller. It is important that you first understand the difference between the word microprocessor and microcontroller. The microprocessor is the part of a computer without memory, I/O, and peripherals needed for a complete system. For example, 8088 and 80286 chips are microprocessors. All the other chips in the IBM PC add to the features not found in the microprocessor itself. The hardware designer can choose to implement from those features in different ways, although the designer has a choice of design at the end of the day it is still an IBM PC clone.

When a microprocessor is combined with I/O and memory peripherals functions, the combination is called a microcomputer. The fact that combining the CPU with memory and I/O products produces a microcomputer also holds true at the chip level. Generally speaking, microcomputer chips are designed for very small computer-based products that don't need all the functions of a full computer system. In cost-sensitive control applications, even a few chips that are needed to support a CPU like 8088 or Z80 are too many. Instead designers employ a single chip microcomputer to handle specific control activities. When single chip microcomputers are designed to be used in industrial control systems they are called microcontrollers. Basically there are no difference between microcomputers and microcontrollers, the name depends on how we use them.

Frequently microcontrollers are used to replace circuit functions that often require too many low-level chips. The IBM PC keyboard is a prime example of the use of a microcontroller chip.

The Intel 8051 chip is a classic microcontroller (it is a generation more advanced than the 8742) is a true single chip microcomputer containing parallel I/O, counters and timers, serial I/O, RAM and Flash Eprom. There are many different versions of this microcontroller but we chose to use the ATME1 8051 Flash Microcontroller because of its cheap price, wide availability, easy programming and easy re-programming. The 8051 contains 4K bytes of RAM which will hold the program and its system variables.

Using the 8051 chip is as simple as hooking up the power supply and a clock crystal. We also must remember that a single chip microcontroller replaces all the digital logic you would normally use for control, timing and so forth. You need only to add the keyboard, displays, switches, relays and other specific I/O that actually makes up the final product.

A single I/O port can scan a 16 key matrix. With an additional output bit it can drive a 2-line by 20 character smart liquid display at the same time. The remaining I/O bits can handle triacs of power FETS for AC or DC control. Burn a program into the microcontroller's flash and you have a real time power controller. Run the serial port through a MAX121 RS-232C level converter, and you have a standard serial port for remote control or status monitoring at your master computer.

If you don't need the serial port, counters, timers, and external interrupts the 8051 can use those bits as another I/O port. The point of this is that the "computer" part of your system need not require elaborate hardware. For a unit of reasonable size you will spend most of your time on the I/O devices rather than the 8051 circuit.

The main benefit of using a microcontroller is the ease in adding new features to your system, just by changing the program, not changing the circuit board connections you can give your system a completely new personality. Try doing that with a board full of TTL control logic!

Now to come to the software part. If you have ever written or are familiar with assembly language programming for any microprocessor you will find that the 8051 will have many same instructions. There is however a big difference in internal and external memory addressing. In this project we will only use internal memory addressing so this will be discussed no further.

To go into greater detail of the internal memory of the microcontroller we will explain the four types of addressing here. There are four addressing modes direct, intermediate register, and register indirect. Direct mode embeds an internal address in the instruction. Immediate mode uses the data value itself. Register and register indirect use a register number, with indirect addressing taking the contents of that register as a direct address to access the data.

The 8051 has a single accumulator called ACC or A depending on the use of the instruction. Nearly all instructions use the accumulator in one way or another.

Because the microcontroller applications require handling at least few I/O bits, the 8051 has a rich selection of bit manipulation instructions that are completely separate from standard byte instructions. A single instruction set can set, clear, compliment or copy any bit in internal data memory. The on chip I/O ports show up in that address space, so there is no need for the "read, mask, set, combine, write" instructions found in most other microprocessors.

Unlike the intel 8088 or Z80 microprocessor families, the 8051 has no explicit I/O instructions. The on chip I/O ports are mapped into the internal data memory-address space and accessed with the same MOV instruction used for other transfers.

There is however an ugly side of microcontrollers is that of getting the software to work. But thanks to the special debugger I borrowed off my friend I can debug programs on my PC and immediately upload them into the debugger and test my program out. I can keep doing that until my program works perfectly. Also using a logic probe and an oscilloscope helps a lot. With this debugger you can use program breakpoints to stop execution at specific 8051 instructions or when a given condition

occurs. Also, since the debugger records each particular variable you can examine the contents of the variable.

After debugging the program I programmed the embedded microcontroller with a ACP programmer which was available for use in The Network Research Center 4th Floor E-Building Assumption University. This programmer is a handy one because it can be programmed by a PC or programmed directly into it's keyboard. The programmer was purchased in Ban Moh in China Town from a shop called Electronics Source LTD. The price of this programmer was approximately 8,000 Bahts, that was before the US dollar sky rocketed to 50 Bahts.

A detailed data sheet of the Microcontroller from Atmel Electronics which is used in this project can be found at the appendix at the end of this project.

Timer Circuit Description

Now it is time to explain how the timer circuit we designed works. This is a behind the scenes view of what happens after the microcontroller is interrupted. Before getting into the details of the program we will first discuss the working of the ICM7217CPI counter chip.

Without the ICM7217CPI chip from Harris Semiconductors, driving and multiplexing 4 seven segment displays is no easy job. Thanks to Harris, this counter chip is very easily interfaced to our microcontroller. The chip has a special ZERO output pin which is active low. This pin will go low if the number that is displayed on the seven segment display is zero. There is a count up/down mode pin which if high sets the chip into count up mode and if low will set the chip into count down mode. If we send pulses to the count pin the counter will count up or down one pulse depending whether the mode pin has been set to count up or down. This chip will multiplex 4 seven segment displays by itself with no additional circuitry. Basically all our microcontroller is doing in this circuit is providing the right information in pulses, count mode and resetting the ICM7217CPI chip.

Now I will describe in plain English what the assembly program that is contained in the microcontroller is doing. Our microcontroller works at very

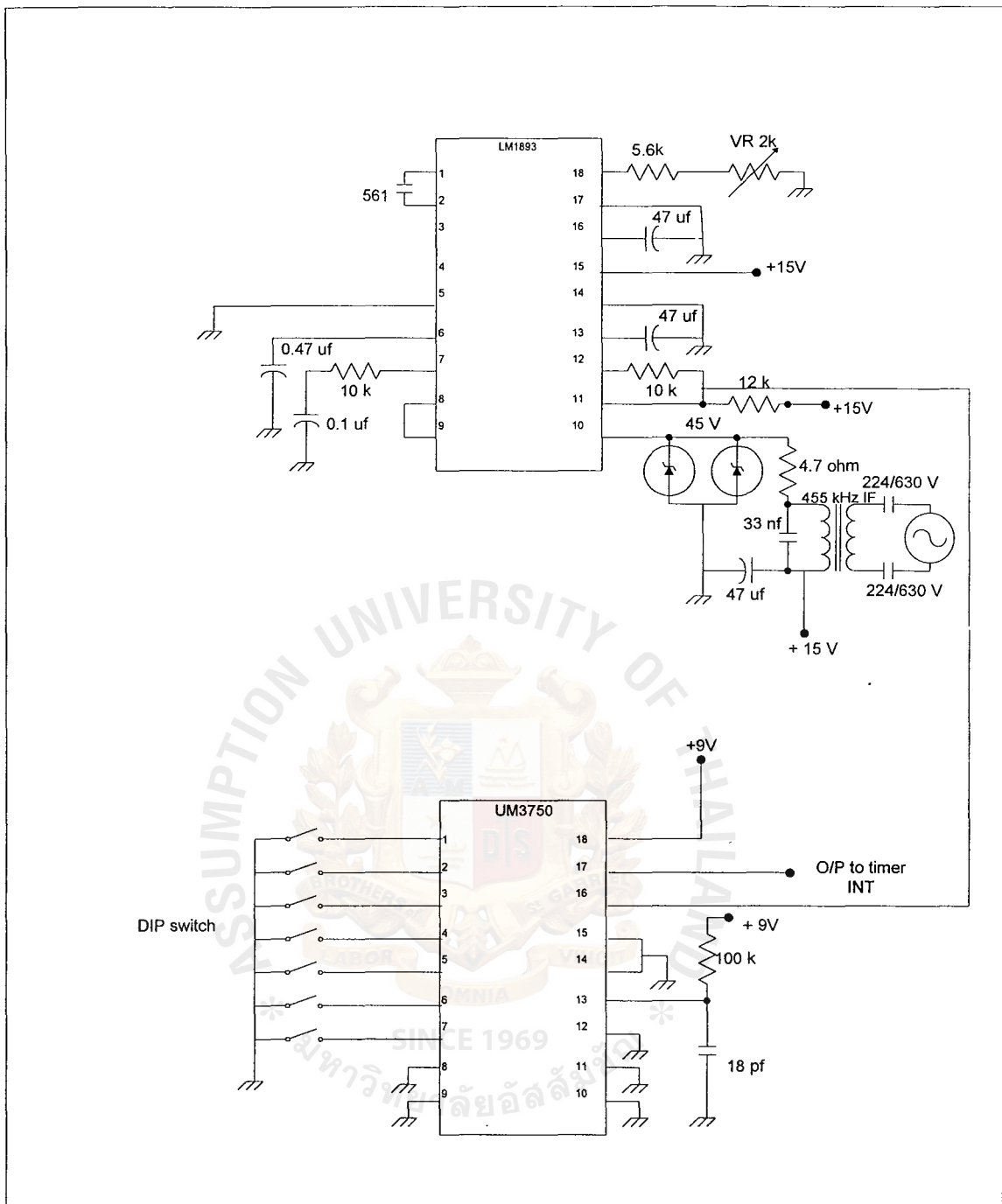
high speed, in this circuit the crystal clock frequency is 11.0592 Mhz. The first section of the program there is a delay, this delay is there so that the ICM7217CPI can get up on its feet and get ready to run. The program then sends a pulse which goes from high to low and goes back to high to reset the ICM7217CPI. This pulse is sent out of pin 4 of the microcontroller to pin 14 of the ICM7217CPI chip. We then disable all external interrupts just in case any were set up in the starting up of the chip. We then proceed to clear the values in various addresses before we set the timer mode. We then define the hardware interrupt procedure. This procedure first will debounce the interrupt that is provide a small delay. We then start off the timer so that it will provide a software interrupt every one minute. After that the microcontroller is instructed to read the input of the dip switch to see how many pulses it should send to the count pin. The microcontroller then sends via pin its pin 2 to pin 10 of ICM7217CPI to send it to count up mode. It then sends a pulse train via its pin 1 to pin 8 of ICM7217CPI to tell it to count up to the value set on the dip switch. Every one minute the software interrupt is serviced, here it will first check pin 21 of microcontroller if it is not low the microcontroller will set the ICM7217CPI into count down mode and will send one pulse to make the ICM7217CPI count down. If the input on pin 21 is low the program will reset the ICM7217CPI and will cut the power from the relay.

Chapter 3

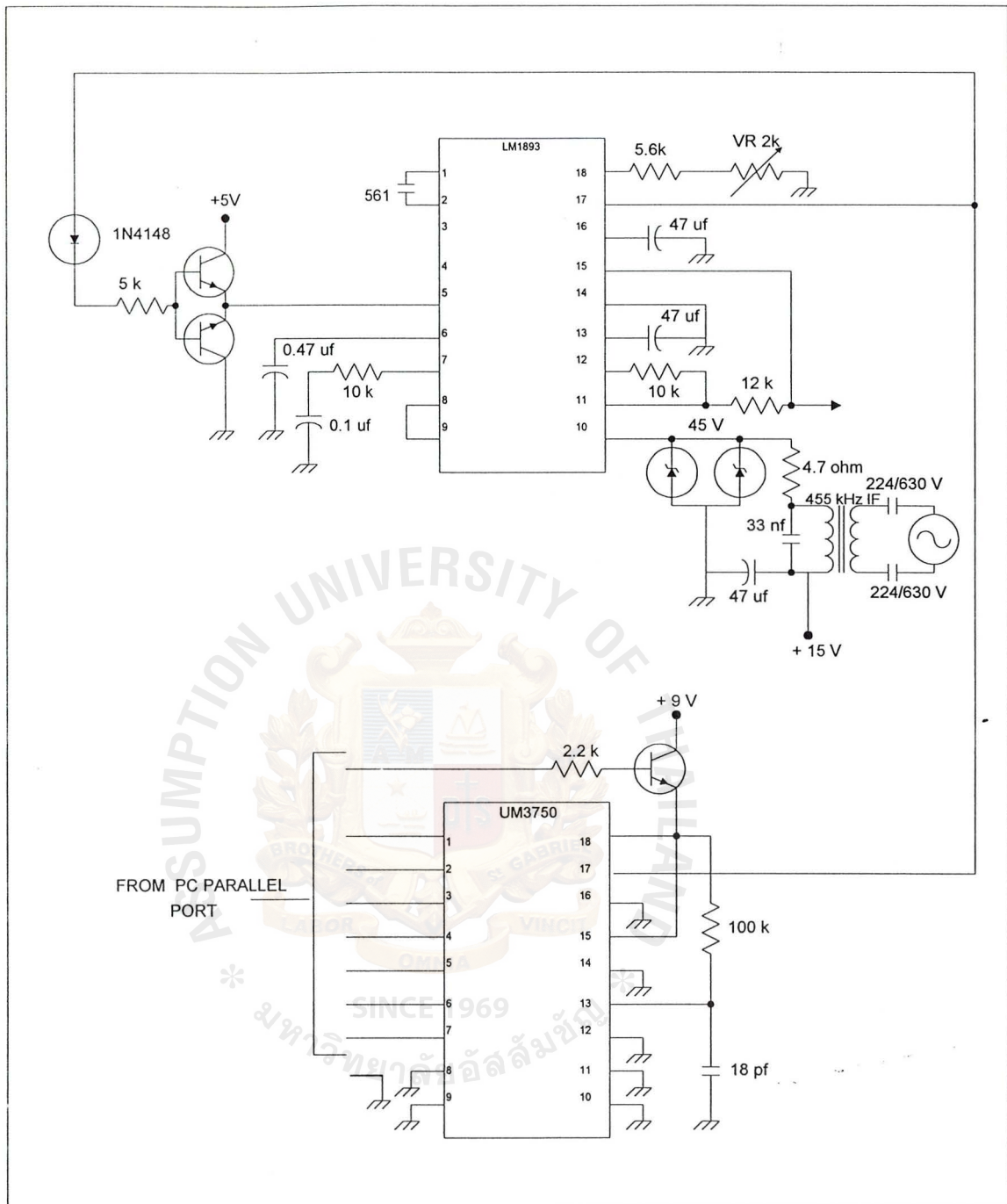
Schematic Diagrams in this Chapter

- Schematic Diagram Microcontroller Based Timer
- Schematic Diagram Receiver
- Schematic Diagram Transmitter





SCHEMATIC OF LM1893 AC LINE RX WITH UM3750 DECODER



SCHEMATIC OF LM1893 AC LINE TX WITH UM3750 ENCODER

Chapter 4

Pascal & The PC Parallel Port

This program will output the decimal value of 85 on to the Parallel Port for one second then output the value on the Parallel Port to the decimal value 0.

```

Program Parallel(input, output);
Uses Dos,Crt;
Begin
    PORT[$378]:=85;
    DELAY(1000);
    PORT[$378]:=0;
end.

```

Foxpro Program Source Code

```

*****
*:
*:
*: Procedure file: C:\FOXPRO\ACLINE\MAIN.PRG
*:
*:
*:      System: Data Communication On Electric Line
*:      Author: Cherdchai J(361-6310) Suvir K(361-6898)
*:      Copyright (c) 1998, ABAC EN 4902 Engineering Project II
*:      Last modified: 03/15/98    15:06
*:
*:
*: Procs & Fncts: EXIT
*:
*:
*:      Calls: SET_SETS          (procedure in SET_SETS.PRG)
*:              : EXIT          (procedure in MAIN.PRG)
*:              : DEV1.PRG
*:              : BIGLETT()      (function in BIGLETT.PRG)
*:              : UNTALK()       (function in UNTALK.PRG)
*:
*:

```

*: Documented 03/15/98 at 17:22

FoxDoc version 2.10f

*:*****

inmain=.T.

DO set _sets

SET ESCAPE OFF

SET SYSMENU TO

ON ESCAPE SET SYSMENU TO DEFA

SET SYSMENU AUTOMATIC

PUBLIC m.company

m.company= " Data Transmission On AC Line Project "

m.company1=" Electronics & Engineering Project II "

m.company2=" Cherdchai Jungsatitkul 361-6310 "

m.company3=" Suvir Kumar 361-6898 "

DEFINE PAD _qoi11lm1o OF _msysmenu PROMPT "Turn On Device"

COLOR SCHEME 3

DEFINE PAD _qoi11lmbx OF _msysmenu PROMPT "E\<xit Program "

COLOR SCHEME 3

ON PAD _qoi11lm1o OF _msysmenu ACTIVATE POPUP employee

ON SELECTION PAD _qoi11lmbx OF _msysmenu DO EXIT

DEFINE POPUP employee MARGIN RELATIVE SHADOW COLOR
SCHEME 4

DEFINE BAR 1 OF employee PROMPT "Device \<One"

DEFINE BAR 2 OF employee PROMPT "Device \<Two "

DEFINE BAR 3 OF employee PROMPT "Device T\<hree"

DEFINE BAR 4 OF employee PROMPT "Device \<Four"

DEFINE BAR 5 OF employee PROMPT "Device F\<ive"

ON SELECTION BAR 1 OF employee DO dev1

MAIN_PROGRAM

ON SELECTION MENU _msysmenu

CLEAR WINDOWS ALL

CLEAR

=biglett(02,1,'DATA TX')

=biglett(11,1,'AC LINE')

[illegible]

31

31

31

31

[illegible]

(@ 20,(40-(LEN(ALLTRIM(m.company1))/2)) SAY

(@ 21,(40-(LEN(ALLTRIM(m.company2))/2)) SAY

@ 22,(40-(LEN(ALLTRIM(m.company3))/2)) SAY

ALLTRIM(m.company3)

USE

```
=untalk()
```

CLEAR WINDOWS

SET SAFETY OFF

ACTIVATE MENU `msysmenu`

ENDDO

* 1

*! Procedure: EXIT

* |

```
*!      Called by: MAIN.PRG
```

* 1

PROCEDURE EXIT

FOR i = 1000 TO 1500 STEP 200

SET BELL TO i,1

?? CHR(7)

ENDFOR

inmain=.F.

SET SYSMENU TO DEFA

```

CLEAR WINDOWS ALL
RELEASE ALL
*quit
RETURN
*: EOF: MAIN.PRG

```

```

*.*****
*:
*:
*: Procedure file: C:\FOXPRO\ACLINE\SET_SETS.PRG
*:
*:
*:   System: Data Communication On Electric Line
*:   Author: Cherdchai J(361-6310) Suvir K(361-6898)
*:   Copyright (c) 1998, ABAC EN 4902 Engineering Project II
*:   Last modified: 05/20/94   9:43
*:
*:
*: Procs & Fncts: SET_SETS
*:
*:   Documented 03/15/98 at 17:22           FoxDoc version 2.10f
*.*****
*!*****
*!
*!   Procedure: SET_SETS
*!
*!   Called by: MAIN.PRG
*!
*!*****
PROCEDURE set_sets

```

```

*****
* DO set_sets
* Version # 1.0 FP      Date: 02-05-90
* Programmed by: Malcolm C. Rubel
*
* Copyright (c) 1990
* Performance Dynamics Associates
* All Rights Reserved
*

```


- * Note: SET_SETS sets all sets to the setting to which
- * they should be set when you set out to set up your
- * application. Set it in your mind that some of the sets
- * are not set to the standard setting for sets.

SET ALTERNATE OFF

SET ALTERNATE TO

*SET AUTOSAVE on

SET BELL TO 440,2 && not the normal tone

SET BELL OFF

SET BLINK OFF

SET BLOCKSIZE TO 64

SET BORDER TO && single line border

SET BRSTATUS OFF

SET CARRY OFF

SET CENTURY OFF

SET CLEAR ON

SET CLOCK OFF

SET COMPATIBLE OFF

SET CONFIRM OFF

SET CONSOLE ON

SET CURRENCY TO && dollar default

SET CURRENCY LEFT

SET CURSOR ON

SET DATE BRITISH && British default

*SET DEBUG off

SET DECIMALS TO 2

SET DELETED ON

SET DELIMITERS TO '[' && not the default

SET DELIMITERS OFF && but do not use it

SET DEVELOPMENT ON && Crazy About You OUI

SET DEVICE TO SCREEN

SET DOHISTORY OFF

SET ECHO OFF

SET ESCAPE OFF

SET EXACT ON

SET EXCLUSIVE OFF

SET FIELDS TO

SET FIELDS OFF

SET FIXED ON && not a default
 SET FORMAT TO
 SET FULLPATH ON

 SET FUNCTION 1 TO *
 SET FUNCTION 2 TO * && clears function key
 SET FUNCTION 3 TO * && assignments
 SET FUNCTION 4 TO *
 SET FUNCTION 5 TO *
 SET FUNCTION 6 TO *
 SET FUNCTION 7 TO *
 SET FUNCTION 8 TO *
 SET FUNCTION 9 TO *
 SET FUNCTION 10 TO *

 IF FKMAX() = 12 && twelve function keys
 SET FUNCTION 11 TO *
 SET FUNCTION 12 TO *
 ENDIF

 SET HEADING OFF && not a default
 SET HELP ON
 SET HISTORY OFF
 SET HOURS TO 12
 SET INTENSITY ON
 SET LOGERRORS OFF
 SET MARGIN TO 10 && not a default
 SET MARK TO '/'
 SET MEMOWIDTH TO 50
 SET MESSAGE TO 24
 SET MOUSE TO 5
 SET MOUSE ON
 SET NEAR ON
 SET NOTIFY ON
 SET ODOMETER TO 100
 SET POINT TO '!'
 SET PRINTER OFF
 SET SAFETY OFF && not a default
 SET SCOREBOARD OFF

```

SET SEPARATOR TO ','
SET SHADOWS ON
SET SPACE ON
SET STATUS OFF
*SET STEP off
SET STICKY ON
SET sysmenus TO DEFA
SET SYSMENU OFF
SET TALK OFF
SET TITLE OFF
SET TOPIC TO
SET TYPEAHEAD TO 20

```

```

IF VERSION() > 'FoxPro 1.01')
  SET UDFPARMS TO VALUE && version 1.02 command
ENDIF

```

```

SET UNIQUE OFF
= INSMODE(.T.)
= CAPSLOCK(.F.)
= NUMLOCK(.T.)

```

```

RETURN

```

```

*: EOF: SET_SETS.PRG

```

```

*.*****

```

```

*.:

```

```

*.:   Program: C:\FOXPRO\ACLINE\DEV1.PRG

```

```

*.:

```

```

*.:   System: Data Communicaiton On Electric Line

```

```

*.:   Author: Cherdchai J(361-6310) Suvir K(361-6898)

```

```

*.:   Copyright (c) 1998, ABAC EN 4902 Engineering Project II

```

```

*.: Last modified: 03/15/98   15:36

```

```

*.:

```

```

*.:   Called by: MAIN.PRG

```

```

*.:

```

```

*.:   Calls: WEXPLODE()      (function in WEXPLODE.PRG)

```

```

*.:       : BIGLETT()      (function in BIGLETT.PRG)

```

```

*.:       : YESNO()        (function in YESNO.PRG)

```

```

*.:       : WIMPLODE()     (function in WIMPLODE.PRG)

```

```

*:
*:   Documented 03/15/98 at 17:22           FoxDoc version 2.10f
*: *****
=wexplode('abac',1,0,24,79,'Turn On Device One')
=biglett(3,0,'Device')
=biglett(13,0,'One')
choice=yesno('Turn On Device One')
IF choice=.T.
    ! device1.exe
ENDIF
=wimplode('abac','Turn On Device One')
RETURN
*: EOF: DEV1.PRG
*: *****
*:
*: Procedure file: C:\FOXPRO\ACLINE\WEXPLODE.PRG
*:
*:   System: Data Communicaiton On Electric Line
*:   Author: Cherdchai J(361-6310) Suvir K(361-6898)
*:   Copyright (c) 1998, ABAC EN 4902 Engineering Project II
*:   Last modified: 03/21/94   20:43
*:
*: Procs & Fncts: WEXPLODE()
*:
*:   Documented 03/15/98 at 17:22           FoxDoc version 2.10f
*: *****
*: *****
*!
*!   Function: WEXPLODE()
*!
*!   Called by: DEV1.PRG
*!
*!   Calls: POPERROR()      (function in POPERROR.PRG)
*!
*: *****
FUNCTION wexplode
PARAMETERS w_name, ul_rr, ul_cc, lr_rr, lr_cc, b_type;
    b_title, c_scheme
PRIVATE w_name, ul_rr, ul_cc, lr_rr, lr_cc, b_type, ;

```



```

    b_type, c_scheme
PRIVATE mid_rr, mid_cc, rr_it, cc_it, max_it, b_start
PRIVATE rr_incr, cc_incr, i, b_incr, pcount, rvalue

```

```

*****
* wexplode(<expC1>,<expN1>,<expN2>,<expN3>,<expN4>;
*          [,<expC2>][,<expC3>[,<expN5>]])
* Version # 2.1      Date: 08-29-91
* Programmed by: Malcolm C. Rubel
*
* Copyright (c) 1990,91
* Performance Dynamics Associates
* All Rights Reserved
*
* Note: Function takes window name, window coordinates,
* and optionally the window type and explodes the window
* up to that size. Function returns the name of the
* window that was active before the window exploded on
* screen. If no window was active, the function returns
* a null value.
* Modified 10-1-90 to include a color scheme choice.
* Modified 1-23-91 to reduce the use of macro expansion
* to a minimum.
* Modified 8-29-91 to change WONTOP to WOUTPUT.
*****

```

```

pcount = PARAMETERS()    && how many were passed
rvalue = WOUTPUT()       && active window

```

```

IF pcount < 5             && not enough parameters
    = poperror('Not enough parameters passed to WEXPLODE. '+'
    'Window will not pop.')
    RETURN(rvalue)
ENDIF

```

```

IF pcount = 5
    b_type = "
    c_scheme = 1
ENDIF

```

IF pcount = 6

IF TYPE('b_type') = 'C'

IF LEN(b_type) = 1

b_type = UPPER(b_type)

b_title = "

c_scheme = 1

ELSE

b_title = b_type

b_type = "

c_scheme = 1

ENDIF

ELSE

IF TYPE('b_type') = 'N'

b_type = "

b_title = "

c_scheme = b_type

ENDIF

ENDIF

ENDIF

IF pcount = 7

IF TYPE('b_title') = 'N'

c_scheme = b_title

b_title = "

ENDIF

ENDIF

b_type = UPPER(b_type)

DO CASE

```
CASE b_type = 'D'  
  b_type = 'DOUBLE'
```

```
CASE b_type = 'P'  
  b_type = 'PANEL'
```

```
OTHERWISE  
  b_type = "
```

```
ENDCASE
```

```
*** first find the screen coordinates for the middle of the  
*** box for both row and column
```

```
mid_rr = ul_rr + INT((lr_rr - ul_rr)/2)  
mid_cc = ul_cc + INT((lr_cc - ul_cc)/2)
```

```
*** how many 'steps' will we have to take in both the x  
*** and y axes to 'grow' the box to its full size
```

```
rr_it = INT((lr_rr - ul_rr)/2)  
cc_it = INT((lr_cc - ul_cc)/2)
```

```
*** if the box is greater than the minimum size that makes  
*** exploding worthwhile
```

```
IF rr_it >= 4 .AND. cc_it >= 4
```

```
*** which is larger the x or y axis. use the larger axis  
*** to control the explosion.
```

```
max_it = IIF(rr_it > cc_it, rr_it, cc_it)  
b_start = INT(max_it/4)    && where to start from  
b_incr = CEILING(max_it/5) && what 'grow' increment
```

```
*** explode the window in steps
```

```
FOR i = b_start TO max_it - 2 STEP b_incr
```

```
rr_incr = INT(rr_it*(i/max_it))
cc_incr = INT(cc_it*(i/max_it))

DEFINE WINDOW (w_name) ;
  FROM mid_rr-rr_incr,mid_cc-cc_incr;
  TO mid_rr+rr_incr, mid_cc + cc_incr;
  &b_type COLOR SCHEME c_scheme
ACTIVATE WINDOW (w_name)

= INKEY(.01)      && pause just a bit

ENDFOR

ENDIF

*** now activate the real window!

b_title = IIF(EMPTY(b_title),'TITLE "' + b_title + '"')

DEFINE WINDOW (w_name) FROM ul_rr, ul_cc TO lr_rr,lr_cc ;
  &b_type &b_title COLOR SCHEME c_scheme
ACTIVATE WINDOW (w_name)

RETURN(rvalue)
*: EOF: WEXPLODE.PRG
*.:
*.: *****
*.:
*.: Procedure file: C:\FOXPRO\ACLINE\WIMPLODE.PRG
*.:
*.:   System: Data Communictaion On Electric Line
*.:   Author: Cherdchai J(361-6310) Suvir K(361-6898)
*.:   Copyright (c) 1998, ABAC EN 4902 Engineering Project II
*.:   Last modified: 09/12/91   0:00
*.:
*.: Procs & Fncts: WIMPLODE()
*.:
*.:   Documented 03/15/98 at 17:22           FoxDoc version 2.10f
*.: *****
*.: *****
```



```

*!
*!   Function: WIMPLODE()
*!
*!   Called by: DEV1.PRG
*!
*!*****
FUNCTION wimplode
PARAMETERS w_name, b_type, c_scheme
PRIVATE w_name, b_type, c_scheme
PRIVATE mid_rr, mid_cc, rr_it, cc_it, max_it, b_fin, rr_incr
PRIVATE cc_incr, b_incr, lr_rr, lr_cc, ul_rr, ul_cc, pcount
PRIVATE i, rvalue

*****
* wimplode(<expC1>[,<expC2>][,<expN>])
* Version # 2.1      Date: 08-29-91
* Programmed by: Malcolm C. Rubel
*
* Copyright (c) 1990,91
* Performance Dynamics Associates
* All Rights Reserved
*
* Note: Function takes window name, and optionally, the
* window type, and implodes the window. Function returns
* the name of the window that was active when the
* function was called.
* Modified 10-1-90 to include a color scheme choice.
* Modified 1-23-91 to reduce the use of macro expansion
* to a minimum.
* Modified 8-29-91 to change WONTOP to WOUTPUT.
*****

pcount = PARAMETERS()      && how many were passed
rvalue = WOUTPUT()         && active window

IF pcount = 1
  b_type = "
  c_scheme = 1
ENDIF

```

IF pcount = 2

```
IF TYPE('b_type') = 'C'
  b_type = UPPER(b_type)
  c_scheme = 1
ELSE
```

```
  IF TYPE('b_type') = 'N'
    b_type = "
    c_scheme = b_type
  ENDIF
```

```
ENDIF
```

```
ENDIF
```

```
DO CASE
```

```
CASE b_type = 'D'
  b_type = 'DOUBLE'
```

```
CASE b_type = 'P'
  b_type = 'PANEL'
```

```
OTHERWISE
  b_type = "
```

```
ENDCASE
```

*** find out if the named window is the active window. If
*** it is not, activate it before imploding it.

```
IF WONTOP() # UPPER(w_name)
  ACTIVATE WINDOW (w_name)
ENDIF
```

*** get the row and column coordinates for the window.

```

ul_rr = WLROW()          && upper left hand corner
ul_cc = WLCOL()          && upper left hand corner
lr_rr = ul_rr + WROWS()  && lower right corner
lr_cc = ul_cc + WCOLS()  && lower right corner

*** first find the screen coordinates for the middle of the
*** box for both row and column

mid_rr = ul_rr + INT((lr_rr - ul_rr)/2)
mid_cc = ul_cc + INT((lr_cc - ul_cc)/2)

*** how many 'steps' will we have to take in both the x
*** and y axes to implode the box

rr_it = INT((lr_rr - ul_rr)/2)
cc_it = INT((lr_cc - ul_cc)/2)

*** if the box is greater than the minimum size that makes
*** imploding worthwhile

IF rr_it >= 4 .AND. cc_it >= 4

*** which is larger the x or y axis. use the larger axis
*** to control the implosion.

max_it = IIF(rr_it > cc_it, rr_it, cc_it)
b_fin = INT(max_it/4)    && where to start from
b_incr = -(CEILING(max_it/5)) && what implode increment

*** implode the window in steps

FOR i = max_it - 2 TO b_fin STEP b_incr
  rr_incr = INT(rr_it*(i/max_it))
  cc_incr = INT(cc_it*(i/max_it))

  DEFINE WINDOW (w_name) FROM mid_rr-rr_incr,mid_cc-cc_incr;
  TO mid_rr+rr_incr, mid_cc + cc_incr;
  &b_type COLOR SCHEME c_scheme
  ACTIVATE WINDOW (w_name)

```

```

        = INKEY(.01)          && pause just a bit

    ENDFOR

ENDIF

*** now activate the real window!

RELEASE WINDOW (w_name)

RETURN(rvalue)
*: EOF: WIMPLode.PRG
*!*****
*!
*! Procedure file: C:\FOXPRO\ACLINE\YESNO.PRG
*!
*!      System: Data CommunicatIon On Electric Line
*!      Author: Cherdchai J(361-6310) Suvir K(361-6898)
*!      Copyright (c) 1998, ABAC EN 4902 Engineering Project II
*!      Last modified: 09/12/91    0:00
*!
*! Procs & Fncts: YESNO()
*!
*!      Documented 03/15/98 at 17:22          FoxDoc version 2.10f
*!*****
*!*****
*!
*!      Function: YESNO()
*!
*!      Called by: DEV1.PRG
*!
*!      Calls: POPERROR()      (function in POPERROR.PRG)
*!
*!*****
FUNCTION yesno
PARAMETERS s_row, s_col, bx_mess
PRIVATE s_row, s_col, bx_mess, num_lines, cur_width, e_mess
PRIVATE i, m_col, yes_on, _temp, cur_win, rvalue

```

* yesno([<expN1>,[<expN2,][<expC>])

*

* Version # 2.2 FP Date: 08-29-91

* Programmed by: Malcolm C. Rubel

*

* Copyright (c) 1990,91

* Performance Dynamics Associates

* All Rights Reserved

*

* Note: Function creates a dialog box in the middle of
* the screen, paints the message passed in <expC> and
* puts up two choices, "Yes" and "No", with "Yes" being
* the default. Function returns logical TRUE if the
* user selects "Yes", and FALSE if they select "No". The
* function returns TRUE if the user presses Ctrl + Enter
* no matter what prompt is currently selected.

* Modified 10-16-90 to make the mouse work properly.

* Function now uses no READ and no menu to get response.

* Modified 11-29-90 to add row and column movement.

* Modified 1-21-91 to take out macro expansion.

* Modified 7-20-91 to clear ON KEY LABELs with PUSH KEY

* CLEAR/POP KEY.

* Modified 8-29-91 to use WOUTPUT to control windows.

PUSH KEY CLEAR

rvalue = .F.

e_mess = 'Invalid parameters passed to the function '+';

'YESNO. Function will return FALSE.'

cur_win = WOUTPUT()

DO CASE

CASE PARAMETERS() = 0 && no parameter passed

s_row = 9

s_col = 16

bx_mess = 'Your choice.....'

CASE PARAMETERS() = 1

```
IF TYPE('s_row') = 'C'
    bx_mess = s_row
    s_row = 9
    s_col = 16
ELSE
    IF TYPE('s_row') = 'N'
        s_col = 16
        bx_mess = 'Your choice.....'
    ELSE
        = poperror(e_mess)
        POP KEY
        RETURN(.F.)
    ENDIF
ENDIF
```

CASE PARAMETERS() = 2

```
IF TYPE('s_row') = 'N' .AND. TYPE('s_col') = 'C'
    bx_mess = s_col
    s_col = 16
ELSE
    IF TYPE('s_row') = 'N' .AND. TYPE('s_col') = 'N'
        bx_mess = 'Your choice.....'
    ELSE
        = poperror(e_mess)
        POP KEY
        RETURN(.F.)
    ENDIF
ENDIF
```

CASE PARAMETERS() = 3

```

IF TYPE('s_row') # 'N' .OR. TYPE('s_col') # 'N' .OR. ;
    TYPE('bx_mess') # 'C'
    = poperror(e_mess)
    POP KEY
    RETURN(.F.)
ENDIF

OTHERWISE                && real bad parameters
    = poperror(e_mess)
    POP KEY
    RETURN(.F.)
ENDCASE

cur_width = SET('memowidth')

*** paint the message that is to appear at the top
*** of the dialog box.

IF LEN(bx_mess) <= 40      && if message is one line
    num_lines = 1
ELSE                      && if message is 2+ lines
    SET MEMOWIDTH TO 40
    num_lines = MEMLINES(bx_mess)
ENDIF

optcolor = SCHEME(2,6)    && for the option choices
hotcolor = SCHEME(2,7)    && for the hotkeys

*** make sure that everything fits on the screen!

s_row = IIF(s_row+5+num_lines<25,s_row,24-5-num_lines)
s_col = IIF(s_col<33,s_col,32)

DEFINE WINDOW yesno FROM s_row,s_col TO ;
    s_row+5+num_lines,s_col+47 ;
    DOUBLE COLOR SCHEME 1
ACTIVATE WINDOW yesno

IF num_lines = 1

```

```

    @ i,03 SAY PADC(bx_mess,40)
    i = 3
ELSE

    FOR i = 1 TO num_lines
        @ i,03 SAY MLINE(bx_mess,i)
    ENDFOR

    i = i + 1
ENDIF

@ i,07 SAY CHR(174) + ' Yes ' + CHR(175)
@ i,29 SAY '< No >'
SET COLOR OF NORMAL TO (hotcolor)
@ i,10 SAY 'Y'
@ i,32 SAY 'N'
SAVE SCREEN TO _temp

yes_on = .T.          && starting condition
KEY = 0

DO WHILE .T.

    DO CASE

        CASE KEY = 151          && if mouse button pressed
            m_col = MCOL()

            DO CASE

                CASE MROW() # i          && not on right row
                    LOOP

                CASE BETWEEN(m_col,7,15)          && hit on yes
                    rvalue = .T.
                    EXIT

                CASE BETWEEN(m_col,29,36)          && hit on no
                    rvalue = .F.

```

EXIT

ENDCASE

*** test for right or left arrow keys and repaint

CASE KEY = 4 .OR. KEY = 19
yes_on = IIF(yes_on,.F.,.T.)

CASE KEY = 13 && Enter key pressed
rvalue = IIF(yes_on,.T.,.F.)
EXIT

*** test for 'y', 'Y', and Ctrl + Enter

CASE KEY = 89 .OR. KEY = 121 .OR. KEY = 10
rvalue = .T.
EXIT

CASE KEY = 78 .OR. KEY = 110 && 'N' or 'n'
rvalue = .F.
EXIT

ENDCASE

IF yes_on *
SET COLOR OF NORMAL TO (optcolor)
@ i,08 SAY ' Yes ' *
ELSE
SET COLOR OF NORMAL TO (optcolor)
@ i,30 SAY ' No ' *
ENDIF

KEY = INKEY(0,'hm') && wait for key or mouse

RESTORE SCREEN FROM _temp

ENDDO

```

IF KEY = 151          && mouse hit
  RESTORE SCREEN FROM _temp
  SET COLOR OF NORMAL TO (optcolor)

  IF rvalue
    @ i,07 SAY CHR(174) + ' Yes ' + CHR(175)
  ELSE
    @ i,29 SAY '< No >'
  ENDIF

  = INKEY(.3,'H')
ENDIF

SET MEMOWIDTH TO cur_width    && reset memowidth
SET COLOR OF NORMAL TO
RELEASE WINDOW yesno

IF EMPTY(cur_win)
  ACTIVATE SCREEN
ENDIF

POP KEY

RETURN(rvalue)
*: EOF: YESNO.PRG
*: *****
*:
*: Procedure file: C:\FOXPRO\ACLINE\POPERROR.PRG
*:
*:   System: Data Communictaion On Electric Line
*:   Author: Cherdchai J(361-6310) Suvir K(361-6898)
*:   Copyright (c) 1998, ABAC EN 4902 Engineering Project II
*:   Last modified: 09/12/91    0:00
*:
*: Procs & Fncts: POPERROR()
*:
*:   Documented 03/15/98 at 17:22          FoxDoc version 2.10f
*: *****
*: *****

```



```

*!
*!   Function: POPERROR()
*!
*!   Called by: BIGLETT()      (function in BIGLETT.PRG)
*!               : WEXPLODE()  (function in WEXPLODE.PRG)
*!               : YESNO()     (function in YESNO.PRG)
*!
*!   Calls: BEEP()            (function in BEEP.PRG)
*!
*!*****
FUNCTION poperror
PARAMETERS err_mess
PRIVATE cur_color, cur_curs, bord_str, err_mess, say_mess
PRIVATE num_lines, start_line, cur_width, i, rvalue
PRIVATE cur_win

*****
* poperror(<expC>)
* Version # 2.0 FP      Date: 07-20-91
* Programmed by: Malcolm C. Rubel
*
* Copyright (c) 1991
* Performance Dynamics Associates
* All Rights Reserved
*
* Note: Procedure pops up an error in lower right corner
* of screen and waits for a keypress to go back to screen.
* Modified 7-20-91 to include PUSH/POP key.
*****

```

PUSH KEY CLEAR
= beep(1)

```

cur_win = WOUTPUT()
cur_width = SET('memowidth')  && save the old setting
SET MEMOWIDTH TO 48

```

```

num_lines = MEMLINES(err_mess)  && how long is message?

```

```

start_line = 20 - num_lines    && starting row for box

DEFINE WINDOW poperr FROM start_line,14 TO 23,65 DOUBLE ;
    SHADOW COLOR SCHEME 19

ACTIVATE WINDOW poperr

*** paint the message on the screen line by line

IF num_lines = 1
    @ 0,01 SAY PADC(err_mess,48)
    i = 1
ELSE

    FOR i = 0 TO num_lines-1
        say_mess = MLINE(err_mess,i+1)
        @ i,01 SAY LTRIM(say_mess)    && say message line
    ENDFOR

ENDIF

*** draw a line across the bottom of the message and
*** paint "press any key..."

@ i,00 SAY REPLICATE(CHR(196),50)    && draw line

@ i+1,01 SAY 'Press any key to continue....'

rvalue = INKEY(0,'hm')    && hide the cursor

IF WEXIST('poperr')
    RELEASE WINDOW poperr
ENDIF

IF EMPTY(cur_win)
    ACTIVATE SCREEN
ENDIF

SET MEMOWIDTH TO cur_width

```

POP KEY

RETURN(rvalue)

*: EOF: POPERROR.PRG

*.*****

*:

*: Procedure file: C:\FOXPRO\ACLINE\BEEP.PRG

*:

*: System: Data Communicaiton On Electric Line

*: Author: Cherdchai J(361-6310) Suvir K(361-6898)

*: Copyright (c) 1998, ABAC EN 4902 Engineering Project II

*: Last modified: 09/12/91 0:00

*:

*: Procs & Fncts: BEEP()

*:

*: Documented 03/15/98 at 17:22 FoxDoc version 2.10f

*.*****

*!*****

*!

*! Function: BEEP()

*!

*! Called by: POPERROR() (function in POPERROR.PRG)

*!

*!*****

FUNCTION beep

PARAMETERS song

PRIVATE song, i

* beep(<expN>)

* Version # 1.0 FP Date: 10-26-89

* Programmed by: Malcolm C. Rubel

*

* Copyright (c) 1988

* Performance Dynamics Associates

* All Rights Reserved

*

* Note: Plays the songs from the Xbase Hit Parade.

*

```

* song 1 = error
*      2 = danger
*      3 = hello
*      4 = death
*      5 = slide up
*      6 = slide down

```

```

IF TYPE('song') # 'N'      && if bizzare thing passed
    song = 0
ENDIF

```

DO CASE

```

CASE song = 1
    SET BELL TO 800,1
    ?? CHR(7)
    = INKEY(.1)
    ?? CHR(7)

```

```

CASE song = 2
    SET BELL TO 523.3,1
    ?? CHR(7)
    = INKEY(.1)
    ?? CHR(7)
    = INKEY(.1)
    ?? CHR(7)
    = INKEY(.1)
    ?? CHR(7)
    = INKEY(.1)

```

```

CASE song = 3
    SET BELL TO 261,3
    ?? CHR(7)
    SET BELL TO 349,4
    ?? CHR(7)
    SET BELL TO 440,1
    ?? CHR(7)
    SET BELL TO 349,1

```

```
?? CHR(7)
SET BELL TO 261,3
?? CHR(7)
SET BELL TO 349,4
?? CHR(7)
SET BELL TO 440,8
?? CHR(7)
SET BELL TO 349,6
?? CHR(7)
```

```
CASE song = 4
SET BELL TO 261,8
?? CHR(7)
SET BELL TO 261,7
?? CHR(7)
SET BELL TO 261,2
?? CHR(7)
SET BELL TO 261,8
?? CHR(7)
SET BELL TO 311,7
?? CHR(7)
SET BELL TO 293,2
?? CHR(7)
SET BELL TO 293,7
?? CHR(7)
SET BELL TO 261,2
?? CHR(7)
SET BELL TO 261,7
?? CHR(7)
SET BELL TO 247,2
?? CHR(7)
SET BELL TO 261,8
?? CHR(7)
```

```
CASE song = 5
FOR i = 400 TO 1800 STEP 100
SET BELL TO i,1
?? CHR(7)
ENDFOR
```



```
CASE song = 6
```

```
  FOR i = 1800 TO 400 STEP -100
```

```
    SET BELL TO i,1
```

```
    ?? CHR(7)
```

```
  ENDFOR
```

```
OTHERWISE
```

```
  SET BELL TO 440,6
```

```
  ?? CHR(7)
```

```
ENDCASE
```

```
RETURN(.T.)
```

```
*: EOF: BEEP.PRG
```

```
*: *****
```

```
*:
```

```
*: Procedure file: C:\FOXPRO\ACLINE\UNTALK.PRG
```

```
*:
```

```
*:   System: Data Communicaiton On Electric Line
```

```
*:   Author: Cherdchai J(361-6310) Suvir K(361-6898)
```

```
*:   Copyright (c) 1998, ABAC EN 4902 Engineering Project II
```

```
*:   Last modified: 09/12/91   0:00
```

```
*:
```

```
*: Procs & Fncts: UNTALK()
```

```
*:
```

```
*:   Documented 03/15/98 at 17:22   FoxDoc version 2.10f
```

```
*: *****
```

```
*! *****
```

```
*!
```

```
*!   Function: UNTALK()
```

```
*!
```

```
*!   Called by: MAIN.PRG
```

```
*!
```

```
*! *****
```

```
FUNCTION untalk
```

```
*****
```

```
*  untalk()
```

```

* Version # 1.0 FP      Date: 01-29-90
* Programmed by: Malcolm C. Rubel
*
* Copyright (c) 1990
* Performance Dynamics Associates
* All Rights Reserved
*
* Note: Function releases the window that was defined by
* POPTALK.
*****

```

```

IF WEXIST('pop_talk')
  RELEASE WINDOW pop_talk
ENDIF

```

```

RETURN("")
*: EOF: UNTALK.PRG

```



AT89C51 Assembly Program

```

*****
;
;          T I M E R . A S M
;      Interfacing ICM7217CPI & AT89C51 Microcontroller
;      Displays Time Remaining In Hours And Minutes
;      Hardware and Software Design By
;      Suvir Kumar 3616898 and 3616310 Cherdchai Jungsatitkul
;      Electronics and Electrical Engineering Project
;      ASSUMPTION UNIVERSITY FACULTY OF ENGINEERING
;
*****

```

```

ORG 0000H                ;Starting Address

TMOD DATA 089H          ;Timer Mode
IE0  BIT 089H            ;Interrupt
TL0  DATA 08AH          ;Timer 0 Low Byte
TH0  DATA 08CH          ;Timer 0 High Byte
TR0  BIT 08CH            ;Timer 0 Run Control
P0   DATA 080H          ;Port 0 Dip Switch Port
P1   DATA 090H          ;Port 1 Control HARRY Port
P2   DATA 0A0H          ;Relay Driver Port
EX0  BIT 0A8H            ;External Interrupt
ET0  BIT 0A9H            ;Enable Timer 0 Interrupt
EA   BIT 0AFH            ;External Interrupt Enable
PSW  DATA 0D0H          ;Program Status Word
ACC  DATA 0E0H          ;Accumulator

SJMP START               ;Jump Straight Into Program Main Code Segment

ORG 0003H                ;Address of Hardware Int
ACALL INT_INT0            ;Call Count Up Interrupt Service (HARDWARE)
RETI                     ;Return From Interrupt

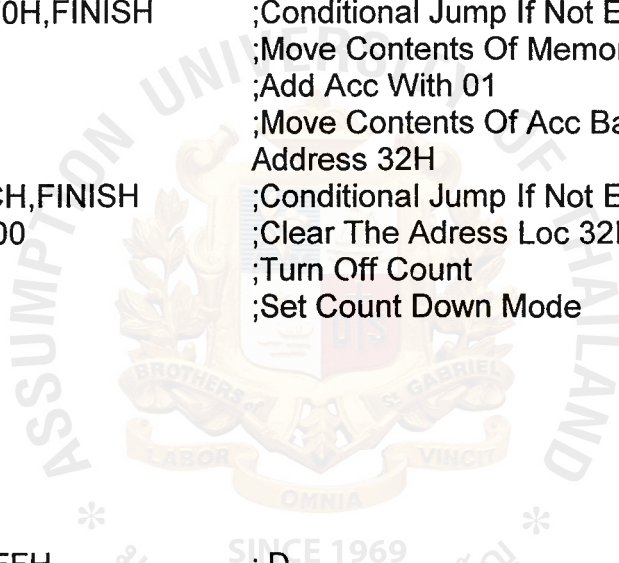
ORG 000BH                ;Address of Timer Int
ACALL INT_TC0            ;Call Count Down With Timing Interrupt
(SOFTWARE)
RETI                     ;Return From Interrupt

ORG 0045H                ;Address Of Start
START:                   ;Start

```

MOV R1,#0FFH	; D
ALAY1:	; E
MOV R2,#0FFH	; L
DJNZ R2,\$; A
DJNZ R1,ALAY1	; Y
MOV R1,#0FFH	; D
ALAY2:	; E
MOV R2,#0FFH	; L
DJNZ R2,\$; A
DJNZ R1,ALAY2	; Y
SETB P1.3	; -----
MOV R1,#0FFH	;
ALAY3:	;
MOV R2,#0FFH	;
DJNZ R2,\$;
DJNZ R1,ALAY3	;
CLR P1.3	; -----
MOV R1,#0FFH	;
ALAY4:	;
MOV R2,#0FFH	;
DJNZ R2,\$;
DJNZ R1,ALAY4	;
SETB P1.3	; And Thou Shalt Remain High
CLR ET0	; Disable Timer Interrupt
CLR TR0	; Stop Timer 0
MOV 30H,#00H	; Clear Value In Address 30H Before Start
MOV 31H,#00H	; Clear Value In Address 31H Before Start
MOV 32H,#00H	; Clear Value In Address 32H Before Start
MOV TMOD,#01H	; Set Timer Mode 1 (16 bit)
MOV TL0,#000H	; Set Countdown
MOV TH0,#090H	; Until 09000H
SETB EA	; Enable All External Interrupts
SETB IE0	; To Detect Falling Edge Of Interrupt
SETB EX0	; Enable External Interrupt E1
SJMP \$; Jump Up And Down Here Forever
INT_INT0:	; Hardware Interrupt Service Procedure
PUSH ACC	; Push Accumulator
PUSH PSW	; Push Program Status Word

MOV R1,#0FFH	;D
ALAY5:	;E
MOV R2,#0FFH	;B
DJNZ R2,\$;O
DJNZ R1,ALAY5	;U
MOV R1,#0FFH	;N
ALAY6:	;C
MOV R2,#0FFH	;E
DJNZ R2,\$	
DJNZ R1,ALAY6	
SETB ET0	;Enable Timer Interrupt
SETB TR0	;Start Timer 0
CLR P1.2	;Turn On Relay
CLR A	;Clear Accumulator
MOV 30H,#00H	;Clear Address 30H
MOV A,P0	;Read Data From Dip Switch Into Acc
MOV 30H,A	;Move Dip Sw Value into 30H
PULSER:	;Procedure To Generate Up Count Pulses
MOV R1,#050H	;D
ALAY7:	;E
MOV R2,#050H	;L
DJNZ R2,\$;A
DJNZ R1,ALAY7	;Y
SETB P1.1	;Set Harry To Count Up Mode
MOV R1,#050H	;D
ALAY8:	;E
MOV R2,#050H	;L
DJNZ R2,\$;A
DJNZ R1,ALAY8	;Y
CLR P1.0	!
MOV R1,#050H	!
ALAY9:	!
MOV R2,#050H	!
DJNZ R2,\$!
DJNZ R1,ALAY9	!-----!
SETB P1.0	!
MOV R1,#050H	!
BLAY1:	!
MOV R2,#050H	!
DJNZ R2,\$!
DJNZ R1,BLAY1	!-----!
CLR P1.0	
DJNZ 30H,PULSER	;And Thou Shalt Remain Low
POP ACC	;Number Of Pulses To Be Sent
POP PSW	;Pop Value Of Accumulator
RET	;Pop Value Of Program Status Word

INT_TC0:	;Software Interrupt Service Procedure
PUSH ACC	;Push Value Of Accumulator On To Stack
PUSH PSW	;Push Value Of Program Status Word On To Stack
MOV A,P2	;Check If 00.00 On Display
JZ ZERO_DISP	
COUNT_DWN:	
MOV TL0,#00H	;Set Timer Count
MOV TH0,#90H	;Down Until 0900EH
MOV A,31H	;Move Contents Of Memory Loc 31H into Acc
ADD A,#08	;Add Acc With 08
MOV 31H,A	;Move Contents Of Acc Back Into Memory Address 31H
CJNE A,#0F0H,FINISH	;Conditional Jump If Not Equal To Finish...
MOV A,32H	;Move Contents Of Memory Loc 32H into Acc
ADD A,#1	;Add Acc With 01
MOV 32H,A	;Move Contents Of Acc Back Into Memory Address 32H
CJNE A,#3CH,FINISH	;Conditional Jump If Not Equal To Finish
MOV 32H,#00	;Clear The Adress Loc 32H
CLR P1.0	;Turn Off Count
CLR P1.1	;Set Count Down Mode
	
MOV R1,#0FFH	; D
BLAY2:	; E
MOV R2,#0FFH	; L
DJNZ R2,\$; A
DJNZ R1,BLAY2	; Y
CLR P1.0	; !
MOV R1,#0FFH	; !
BLAY3:	; !
MOV R2,#0FFH	; !
DJNZ R2,\$; !
DJNZ R1,BLAY3	; !
SETb P1.0	; -----!
MOV R1,#0FFH	; !
BLAY4:	; !
MOV R2,#0FFH	; !

```

DJNZ R2,$
DJNZ R1,BLAY4
CLR P1.0
MOV R1,#0FFH
BLAY5:
MOV R2,#0FFH
DJNZ R2,$
DJNZ R1,BLAY5

```

```

;
;
;-----!
;
;
;
;
;
;
;
;
;
;

```

```

SJMP FINISH

```

```

ZERO_DISP:

```

```

SETB P1.2      ;Turn Off Relay
SETB P1.1      ;Make It Count Up Mode (SAFETY SAKE)
CLR ET0        ;Disable Timer Interrupt
CLR TR0        ;Stop Timer 0

```

```

SETB P1.3
MOV R1,#0FFH
BLAY6:
MOV R2,#0FFH
DJNZ R2,$
DJNZ R1,BLAY6
CLR P1.3
MOV R1,#0FFH
BLAY7:
MOV R2,#0FFH
DJNZ R2,$
DJNZ R1,BLAY7
SETB P1.3
CLR P1.0

```

```

;-----!
;
;
;-----!
;
;
;
;
;
;
;
;
;
;

```

```

FINISH:        ;AND THE FINISH LINE
POP ACC        ;Pop Value Of Accumulator On To Stack
POP PSW        ;Pop Value Of Program Status Word To Stack
RET            ;Return From Interrupt

```

```

END            ;ABDE ABDE THATS ALL FOLKS!!

```

Chapter 5

First Experimental Tests

The first thing we built is the microcontroller based timer. We started by connecting up the ICM7217CIP1 chip on the bread board. The IC would only work if we connected Pins 8, 20 and 21 to ground. We then used Universal PCB to connect up the seven segment displays. We connected the Universal PCB to the breadboard. We supplied 5 volts to the chip and supplied a TTL output from the function generator to the count input pin of the ICM7217CIP1. The ICM7217CIP1 counted up normally. When the chip counted till 59 it would count on till 1 hour. This chip could have a maximum count of 59 hours and 59 minutes. We also discovered that if we supply a voltage to the ICM7217CIP1 it would show some number on the seven segment display even though we have not instructed it to count up. We then realized that we had to supply a reset pulse every time we supplied a voltage to start up the chip.

Another problem with the ICM7217CIP1 chip is that the count input is very sensitive. We proceeded to read the data sheets that were provided from Harris Semiconductors to find out that there is already a schmitt trigger on the input pin. To solve this problem we connected a buffer transistor with a capacitor and resistor to ground. This effectively desensitized the ICM7217CIP1 count input pin.

We proceeded on to write out an algorithm for the microcontroller program. We were lucky that we had a debugger to test our program before programming it into the microcontroller. With a logic probe we tested the outputs of the various ports and programmed it until we were satisfied.

After that we reasonably satisfied with our control program we used the ACP-04 programmer to program the AT89C51 chip. The circuit did not work at all. We then found out that we had to make some modifications in the source code. The starting address of the debugger and the actual microcontroller were different, some modification in the address was needed.

The modification was made and the circuit was showing some response. After solving many problems in the source code, for example using ret

instead of reti and using sjmp instead of acall will work but after a while the program in the microcontroller will hang.

Now to discuss the working of the encoder and decoder chip UM3750. This we connected up this chip on the bread board and it worked on the first shot. We were very pleased with our results.

We then moved on to the AC Line transmitter and receiver part. After building the transmitter on the breadboard we just realized that we could not check it unless we also built the receiver. We were at the point of deciding whether to buy a commercially made TOKO Transformer the part number was given in the datasheet from National Semiconductors. We went to Ban Moh and had no success in finding the TOKO transformer that we were looking for. We became very worried. After discussing this problem with a fellow researcher Zaw Tin Oo we found a simple solution. Zaw told us that even a 455 Khz IF Black IF Transformer that is found in all AM radios works just fine. We then built the transmitter and receiver. We transmitted our signal into the AC line and tried to receive it with another chip. The transmitter was working fine when connected to the oscilloscope. We then connected the transmitter circuit to the AC line. As soon as we connected the circuit to the AC line the circuit refused to transmit. The waveform on the oscilloscope screen disappeared. As soon as we removed the AC line the transmitter began transmitting again. This phenomenon really confused us. We had never seen such a problem before. We tried to change the value of capacitance and resistance. After some time the oscilloscope showed some distorted waveform. We were happy that there was some progress. The receiver was also showing some waveform. The received waveform was small and distorted. After some modifications to the ALC circuit of the LM1893 transmitter chip we got a strong 1v pp signal. The transmitter and receiver stage was then complete. We now have a working timer, a working transmitter, a working receiver, a working encoder and a working decoder. These are all the blocks that we need in our final design. At the time of writing this report all circuits are still in blocks we have one more week to complete our project and hope that we will have a working circuit to present on Saturday the 23rd 1998 to our five project advisor committee.

Equipment Used In Experiment and Fabrication

In the fabrication of our project we used many different pieces of equipment they are as far as we can remember.....

- ◆ IBM PC 486 DX 100 Mhz computer to type out this report and program the microcontroller in assembly
- ◆ ACP-04 Microcontroller Programmer
- ◆ ETS 7000 Digital Trainer Board
- ◆ Iwatsu 20 Mhz Dual Trace Oscilloscope
- ◆ Load Star Function Generator
- ◆ Frequency Counter
- ◆ Resistance Decade Box
- ◆ Capacitance Decade Box
- ◆ PC Parallel Port Connectors
- ◆ Logic Probe
- ◆ Digital Multimeter
- ◆ Soldering Equipment (Gun and Solder Sucker)
- ◆ Electric Drill
- ◆ Cutters, Pliers
- ◆ PCB Holder
- ◆ File
- ◆ Screwdriver Set

Electronic Components Used

- ◆ Electric Fuse and Fuse Holder
- ◆ Transformer 220, 9-0-9 V, 500 mA
- ◆ 1N4001 Rectifier Diodes
- ◆ Capacitors
- ◆ Resistors (Fixed, Adjustable)
- ◆ Led Small Red
- ◆ 7805, 7809, 7815 IC Regulators
- ◆ Zener Diodes
- ◆ NPN BJT
- ◆ PNP BJT
- ◆ Two contact Magnetic Relay
- ◆ 11.0592 Mhz Quartz Crystal
- ◆ ICM 7217CPI Counter Chip
- ◆ AT89C51 Microcontroller Chip
- ◆ Dip Switch
- ◆ UM3750 Encoder / Decoder Chip
- ◆ IF Black 455 KHz Coupling Transformer
- ◆ LM 1893 Carrier Current Transceiver

Chapter 6

Conclusion

The project report is now nearly complete and now we are in the conclusion part. This is the first time we feel that we will actually graduate as Engineers. The process of studying here in ABAC is long and requires a lot of patients and the thirst of knowledge. The encouragement of our parents, teachers and friends has brought us this far. It took us a long time to think up a project title. What should we build that will demonstrate to others our knowledge gained here in ABAC. We were also afraid to choose too complicated a project, something that we would not be able to finish. This project taught us a lot of things. This is the first time I am using Microsoft Word, prior to this I was using wordstar. Without Microsoft Word this project would not be as neat as it is, using Microsoft Word also enabled us to import schematic diagrams from other programs such as Visio Technical. We are lucky that we have many experienced professors to advise us . This project made us read a lot of books, mostly Electronic and Computer manuals. The world wide web was also a great source on information. This was the first time we knew that it was possible to transmit RF on to AC lines. This idea was very new to us and we did a lot of research on this topic.. After we read up the theory part, we started to design the circuit. We carefully chose the Electronic components that we were going to use because some of them are not available in Thailand . This is the first time that we put to use our microprocessor knowledge into practice. We have built and thrown away many circuit boards and a lot of money has been spent in the fabrication of this project. We have learned that there is always a better way, always a better design than the one that we are using now. We have to settle for the best design, and at the same time also consider the cost factor. Electronic components that were selected in the design of our process were a result of experimentation and were not anywhere near the component values we calculated in the theory part. PCB design can be very tiresome and frustrating, especially if you are not good at drawing like us. We also tried to use programs such as Protel PCB but experienced too many problems and decided to draw the PCB the traditional way, by hand. Soldering was not a problem for us as we have already gained some experience in the EFE Summer course offered by Dr. Win Tin. Finally we would like to say that we have used the knowledge we gained in Electronics

I, Electronics II, Electronics III, Communication Electronics, Industrial Instrumentation and Control, Digital Circuits, Microprocessor and Microprocessor Interfacing techniques.

Recommendation

We would first of all like to recommend the Faculty to give us more time to research on our project. I am not saying that the time provided is too little, but we have to submit our project immediately after our finals and that seriously degrades the quality of our project. If possible it should we should be able to send our project within the summer period.

The circuit we used in this design is no where near perfect. It still has many faults. There are many better possible designs. We chose a design which we could easily design with the minimum chip count. We chose many dedicated devices in stead of using general purpose ICs such as logical AND and logical OR gates. If the design were good this circuit would only contain the microcontroller and LM1893 IC at the receiving end and at the transmitting end only have the LM1893 chip. The size of this project is also physically big. We used a metal box which we had at home, we did not purchase any special box, that is why the project is rather large..

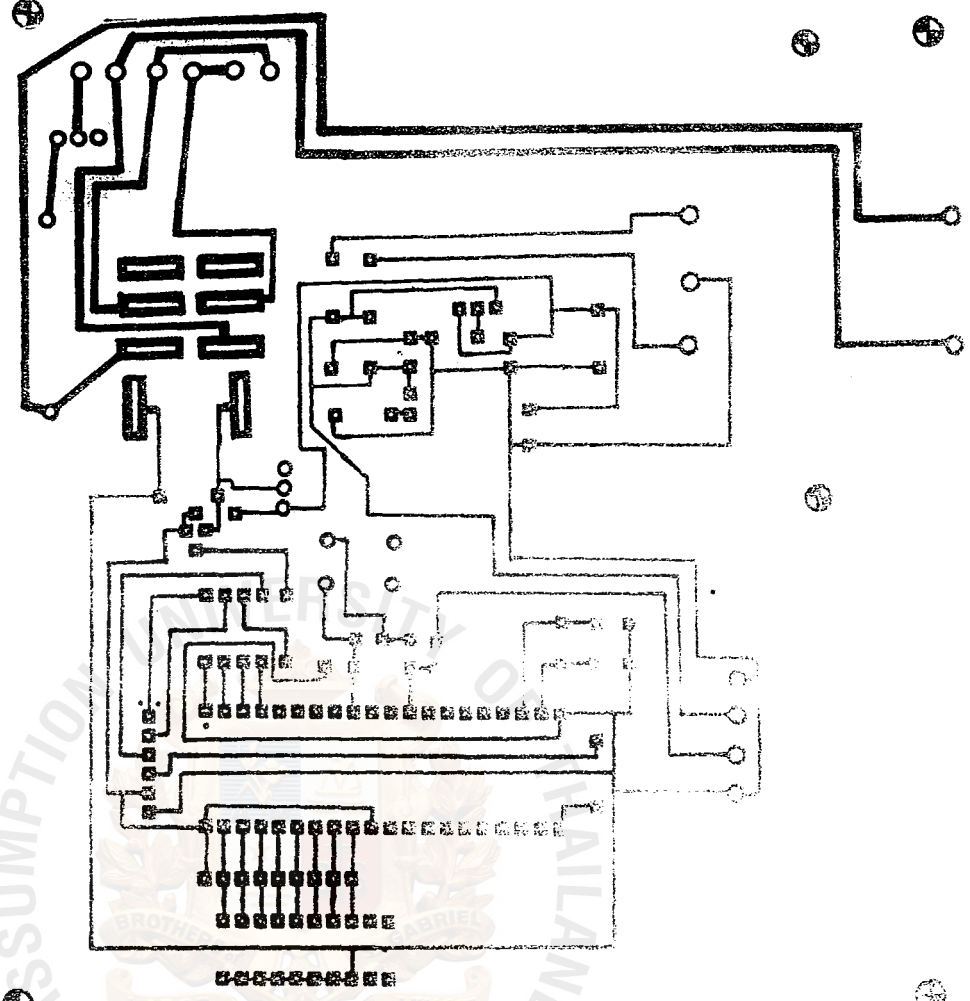


Cherdchai Jungsatitkul
u3616310@home.au.ac.th

I was born on March 2, 1975 at Houcheuw Hospital in Bangkok. I attended many different elementary and high schools. First, I studied in Rungruang School. After that I studied Prathom 1 to 4 at Attawit School and changed school again in Prathom 5 and 6 to Wat Bangnanai School. I got my high school education from Assumption Samrong College and Saint Gabriel College. I did not graduate from Saint Gabriel college because I passed the M.6 equivalent exam first. When I joined ABAC Engineering Faculty, I did not know what major I should choose between Electrical and Electronics. Two years of experience, tells me I should choose the Electrical Major. I like the subject Power System, anything that is physically big. I do not like small circuit that is full of ICs and electronic devices. My favourite hobbies are learning about machines, motor structures and power system transmission from my friend and my father. If I have free time, I take up the same activities such as playing computer games, watching movies at theatre, eating and playing sports. My favourite sport is badminton. After 5 years studying at ABAC, I have received a lot of necessary things such as knowledge and social of ABAC student. I learned a lot from this project and my partner. I really want to thank to my partner who helped me with everything in these 5 years that we studied together.

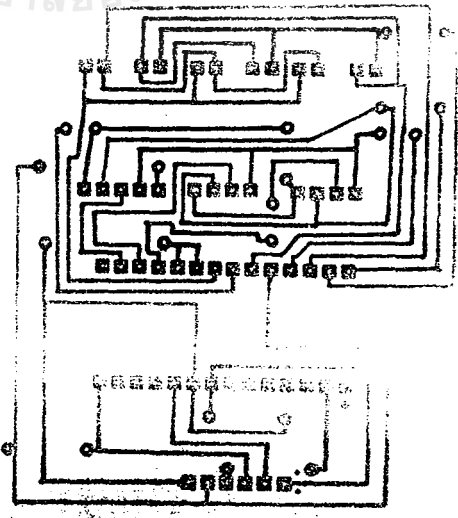
พ. ๐๖๐๐๐๐๐๐๐๐

๐๘๒๕ E 6 1111



+

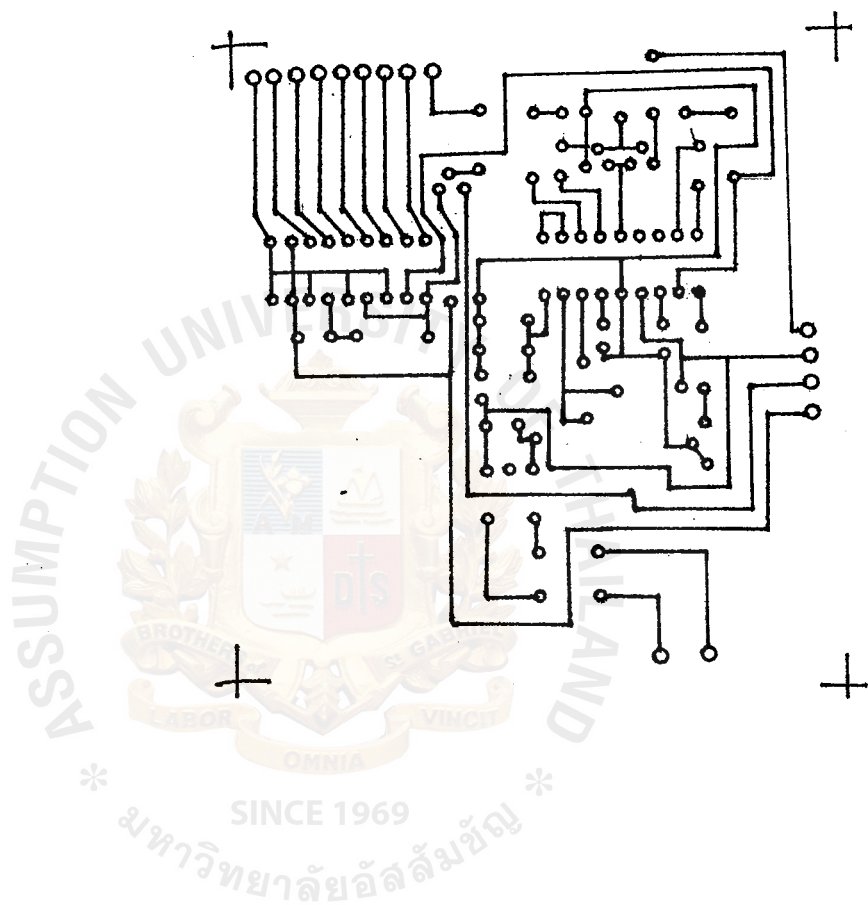
SINCE 1969
มหาวิทยาลัยอัสสัมชัญ



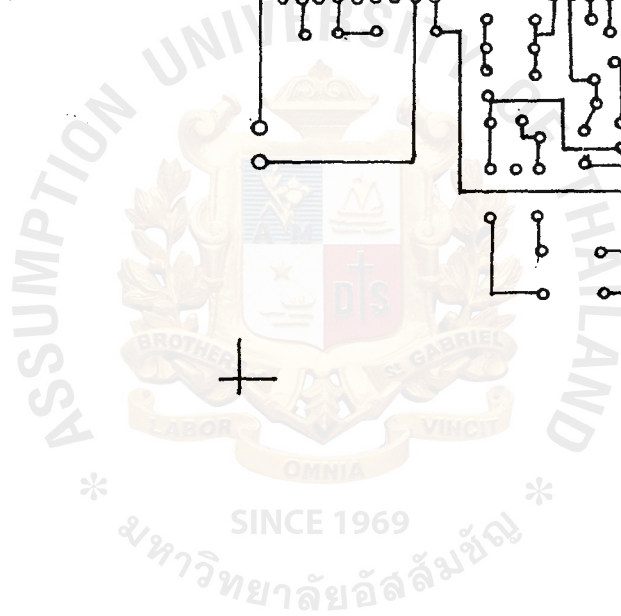
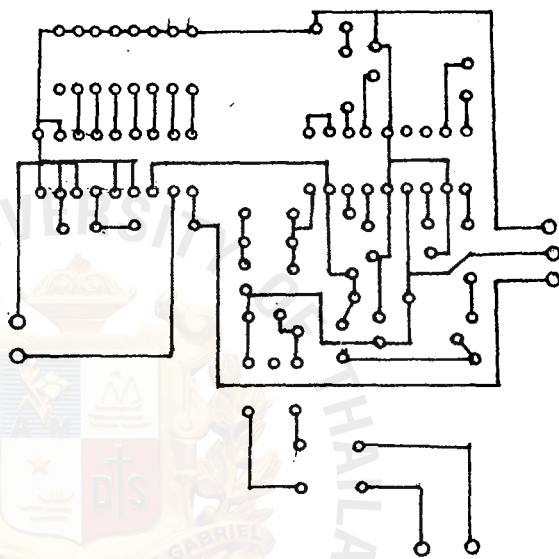
๐๘๒๕

พ. ๐๖๐๐๐๐๐๐๐๐
พ. ๐๖๐๐๐๐๐๐๐๐

E 6 1111



TX

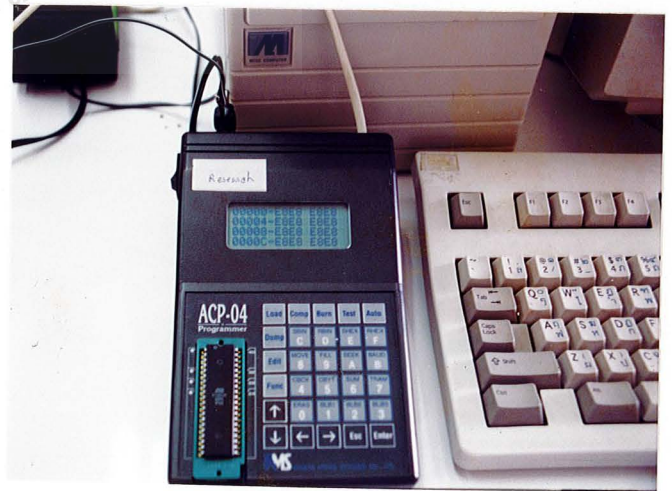
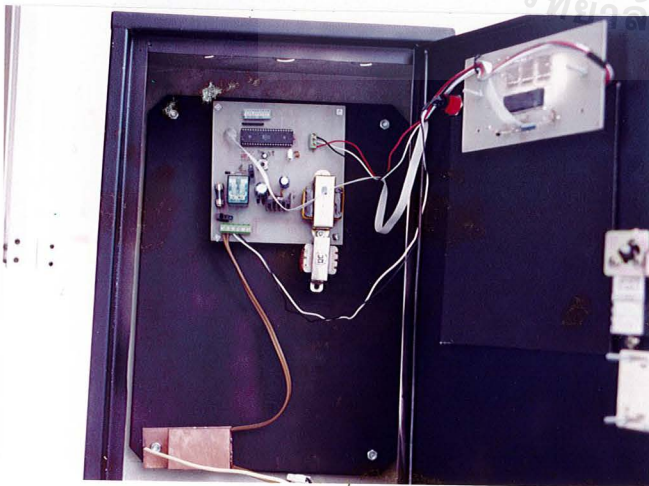
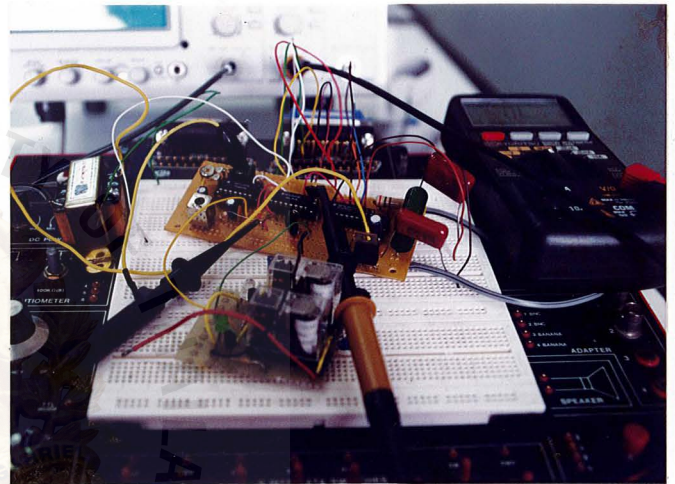
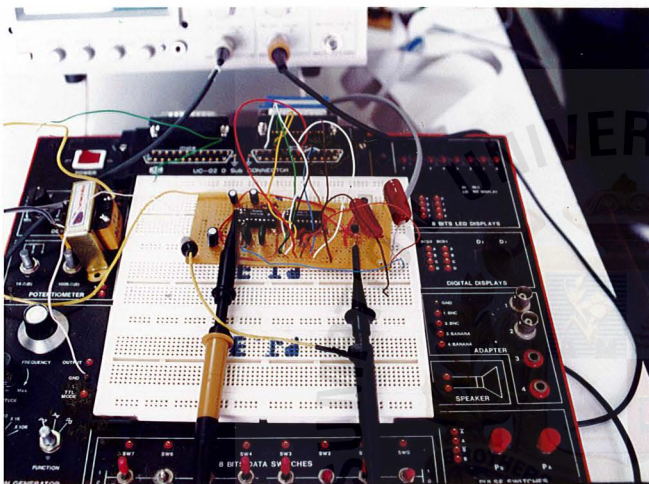


2X.

Project Photographs

In Order From Top To Bottom

1. Transmitter Unit
2. Receiver Unit
3. Microcontroller Based Timer
4. ACP 04 Microcontroller Programmer



Appendix

Data Sheet UM 3750 Encoder/Decoder

Source From Maplin Electronics Catalog

A single chip which includes both encoder and decoder for a coded transmission system. When the code present on the decoder match the code transmitted from the encoder pin 17 goes low for 128ms. If a further match is received in the 128ms period pin 17 stays low for another 128ms and so on. A total of 4096 different codes are possible making the device suitable in alarm control systems, security systems, garage door openers, and remote control.

The system is protected against false transmissions because it only switches after receiving four valid codes and each code must be received within 64ms of the previous one. This system can be used with rf, ultrasonic or infra-red modulators and demodulators. A Min Res 100k and 180pf are required with each chip.

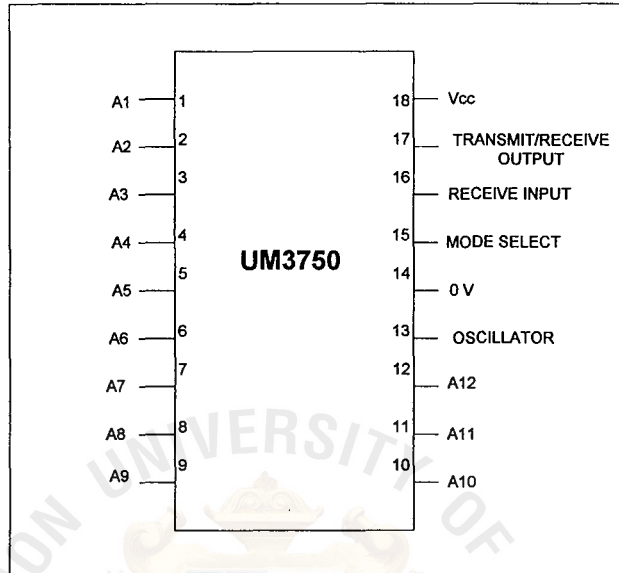
Specification

Supply Voltage : 3V to 11V

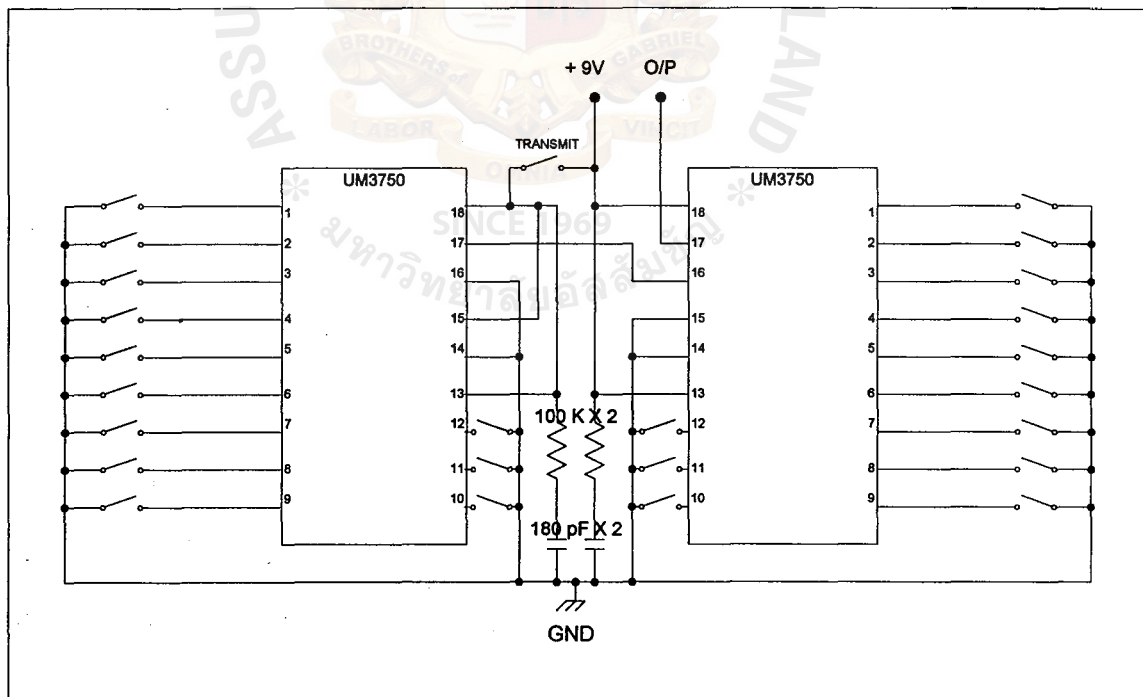
Receive Output : Active low, can sink 2mA

Clock Frequency : 100Khz with components shown $f=2/RC$

Pinouts and Test Circuit



Test Circuit



LM1893/LM2893 Carrier-Current Transceiver

Carrier-current systems use the power mains to transfer information between remote locations. This bipolar carrier-current chip performs as a power line interface for half-duplex (bi-directional) communication of serial bit streams of virtually any coding. In transmission, a sinusoidal carrier is FSK modulated and impressed on most any power line via a rugged on-chip driver. In reception, a PLL-based demodulator and impulse noise filter combine to give maximum range. A complete system may consist of the LM1893, a COPSTM controller, and discrete components.

- Noise resistant FSK modulation
- User-selected impulse noise filtering
- Up to 4.8 kBaud data transmission rate
- Strings of 0's or 1's in data allowed
- Sinusoidal line drive for low RFI

- Output power easily boosted 10-fold
- 50 to 300 kHz carrier frequency choice
- TTL and MOS compatible digital levels
- Regulated voltage to power logic
- Drives all conventional power lines

- Energy management systems
- Home convenience control
- Inter-office communication
- Appliance control
- Fire alarm systems
- Security systems
- Telemetry
- Computer terminal interface

FIGURE 1. Block diagram of carrier—current chip with a complement of discrete components making a complete $F_0 = 125$ kHz, $f_{DATA} = 360$ Baud transceiver. Use caution with this circuit—dangerous line voltage is present.

BI-LINETM and COPSTM are trademarks of National Semiconductor Corp.
†Carrier-Current Transceivers are also called Power Line Carrier (PLC) transceivers.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply voltage	30 V
Voltage on pin 12	55 V
Voltage on pin 10 (Note 1)	41 V
Voltage on pins 5 and 17	40 V
5.6 V DC zener current	100 mA
Junction temperature: transmit mode	150°C
receive mode	125°C
Electro-Static Discharge (120 pF, 1500Ω)	1KV

Maximum continuous dissipation, $T_A = 25^\circ\text{C}$, plastic DIP N (Note 2): transmit mode 1.66 W
receive mode 1.33 W

Operating ambient temp. range	-40 to 85°C
Storage temperature range	-65 to 150°C
Lead temp., soldering, 7 seconds	260°C

Note: Absolute maximum ratings indicate limits beyond which damage to the device may occur. Electrical specifications are not ensured when operating the device above guaranteed limits but below absolute maximum limits, but there will be no device degradation.

General Electrical Characteristics

(Note 3). The test conditions are: $V^+ = 18\text{V}$ and $F_0 = 125\text{ kHz}$, unless otherwise noted.

#	Parameter	Conditions	Typical	Test Limit (Note 4)	Design Limit (Note 5)	Limit Units
1	5.6 V Zener voltage, V_Z	Pin 11, $I_Z = 2\text{ mA}$	5.6	5.2 5.9		V min. V max.
2	5.6 V Zener resistance, R_Z	Pin 11, $R_Z = (V_Z @ 10\text{ mA} - V_Z @ 1\text{ mA}) / (10\text{ mA} - 1\text{ mA})$	5			Ω
3	Carrier I/O peak survivable transient voltage, V_{OT}	Pin 10, discharge 1 μF cap. charged to V_{OT} thru $< 1\Omega$	80	60		V max.
4	Carrier I/O clamp voltage, V_{OC}	Pin 10, $I_{OC} = 10\text{ mA}$, RX mode 2N2222 diode pin 8 to 9	44	41 50		V min. V max.
5	Carrier I/O clamp resistance, R_{I0}	Pin 10, $I_{OC} = 10\text{ mA}$	20			Ω
6	TX/RX low input voltage, V_{IL}	Pin 5	1.8	0.8		V max.
7	TX/RX high input voltage, V_{IH}	Pin 5 (Note 9)	2.2	2.8		V min.
8	TX/RX low input current, I_{IL}	Pin 5 at 0.8 V	-2	-20 1		μA min. μA max.
9	TX/RX high input current, I_{IH}	Pin 5 at 40 V	10 ⁻⁴	-1 10	0	μA min. μA max.
10	RX - TX switch-over time, T_{RT}	Time to develop 63% of full current drive thru pin 10	10			μs
11	TX - RX switch-over time, T_{TR}	1 bit time, $T_B = 1/(2F_{DATA})$. Time T_{TR} is user controlled with C_M , see Apps. Info.	2			bit
12	ICO initial accuracy of F_0	TX mode, $R_0 = 6.65\text{ k}\Omega$, $C_0 = 560\text{ pF}$ $F_0 = (F_1 + F_2)/2$	125	113 137		kHz min. kHz max.
13	ICO temperature coefficient of F_0	TX or RX mode, $(F_{OMAX} - F_{OMIN}) / (T_{JMAX} - T_{JMIN})$	-100			PPM/°C
14	Temperature drift of F_0	TX or RX mode, $-40 \leq T_J \leq T_{JMAX}$	± 2.0		± 5.0	% max.

Transmitter Electrical Characteristics (Note 3). The test conditions are: $V^+ = 18\text{ V}$ and $F_0 = 125\text{ kHz}$ unless otherwise noted. The transmit center frequency is F_0 , FSK low is F_1 , and FSK high is F_2 .

#	Parameter	Conditions	Typical	Test Limit (Note 4)	Design Limit (Note 5)	Limit Units
15	Supply voltage, V^+ , range	Meets test 17 spec. at $T_J = 25^\circ\text{C}$ and: $ (F_1[14\text{V}] - F_1[18\text{V}]) / F_1[18\text{V}] < 0.01$ $ (F_1[24\text{V}] - F_1[18\text{V}]) / F_1[18\text{V}] < 0.01$	13 40	14 24	15 23	V min. V max.
16	Total supply current, I_{QT}	Pin 15. Pin 12 high. I_{QT} is I_Q through pin 15 and the average current I_{ODC} of the Carrier I/O through pin 10	52	79		mA max.
17	Carrier I/O output current, I_O	100Ω load on pin 10	70	45		mApp min.
18	Carrier I/O lower swing limit, V_{ALC}	Pin 10. Set internally be ALC. 2N2222 diode pin 8 to 9	4.7	4.0 5.7		V min. V max.
19	THD of I_O (Note 6)	Q of 10 tank driving 10Ω line 100Ω load, no tank	0.6 5.5		5.0 9	% max. % max.
20	FSK deviation, $F_2 - F_1$	$(F_2 - F_1) / ((F_2 + F_1)/2)$	4.4	3.7 5.2		% min. % max.
21	Data In. low input voltage, V_{IL}	Pin 17	1.7	0.8		V max.
22	Data In. high input voltage, V_{IH}	Pin 17 (Note 9)	2.1	2.8		V min.
23	Data In. low input current, I_{IL}	Pin 17 at 0.8 V	-1	-10 1		μA min. μA max.
24	Data In. high input current, I_{IH}	Pin 17 at 40 V	10 ⁻⁴	-1 10	0	μA min. μA max.

Receiver Electrical Characteristics (Note 3). The test conditions are: $V^+ = 18\text{ V}$, $F_O = 125\text{ kHz}$, $\pm 2.2\%$ deviation FSK, $F_{\text{DATA}} = 2.4\text{ kHz}$, $V_{\text{IN}} = 100\text{ mVpp}$, in the receive mode, unless otherwise noted.

#	Parameter	Conditions	Typical	Test Limit (Note 4)	Design Limit (Note 5)	Limit Units
25	Supply voltage, V^+ , range	Functional receiver (Note 7)	12 37	13 30	13.5 28	V min. V max.
26	Supply current, I_{QT}	I_{QT} is pin 15 (V^+) plus pin 10 (Carrier I/O) current. $2.4\text{ k}\Omega$ Pin 13 to GND.	11	5 14		mA min. mA max.
27	Carrier I/O input resistance, $R_{\text{I}0}$	Pin 10	19.5	14 30		k Ω min. k Ω max.
28	Max. data rate, F_{MD}	Functional receiver (Note 7), $C_F = 100\text{ pF}$, $R_F = 0\Omega$, no tank, $2.4\text{ kHz} = 4.8\text{ kBaud}$	10	4.8	2.4	kBaud
29	PLL capture range, F_C	$C_F = 100\text{ pF}$, $R_F = 0\Omega$	± 40	± 15	± 10	% min.
30	PLL lock range, F_L	$C_F = 100\text{ pF}$, $R_F = 0\Omega$	± 45	± 15		% min.
31	Receiver input sensitivity, S_{IN}	For a functional receiver (Note 8) Referred to chip side (pin 10) of the line-coupling XFMR: $F_O = 50\text{ kHz}$ $F_O = 300\text{ kHz}$ Referred to line side of XFMR: (assuming a 7.07:1 XFMR) $F_O = 50\text{ kHz}$ $F_O = 300\text{ kHz}$	1.8 2.0 1.4 0.26 0.29 0.20	10	12	mVRMS mVRMS mVRMS mVRMS mVRMS mVRMS
32	Tolerable input dc voltage offset range, V_{INDC}	Pin 10 lower than pin 15 by V_{INDC}	2	0.1		V max.
33	Data Out. breakdown voltage	Pin 12, leakage $I \leq 20\text{ }\mu\text{A}$	70	55		V min.
34	Data Out. low output, V_{OL}	Pin 12, sat. voltage at $I_{\text{OL}} = 2\text{ mA}$	0.15	0.4		V max.
35	Impulse noise filter current, I_I	Pin 13 charge and discharge current	± 55	± 45 ± 85		μA min. μA max.
36	Offset hold cap. bias voltage, V_{CM}	Pin 6	2.0	1.3 3.5		V min. V max.
37	Offset hold capacitor max. drive current, I_{MCM}	Pin 6, $V(\text{pin } 3) - V(\text{pin } 4) = \pm 250\text{ mV}$	± 55	± 25 ± 80		μA min. μA max.
38	Offset hold bias current, I_{OHB}	Pin 6, TX mode. Bias pin 6 as it self-biased during test 31.	-0.5	-20	-40 40	nA min. nA max.
39	Phase comparator current, I_{PC}	Bias pins 3 and 4 at 8.5 V $I_{\text{PC}} = I(\text{pin } 3) + I(\text{pin } 4)$, TX mode	100	50 200		μA min. μA max.
40	Phase detector output resistance, R_{PD}	Pins 3 and 4. $R_{\text{PD}} = (V @ 100\mu\text{A} - V @ 50\mu\text{A}) / (50\mu\text{A})$	10	6 18		k Ω min. k Ω max.
41	Phase detector demodulated output voltage, V_{PD}	Pin 3 to 4, measured after filtering out the $2F_O$ component	100	60 180		mVpp min. mVpp max.
42	Fast offset cancel voltage "window" -to- V_{PD} ratio, V_W/V_{PD}	$V_{\text{PIN}3} - V_{\text{PIN}4} = \pm V_{\text{WINDOW}} + \text{DC offset}$ Drive for $\pm 1\text{ }\mu\text{A}$ pin 6 current	0.95	0.70 1.20		V/V min. V/V max.
43	Power supply rejection, PSRR	$C_L = 0.1\text{ }\mu\text{F}$. PSRR = CMRR. 120 Hz	80			dB min.

Note 1: More accurately, the maximum voltage allowed on pin 10 is V_{OC} , and V_{OC} ranges from 41 to 50V. Also, transients may reach above 60V; see the transient peak voltage characteristic curve.

Note 2: The maximum power dissipation rating should be derated for device operation above 25°C to insure that the junction temperature remains below the maximum rating. Use a θ_{JA} of 75°C/W for the N package using a socket in still air (which is the worst case). Consult the Application Information section for more detail.

Note 3: The boldface values apply over the full junction temperature range for the specified supply voltage range. All other numbers apply at $T_A = T_J = 25^\circ\text{C}$. Pin numbers refer to LM1893. LM2893 tested by shorting Carrier In to Carrier Out and testing it as an LM1893.

Note 4: Guaranteed and 100% production tested.

Note 5: Guaranteed (but not 100% production tested) over the temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

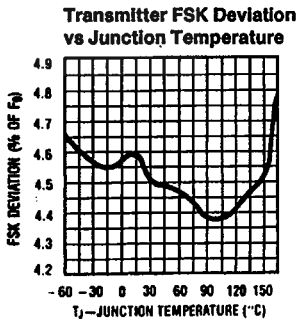
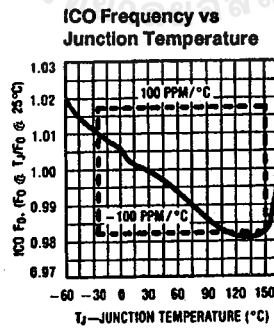
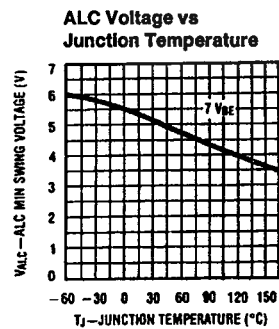
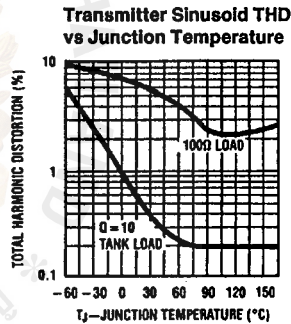
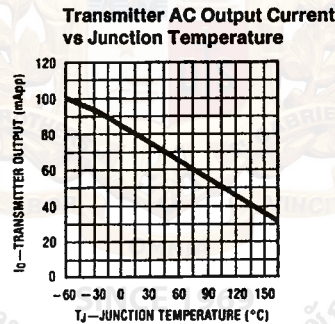
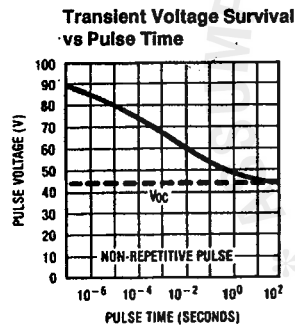
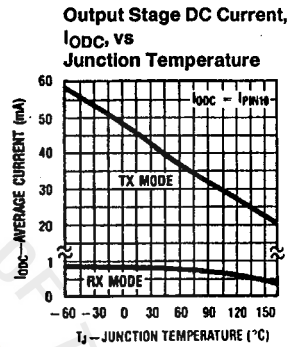
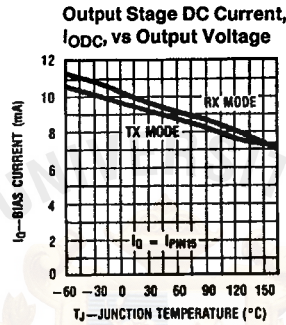
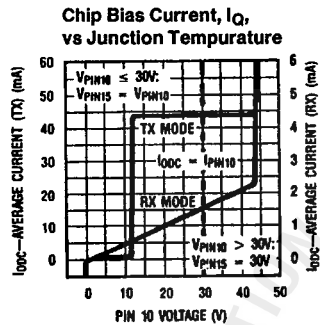
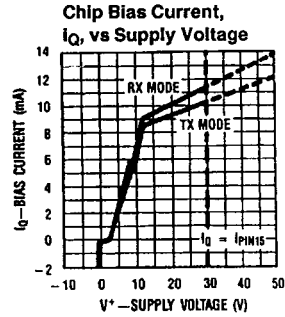
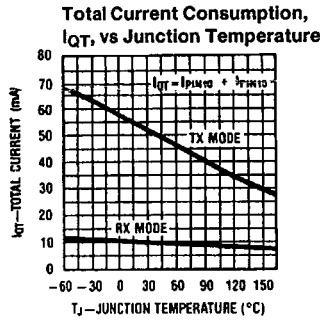
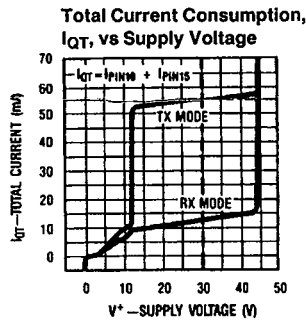
Note 6: Total harmonic distortion is measured using $\text{THD} = [I_{\text{RMS}} (\text{all components at or above } 2F_O)] / [I_{\text{RMS}} (\text{fundamental})]$.

Note 7: Receiver function is defined as the error-free passage of 1 cycle of 50% duty-cycle 2.4 kHz square-wave data (2 sequential $208\text{ }\mu\text{S}$ bits), with the first bit being a "1." All of the data transitions (edges) must fall within $\pm 10\%$ ($\pm 20.8\text{ }\mu\text{s}$) of their noise-free positions. RX time delay is minimized by using no impulse noise filter cap. C_I for this test.

Note 8: During the sensitivity check, note 7 requirements are followed with these exceptions: (1) data rate $F_{\text{DATA}} = 1.2\text{ kHz}$, (2) all of the data transitions must fall within $\pm 20\%$ ($\pm 41.6\text{ }\mu\text{s}$) of their noise-free positions, and (3), a time-domain filter capacitor (C_I) is used. The time delay of C_I is $1/2$ bit, or $208\text{ }\mu\text{s}$. (C_I is approximately 6200 pF).

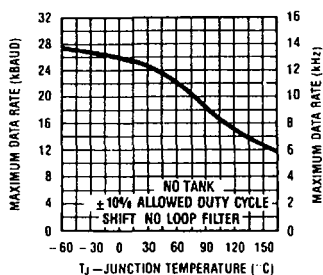
Note 9: For TTL compatibility use a pull-up resistor to increase min. V_{OH} to above 2.8 V .

Typical Performance Characteristics ($V^+ = 18V$, $F_O = 125\text{ kHz}$, circuit of Figure 1, pin numbers for LM1893)

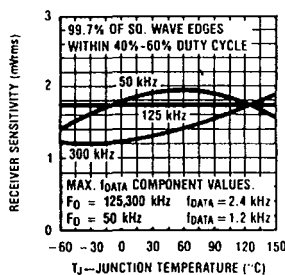


Typical Performance Characteristics (Continued)

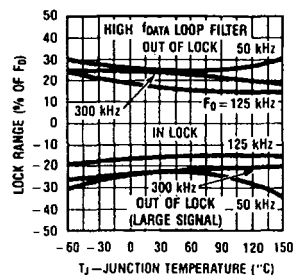
Maximum Data Rate vs
Junction Temperature



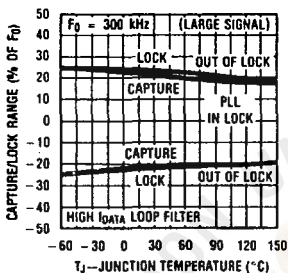
Receiver Sensitivity vs
Junction Temperature



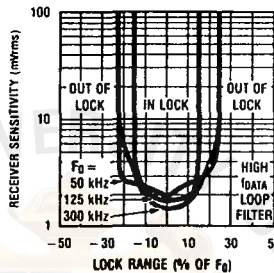
PLL Lock Range vs
Junction Temperature and F_0



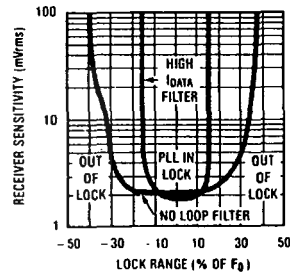
PLL Capture & Lock Range vs
Junction Temperature



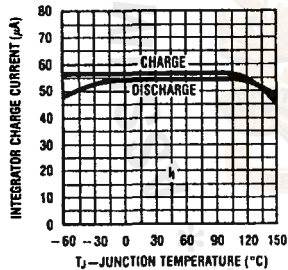
Receiver Sensitivity vs
PLL Lock Range and F_0



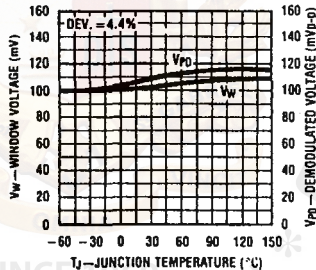
Receiver Sensitivity vs
PLL Lock Range and Loop Filter



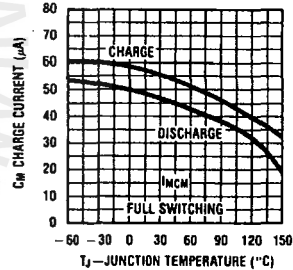
Impulse Noise Filter
Current vs Junction
Temperature



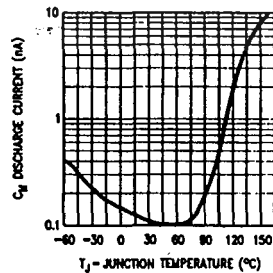
Phase Detector Output
Voltage vs Junction
Temperature



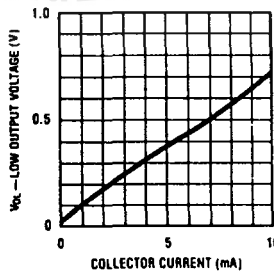
Offset Hold Cap. Charge
Currents vs Junction
Temperature



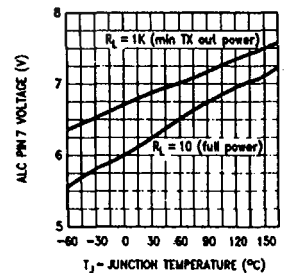
Offset Hold Cap. Bias Current vs
Junction Temperature



Data Out. Low Voltage vs
Pull Down Current



Pin 7 Bias Voltage vs
Junction Temperature



TL/H/6750-39

Application Information*

THE DATA PATH

The BI-LINET[™] chip serves as a power line interface in the carrier-current transceiver (CCT) system of Figure 3. Figure 4 shows the interface circuit now discussed. The controller may select either the transmit (TX) or receive (RX) mode. Serial data from the controller is used to generate a FSK-modulated 50 to 300 kHz carrier on the line in the TX mode. In the RX mode line signal passes through the coupling transformer into the PLL-based receiver. The recreated serial bit stream drives the controller.

With the IC in the TX mode (pin 5 a logic high), baseband data to 5 kHz drive the modulator's Data In pin to generate a switched 0.9781/1.0221 control current to drive the low TC, triangle-wave, current-controlled oscillator to $\pm 2.2\%$ deviation. The tri-wave passes through a differential attenuator and sine shaper which deliver a current sinusoid through an automatic level control (ALC) circuit to the gain of 200 current output amplifier. Drive current from the Carrier I/O develops a voltage swing on T_1 's (Figure 4) resonant tank proportional to line impedance, then passes through the step-down transformer and coupling capacitor C_C onto the line. Progressively smaller line impedances cause reduced signal swing, but never clipping—thus avoiding potential radio frequency interference. When large line impedances threaten to allow excessive output swing on pin 10, the ALC shunts current away from the output amplifier, holding the voltage swing constant and within the amp's compliance limit. The amplifier is stable with a load of any magnitude or phase angle.

In the RX mode (pin 5 a logic low), the TX sections on the chip are disabled. Carrier signal, broad-band noise, transient spikes, and power line component impinge of the receiver's input highpass filter, made up of C_C and T_1 , and the tank bandpass filter. In-band carrier signal, band-limited noise, heavily attenuated line frequency component, and attenuated transient energy pass through to produce voltage swing on the tank, swinging about the positive supply to drive the Carrier I/O receiver input. The balanced Norton-input limiter amplifier removes DC offsets, attenuates line frequency, performs as a bandpass filter, and limits the signal to drive the PLL phase detector differentially. The differential demodulated output signal from the phase detector, containing AC and DC data signal, noise, system DC offsets, and a large twice-the-carrier-frequency component, passes through a 3-stage RC lowpass filter to drive the offset cancel circuit differentially. The offset cancelling circuit works by insuring that the (fixed) ± 50 mV signal delivered to the data squaring ("slicing") comparator is centered around the 0 mV comparator switch point. Whenever the comparator signal plus DC offset and noise moves outside the carefully matched ± 50 mV voltage "window" of the offset cancel circuit, it adjusts its DC correction voltage in series with the differential signal to force the signal back into the window. While the signal is within the ± 50 mV window, the DC offset is stored on capacitor C_M . By grace of the highly non-linear offset hold capacitor charging during offset cancelling, the DC cancellation is done much more quickly than with an AC coupling capacitor normally used in place of the offset cancel circuit. Since impulse noise spikes normally ring the signal symmetrically around 0 V, the fully bilateral offset cancel topology affords excellent noise rejection. The switched current output of the comparator drives the impulse noise filter integrator capacitor that rejects all data pulses of less than the integrator charge time. Noise appears as duty-cycle jitter at the open collector serial data output.

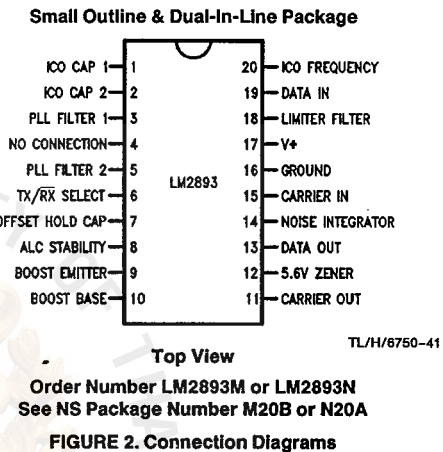
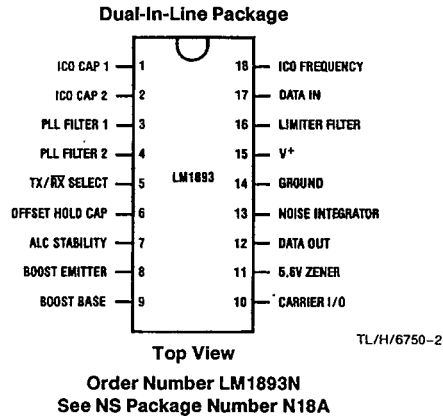


FIGURE 2. Connection Diagrams

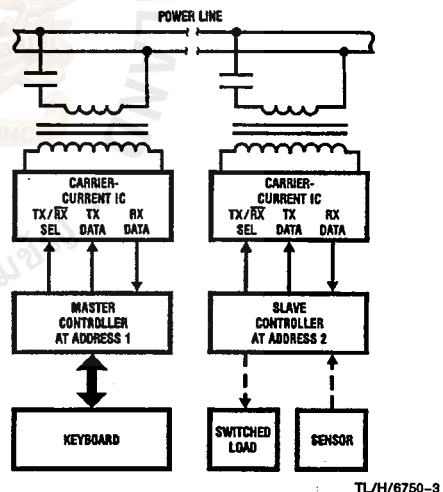


FIGURE 3. The block diagram of a carrier-current system using the Bi-Line chip to interface digital controllers via the power line

*Unless otherwise noted, all pin references refer to LM1893, but hold true for equivalent LM2893 pin.

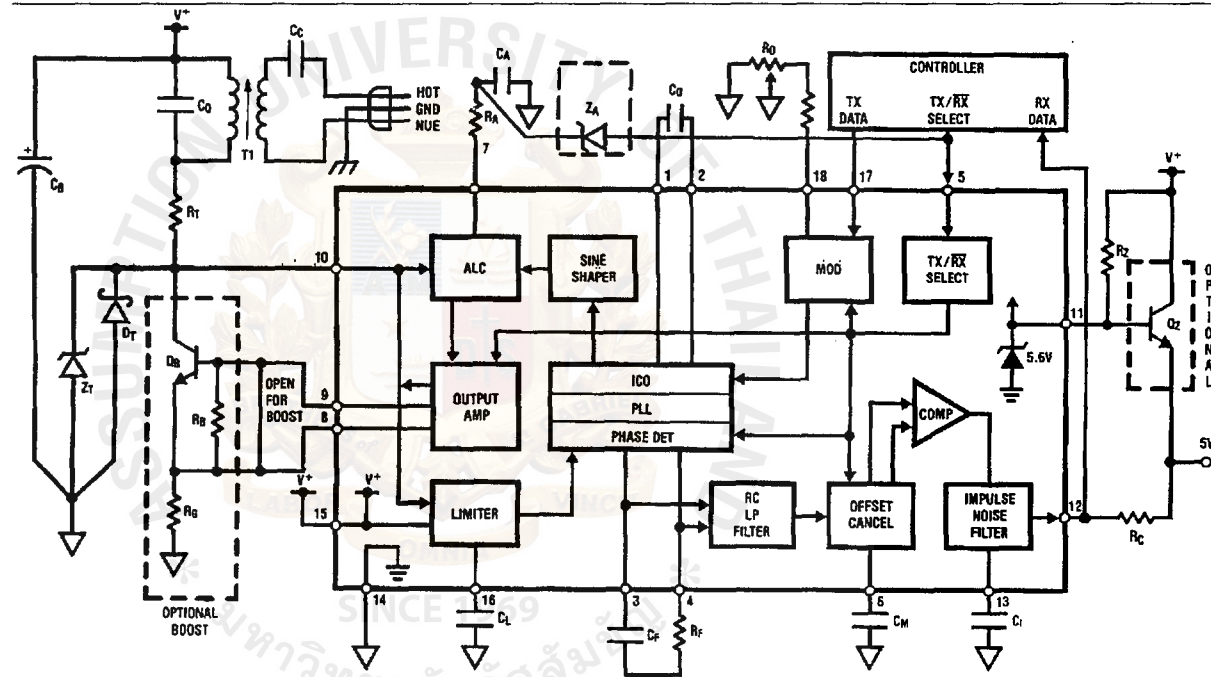


FIGURE 4. Block diagram of a CCT system with the boost and 5V supply options shown in dashed boxes

TL/H/6750-4

Application Information (Continued)

#	Recommended Value	Purpose	Effect of making the component value:		Notes
			Smaller	Larger	
C _O R _O	560 pF 6.2 kΩ	Together, C _O and R _O set ICO F _O .	Increases F _O Increases F _O <5.6 k not recommended.	Decreases F _O Decreases F _O >7.6 k not recommended.	±5% NPO ceramic. Use low TC 2 k pot and 5.6 k fixed R. Poor F _O TC with <5.6 k R _O .
C _F R _F	0.047 μF 3.3 kΩ	PLL loop filter pole PLL loop filter zero	Less noise immune, higher f _{DATA} , more PLL stability. PLL less stable, allows less C _F . Less ringing.	More noise immune, lower f _{DATA} , less PLL stability. PLL more stable, allows more C _F . More ringing.	Depending on R _F value and F _O , PLL unstable with large C _F . See Apps. Info. C _F and R _F values not critical.
C _C	0.22 μF	Couples F _O to line, C _C and T ₁ low-pass attenuates 60 Hz.	Low TX line amplitude. Less 60 Hz T ₁ current. Less stored charge.	Drives lower line Z. More 60 Hz T ₁ current. More stored charge.	≥250 V non-polar. Use 2C _C on hot and neutral for max. line isolation, safety.
C _Q T ₁	0.033 μF Use recommended XFMR	Tank matches line Z, bandpass filters, isolates from line, and attenuates transients.	Tank F _O up or increase L of T ₁ for constant F _O . Smaller L: higher F _O or increase C _C ; decreased F _O line pull.	Tank F _O down or decrease L of T ₁ for constant F _O . Larger L: lower F _O or decrease C _C ; increased F _O line pull.	100 V nonpolar, low TC, ±10% High large-signal Q needed. Optimize for low F _O line pull with control of F _O TC and Q.
C _A R _A	0.1 μF 10 kΩ	ALC pole ALC zero	Noise spikes turn ALC off. Less stable ALC.	Slower ALC response. More stable ALC.	R _A optional. ALC stable for C _A ≥ 100 pF.
C _L	0.047 μF	Limiter 50 kHz pole, 60 Hz rejection.	Higher pole F, more 60 Hz reject. F _O attenuation?	Lower pole F, less 60 Hz reject, more noise BW.	Any reasonably low TC cap. 300 pF guarantees stability.
C _M	0.47 μF	Holds RX path V _{OS}	Less noise immune, shorter V _{OS} hold, faster V _{OS} acquisition, shorter preamble.	More noise immune, longer V _{OS} hold, slower V _{OS} acquisition, longer preamble.	Low leakage ±20% cap. Scale with f _{DATA} .
C _I	0.047 μF	Rejects short pulses like impulse noise.	Less impulse reject, less delay, more pulse jitter.	More impulse reject, more delay, less pulse jitter.	C _I charge time 1/2 bit nom. Must be <1 bit worst-case.
R _C	10 kΩ	Open-col. pull-up	Less available sink I.	Less available source I.	R _C ≥ 1.5 kΩ on 5.6 V
R _Z	12 kΩ	5.6 V Zener bias	Larger shunt current, more chip dissipation.	Smaller shunt current, less V ⁺ current draw.	1 < I _Z < 30 mA recommended. (Chip power-up needs 5.6 V)
Z _T	≥44 V BV <60 V peak	Transient clamp	Z _T failure, higher series R-excess peak V, Zener and chip damage, less ruggedness.	Z _T costly, lower series R gives enhanced transient clamp, more ruggedness.	Recommend Zener rated for ≥500 W for 1 ms.
R _T D _T	4.7 Ω ≥44V BV	Transient I limit Over-drive Clamp	Damage Z _T , pull up V ⁺ . Failure on Transient	Excessive TX attenuation. Costly	Carbon comp. recommended. IRF 11DQ05 or 1N5819
R _B Q _B R _G	180 Ω Power NPN 1.1 Ω	Base bleed Boost gain device Current setting R	Faster, lower THD I _O . Excessive T _J and V _{SAT} . More I _O , need higher h _{FE} .	Inadequate turn-off speed. More rugged, but costly. Less I _O , lower min. h _{FE} .	Boost optional. Q _B F(-3 dB) of >200 MHz. R _B > 24 Ohm. I _O = 70[(10 + R _G)/R _G] mApp.
C _B	≥47 μF	Supply bypass	Transients destroy chip.	Less supply spike.	V ⁺ never over abs. max.
Z _A	5.1V	Stop ALC charge in RX mode	Excess ALC current flow	ALC RX charging not inhibited over T _J	Z _A optional - 5.1V ±20% low leakage type

FIGURE 5. A quick explanation of the external component function using the circuit of Figure 4. Values given are for V⁺ = 18 V, F_O = 125 kHz, f_{DATA} = 360 Baud (180 Hz), using a 115 V 60 Hz power line

Component Selection

Assuming the circuit of Figure 4 is used with something other than the nominal 125 kHz carrier frequency, 180 Hz data rate, 18V supply voltage, etcetera, the component values listed in Figure 5 will need changing. This section will help direct the CCT designer in finding the required component values with emphasis placed on look-up tables and charts. It is assumed that the designer has selected values for carrier center frequency, F_O; data rate, f_{DATA}; supply voltage, V⁺; power line voltage, V_L; and power line frequency, F_L. If one or more of those parameters is not defined, one may read the data sheet and make an educated guess.

Maxims to keep in mind, based on CCT electrical perform-

ance considerations only, are: 1) the higher the F_O the better, 2) the lower the maximum data rate the better, and 3) the more time and frequency filtering the better.

Use Figure 5 as a quick reference to the external component function.

THE TRANSMITTER

C_O

Central to chip operation is the low TC of F_O emitter-coupled oscillator. With proper C_O, the F_O of the 2V_{BE} amplitude triangle-wave oscillator output may vary from near DC to above 300 kHz. While C_O may have any value, C_O should

Component Selection (Continued)

be made above 10 pF so that parasitic capacitance is not dominant. Excessive or unbalanced common-mode-to-ground capacitance should be avoided. A low temperature coefficient (TC) of capacitance (<100 PPM/°C), such as a monolithic NPO ceramic multilayer type, preserves low TC of F_O . Figure 6 finds a C_O value given F_O .

R_O

Resistor R_O is used by the IC to generate a V_{BE}/R related current that is multiplied by 2 to produce the 200 μ A ICO control current that sets F_O . The control current TC "bucks" the V_{BE} related tri-wave amplitude across C_O to effect a low TC of F_O . Vary R_O to trim F_O , within limits. Raising F_O more than 20% above its untrimmed value by means of decreasing R_O more than 20% is not recommended. Low R_O , and so high control current, risks ICO saturation and poor TC under worst-case conditions. Raising R_O reduces the demodulated signal amplitude from the phase detector; raising R_O by more than a factor of 2 (1 octave) is not recommended. Since lower TC pots are relatively costly, it is recommended that R_O be made up of a 5.6 k fixed (<100 PPM/°C) resistor with a 2 k Ω (<250 PPM/°C) series pot.

C_A and R_A

Components C_A and R_A control the dynamic characteristics of the transmitter output envelope. Their values are not critical. Use the values given in Figure 5. C_A and R_A are functions of loaded T_1 tank Q, R_O , f_{DATA} , and line impulse noise. Any changes made in C_A and R_A should be made based on empirical measurements of a CCT on the line. Roughly, C_A acts as an ALC pole and R_A an ALC zero.

T_1

At this point, the CCT system designer may choose to use one of the recommended transformers or to design custom T_1 . Consult "The Coupling Transformer" section to help with the design of T_1 if a new or boost-capable transformer is needed. The recommended 125 kHz transformer functions with an I_O of up to 600 mA.

It is recommended that CCT systems use the recommended transformers, described in Figure 7, for T_1 . The 3 transformers are optimized for use in the ranges of 50–100 kHz, 100–200 kHz, and 200–400 kHz with unloaded Q's (Q_U) of about 35, and loaded Q's (Q_L) of about 12. Three secondary taps are supplied with nominal 7.07, 10, and 14.1 turns ratios (N) to drive industrial and residential power line impedances of 3.5, 7, and 14 Ω respectively. All are inexpensive, all have the same pin-outs for easy exchange in a PC board, and all are small - on the order of 10 mm diameter at the base.

C_Q

Tank resonant frequency F_Q must be correct to allow passage of transmitter signal to the line. Use Figure 8 to find C_Q 's value. Trimming F_Q to equal F_O is done with T_1 's trimming slug. The inductance of T_1 has a TC of +150 PPM/°C which may be cancelled by using a -150 PPM/°C cap such as polystyrene. Since circulating current in the tank is $1/4$ ARMS, C_Q should have a low series resistance (a 1 Ω series resistance is too much). Polypropylene caps are excellent, "orange drop" mylars are adequate, while many other mylars are inadequate. A 100V rating is needed for transient protection.

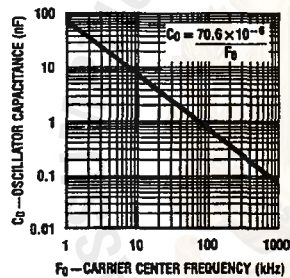


FIGURE 6. Find C_O 's value knowing F_O

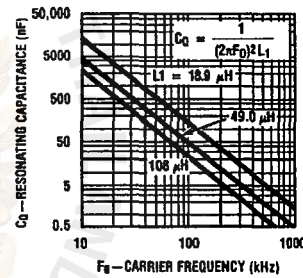


FIGURE 8. Find C_Q 's value given F_Q

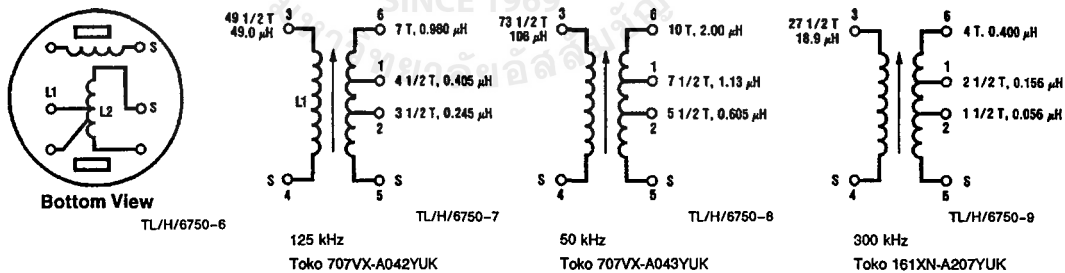


FIGURE 7. The recommended T_1 transformers, available through:
Toko America, 1250 Feehanville Drive, Mount Prospect, IL, 60056, (312) 297-0070

Component Selection (Continued)

C_C

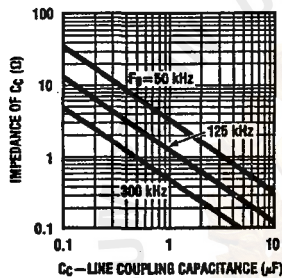
Capacitor C_C 's primary function is to block the power line voltage from T_1 's line-side winding. Also, C_C and T_1 's line-side winding comprise a LC highpass filter. The self-inductance of T_1 is far too low to support a direct line connection. C_C must have a low enough impedance at F_O to allow T_1 to drive transmitted energy onto the line. To drive a 14 Ω power line, the impedance of C_C should be below 14 Ω .

Use Figure 9 to find the reactive impedance of C_C to check that it is less than the line impedance. Then check Figure 10 to see that the power line current is small enough to keep T_1 well out of saturation; the recommended transformers can withstand a 10 Amp-turn magnetizing force (1 Amp through the worst-case 10 turn line-side winding).

Caution is required when choosing C_C to avoid series resonance of the series combination of C_C , the transformer inductance, and the reflected tank impedance. The low resistance of the network under series resonance will load the line, possibly decreasing range. For your particular line coupling circuit, measure for series resonance using some expected line impedance load.

R_B

This base-bleed resistor turns Q_B off quickly - important since the amplifier output swing is about 200V/ μ s. An R_B below about 24 Ω will conduct excessive current and overload the chip amplifier and is not recommended.



TL/H/6750-11

FIGURE 9. C_C 's impedance should be, as a rule-of-thumb, smaller than the lowest expected line impedance

R_G

This resistor, in parallel with the internal 10 Ω resistor, fixes the current gain of the output amplifier, and so the output current amplitude. Figure 11 gives output current and minimum AC current gain h_{fe} for Q_B when R_G is used to boost output current.

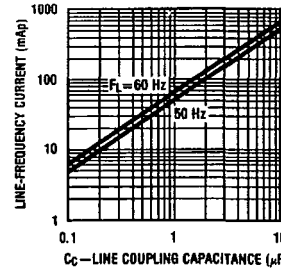
Q_B

The boost gain transistor Q_B must be fast. Double-diffused devices with 50 MHz F_T 's work, slower transistors (epi-base types) do not preserve a sinusoidal waveform when F_O is high or will cause the output amp. to oscillate. Q_B must have a certain minimum h_{fe} for given boost levels, as shown in Figure 11. Figure 12 shows the power Q_B must dissipate continuously operating with a shorted output. BV_{CER} ($R = R_B$) must be 60V or greater and Q_B must have adequate SOA for transient survival.

Z_T

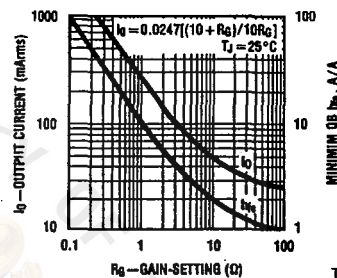
Unfortunately, potentially damaging transient energy passes through transformer T_1 onto the Carrier I/O pin (instanta-

neous power of greater than 1 kW has been measured using the recommended transformers). For self protection, the Carrier I/O has an internal 44V voltage clamp with a 20 Ω series resistance. A parallel low impedance 44V external transient suppression diode will then conduct the lion's share of any current when transients force the Carrier I/O to a high voltage.



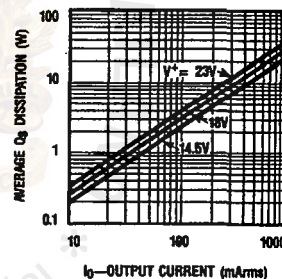
TL/H/6750-12

FIGURE 10. The AC line-induced current passed by C_C



TL/H/6750-13

FIGURE 11. Output amplifier current and required min. Q_B h_{fe} versus gain-setting resistor R_G



TL/H/6750-14

FIGURE 12. Boost transistor power dissipation versus amplifier output current

Z_T must be used unless some precaution is taken to protect the Carrier I/O pin from line transients or transients caused when stored line energy in C_C is discharged by the random phase of power line connection and disconnection. Worst case, C_C may discharge a full peak-to-peak line voltage into the tuned circuit. Another way to reduce the need for Z_T is by placing another magnetic circuit in the signal path that relies on a high, but easily saturated, permeability to couple a primary and secondary winding - a toroidal transformer for example. Toroids cost more than Z_T .

Use an avalanche diode designed specifically for transient suppression — they have orders of magnitude higher pulse

Component Selection (Continued)

power capability than standard avalanche diodes rated for equal DC dissipation. Metal oxide varistors have not proven useful because of their inferior clamping coefficient and are not recommended. Specifications for an example minimum diode are given in *Figure 13*.

Breakdown Voltage	44–49V @ 1 mA
Maximum Leakage	1 μ A @ 40V
Capacitance	300 pF @ BV
Maximum Clamp Voltage	64.5V @ 7.8A
Peak Non-Repetitive Pulse Power	10 kW for 1 μ s
(REA Standard Exponential Pulse)	
Surge Current	70A for 1/120s

FIGURE 13. Key specifications for a recommended transient suppressor Z_T available from General Semiconductor, 2001 West Tenth Place, Tempe, AZ 85281, 602–968-3101, part no. SA40A

R_T

R_T acts as a voltage divider with Z_T , absorbing transient energy that attempts to pull the Carrier Input pin above 44V. Make the resistor a carbon composition 1/4W. When experiments discharging C_C charged to the peak-to-peak 620V AC thru a 1 Ω power line were carried out, film resistors blew open-circuit.

D_T

This Schottky diode is placed in parallel with the CCT chip's substrate diode to pass the majority of the current drawn from ground when the Carrier Input or Carrier Output is pulled below ground by a larger-than-twice-the supply-swing on the tank. Note that Z_T is in parallel with the substrate diode, but is ineffective due to its high forward voltage drop and high diffusion capacitance caused by its low forward speed. Tests proved that a 1N5818 kept a receive-path functional with a 20X boost transmitter with a 7:1 transformer attempted to swing the receiver's Carrier I/O to $\pm 100V$ (300 mA peak ground current in the receiver). Without D_T , the receiver momentarily stops functioning at a 100 times lower ground current.

This diode is not needed if the Carrier I/O never swings below ground. If your CCT systems all run on the same regulated voltage with all matched transformers and turns ratios, it is not needed. Otherwise, it is.

THE RECEIVER

The receiver and transmitter share components C_C , T_1 , C_O , R_T , Z_T , C_O , R_O , and peripheral supply and bias components that are not in need of change for RX mode operation. Values for the balance of the components are now found.

Line-Frequency Rejection

To use the ultimate sensitivity of the device, fully 110 dB of 115 V, 60 Hz attenuation is required between the line and the limiter amplifier output. Using the circuit topology of *Figure 4*, the combined attenuation of the C_C/T_1 highpass, the tuned transformer, and the bandpass filter attenuation of the limiter amplifier give far more line rejection than the above-stated minimum. However, if some other CCT line coupling circuit is used, line rejection will become important to the system designer.

Receiver input power supply rejection (PSRR) and common-mode rejection (CMRR) are one-in-the-same using the supply-referenced signal input of *Figure 4*. Ripple swings both

differential inputs of the Norton amp. equally, while the single-ended input signal swings only the positive input. Overall PSRR consists of the input CMRR (set by the input stage component matching) and the ripple-frequency attenuation of the input amplifier bandpass response that passes carrier frequency but stops low frequencies. A typical 1% resistor and 1 mV n-p-n mirror offsets give 26 dB of attenuation, the bandpass gives 54 dB 120 Hz attenuation, for an overall 80 dB PSRR to allow tens of volts of ripple before impacting ultimate sensitivity.

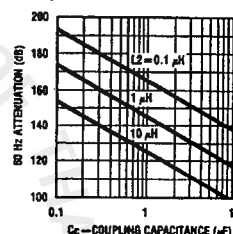
C_C

A value was chosen earlier. Knowing T_1 's secondary inductance allows a check of LC line attenuation using *Figure 14*.

C_L

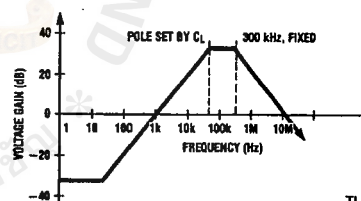
The Norton input limiter amplifier has a bandpass filter for enhanced receiver selectivity, noise immunity, and line frequency rejection. The nominal response curve for $F_O = 50$ kHz is shown in *Figure 15*. The 300 kHz pole is fixed. The 50 kHz pole is set by C_L 's value. After C_L is found, the resulting line frequency attenuation is found for the bandpass filter.

Use *Figure 15* to find a C_L value given for F_O . The approximate line frequency attenuation of the bandpass filter may then be found in *Figure 16*. *Figure 15* returns a value for C_L 33% larger than nominal, giving a low frequency pole 33% low to allow for component tolerances.

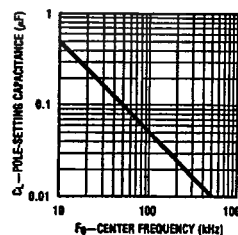


TL/H/6750-15

FIGURE 14. The 60 Hz line rejection of the highpass filter made up of C_C and T_1 's line-side winding (neglecting capacitive coupling)



TL/H/6750-16



TL/H/6750-17

FIGURE 15. Given F_O , C_L is found. Also shown is the input amplifier's small signal amplitude response

Component Selection (Continued)

C_F and R_F

These phase-locked loop (PLL) loop filter components remove some of the noise and most of the $2F_O$ components present in the demodulated differential output voltage signal from the phase detector. They affect the PLL capture range, loop bandwidth, damping, and capture time. Because the PLL has an inherent loop pole due to the integrator action of the ICO (via C_O), the loop pole set by C_F and the zero set by R_F gives the loop filter a classical 2nd-order response.

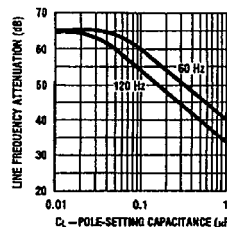


FIGURE 16. The Norton-input limiter amplifier bandpass filter line-frequency signal attenuation given C_L

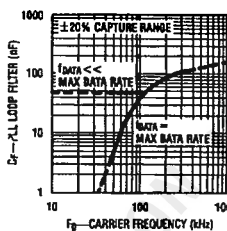


FIGURE 17. Find C_F given F_O . Figure 19 gives the maximum data rate

No C_F and R_F give the most stable PLL with the fastest response. Large C_F 's with a too-small R_F cause PLL loop instability leading to poor capture range and poor step response or oscillation.

Calculation of C_F and R_F is quite difficult, involving not only the 2nd-order loop step response, but also the PLL non-dominant poles, the tuned transformer stepped-frequency response, and the RC lowpass step response (for data rates approaching 1 kHz). C_F and R_F values are best found empirically. Tolerance is not critical. Component values are selected to give the best possible impulse noise rejection while preserving a $\pm 20\%$ capture range and wide stability margin. Figures 17 and 18 give C_F and R_F values versus F_O , where " $f_{DATA} < \text{MAX DATA RATE}$ " means that f_{DATA} should be less than the maximum data rate, in kHz, from Figure 19 divided by 10.

Note that C_F and R_F are a function of data rate only for high data rates and are not plotted against data rate - as one might expect. The reason for this is important to understand if the CCT system designer wishes to find C_F and R_F empirically. Data signal is, loosely speaking, passed through the PLL loop and is therefore potentially attenuated if the loop bandwidth is on the order of the 3rd harmonic of the data rate, or less. Overall loop bandwidth is held as low as possible for maximum noise rejection while passing the data. Loop bandwidth is roughly proportional to the geometric mean of the unfiltered loop bandwidth and the filter pole set by C_F . Therefore, C_F is related to data rate. Unfortunately, the loop capture range falls to critically low values when large enough values of C_F are used to reduce loop bandwidth down to the 100's of Hz range, for low data rates. The

obvious way out is to then reduce the unfiltered loop bandwidth. That bandwidth is approximately proportional to the value of C_O . For a fixed F_O , unfiltered loop bandwidth reduction requires a larger C_O and larger control current. With this chip, changing the control current is not allowed. So one is forced to choose a C_F/R_F combination with some minimum capture range, say $\pm 20\%$, that is within some guardband from the point of loop instability. Happily, impulse noise tends to last only fractions of a millisecond so that the lack of low bandwidth loop response with low data rates is not a heavy penalty. As long as there is adequate capture range, the impulse noise filter performs admirably. Note that reducing F_O will reduce the no-filter loop bandwidth, and indeed the maximum data rate falls below the limit set by the RC lowpass filter as F_O falls below 100 kHz (Figure 19).

The tuned transformer characteristics will affect the demodulated data waveform more than C_F and R_F at low data rates. Tank Q and off-tuning will affect overshoot during the FSK frequency steps. This is a property of tuned circuits. The maximum data rate of Figure 19 is measured from the receiver input to the Data Out and does not include the data bandwidth reducing effects of T_P .

C_M

Capacitor C_M stores a voltage corresponding to a correction factor required to cancel the phase detector differential output DC offsets. The stored voltage is $\frac{1}{2}$ of the DC offset plus some bias level of about 2.2 V. A large C_M value increases the time required to bias-up the receive path at the beginning of transmission. A large C_M does filter well and store its bias voltage long. Because of the initial random charge of C_M , the receiver must be given a data transition to charge to the proper bias voltage. Therefore, reducing C_M 's value to one that may be charged in less than 2 bit-times will not save biasing time and is not recommended.

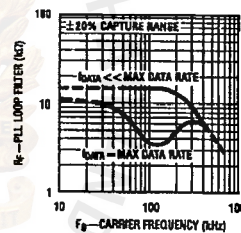


FIGURE 18. Find R_F given F_O with F_{DATA} a parameter

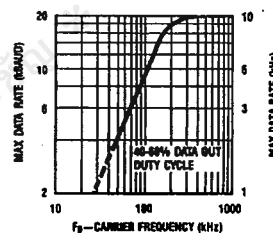


FIGURE 19. The maximum data rate versus F_O using loop filter components optimized for max. noise performance while retaining a min. $\pm 20\%$ capture range (large signal)

Use Figure 20 to find C_M 's value knowing f_{DATA} , assuming the standard 2 bit receive charge time is desired. The cap. value and TC are not critical, but the capacitor should have low leakage.

Component Selection (Continued)

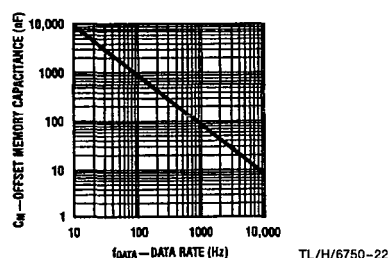


FIGURE 20. Size C_M assuming a 2 bit-time receive bias time

C_I

The impulse noise filter integrator capacitor C_I is used to disallow the passage of any pulse shorter than the integrator charge time. That charge time, set to a nominal $\frac{1}{2}$ bit time, is the time required for a $\pm 50 \mu A$ charge current to swing C_I over a $2 V_{BE}$ range. Charge time under worst case conditions must never be greater than a bit time since no signal could then pass. Using a $\pm 10\%$ capacitor, full junction temperature range, and full specified current range, a maximum nominal charge time of $\frac{1}{2}$ bit is recommended. Figure 21 gives C_I versus data rate under those conditions.

R_C

The collector pull-up resistor is sized to supply adequate pull-up current drive and speed while preserving adequate output low current drive.

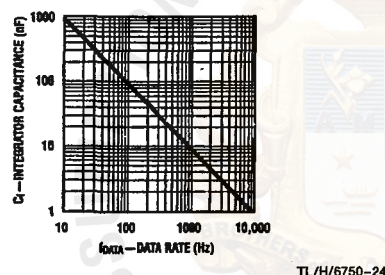


FIGURE 21. Impulse noise filter cap. C_I versus f_{DATA} where the charge time is $\frac{1}{2}$ bit time

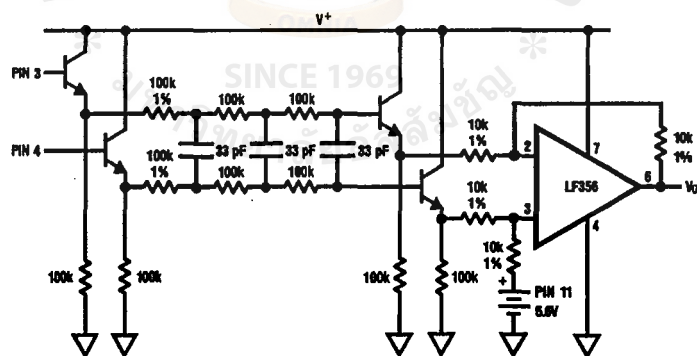


FIGURE 22. Circuit to view the differential demodulated data signal, minus the noise and $2F_0$ components, conveniently with a single-ended gain-of-one output

Z_A

The 5.1V silicon zener diode Z_A is required when a short RX-to-TX switch-over time is needed at the same time that the chip is operating in the RX mode with a pin 10 input signal swing approaching or exceeding twice the supply voltage. Predominant causes of these large swings impinging on the RX input are: 1) a transmitter's supply voltage higher than the receiver's supply voltage, 2) a TX and RX pair that are electrically close, or, 3) a higher RX T_1 step-up turns ratio than the TX T_1 step-down ratio.

Normally, when in the RX mode with small incoming signal on pin 10, the ALC remains off with pin 7 at a 6V ($V_Z - 2V_{BE}$) bias voltage. C_A is then charged to 6V. TX mode may then be selected with 6V on C_A allowing 100% TX power to pump T_1 's tuned circuit, and so the AC line, quickly for fast RX-to-TX switch time. As TX output swing increases so that pin 10 swings below V_{ALC} (4.7V typically), that ALC activates to charge C_A to about 6.6V to reduce TX output drive. However, if in the RX mode pin 10 ever swings below V_{ALC} , C_A will charge to above 6.6V. Now, when the TX mode is selected with C_A at 6.6V, somewhere from 0 to 100% TX output drive is available to pump T_1 's tuned circuit resulting in a slower rising line signal - effectively reducing the RX-to-TX switch time.

Use a 5.1V Z_A driven by a 0 to 0.8V logic low signal to guarantee over-temp. operation. R_A must be in series with Z_A to limit current flow and should never fall below 1 k Ω . If R_A is less than 1 k Ω , then put a 2 k Ω resistor in series with Z_A . Logic high voltages above 10V will cause current flow into pin 7 that must be limited to 1 mA (with R_A or a series R).

Breadboarding Tips

During CCT system evaluation, some techniques listed below will simplify certain measurements.

- Use caution when working on this circuit - dangerous line voltages may be present.
- When evaluating PLL operation, offset cancel circuit operation, and loop filter values, use the filter of Figure 22 to view the demodulated signal minus the $2F_0$ and noise components. This filter models the RC lowpass filter on chip.

Breadboarding Tips (Continued)

- When evaluating OCT system noise performance on a real power line, it is desirable to vary the signal amplitude to the receiver. This is not easy. An in-line line-proof L-pad is fine except that the line impedance is unknown and variable and so the L-pad will rarely match. Instead, the power output of a chip transmitter may be controlled using the circuit of *Figure 23*. This circuit controls the ALC.
- It is sometimes desirable to place impulse noise on the line. A simple light dimmer with a 100 W light bulb load produces representative impulse noise.
- Do not allow peak currents of over 1 A through the 5.6 V Zener. In other words, don't short charged capacitors into this low-impedance device. Take care not to momentarily short pins 10 and 11 - chip damage may result.
- *Figure 24* shows some typical signals beginning with serial data transmitted to received signal.

Tuning Procedure

This procedure applies to circuits similar to *Figure 4* LM1893 or LM2893 circuit.

First, trim F_O by putting the chip in the TX mode, setting a logical high data input, and measuring the TX high frequency, $1.022 F_O$, on the Carrier I/O using these steps:

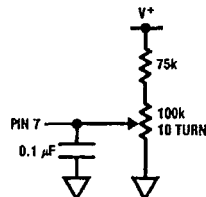
1. Take pin 17 to a logic low.
2. Take pin 5 to a logic high.
3. Place a counter on pin 10.
4. Adjust R_O on pin 18 for $F = 1.022 F_O$.

Second, the line transformer is tuned. The chip is placed in the TX mode, a resistive line load is connected to disable the ALC by reducing tank voltage swing below its limit. FSK data is then passed through the tank so that the tank envelope may be adjusted for equal amplitude for high and low data frequency.

1. Take pin 5 to a logic high.
2. Place a logic-level square wave at or below the receiver's maximum data rate on pin 17.
3. Temporarily place a 330 Ω resistor across the tank.
4. Place a scope on pin 10.
5. Adjust the transformer slug for the least envelope modulation.

In lieu of the 330 Ω resistive load, T_1 may be coupled to the power line to better simulate actual load and tank pull conditions during tank tuning. Alternatively, a passive network

representing an average line impedance may be connected to the line side of T_1 . The circuit of *Figure 23* should then be used to defeat the leveling effect of the ALC.



TL/H/6750-26

FIGURE 23. A means of transmitter output amplitude control is shown

Thermal Considerations

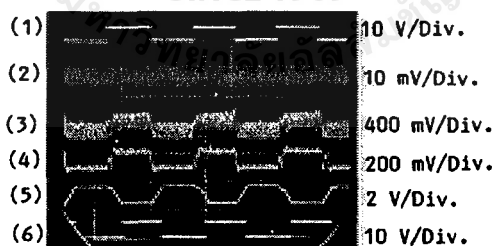
It is desirable to place the largest possible signal on the power line for maximum range, limited only by the chip power dissipation and maximum junction temperature T_J . The falling output power at elevated T_J allows a more optimal power output - high power at low T_J and lower power at high T_J for chip self-protection. However, it is still possible to exceed the maximum T_J within the specified ambient temperature limit ($T_A = 85^\circ\text{C}$) under worst case conditions of 100% TX duty cycle, high supply, shorted load, poor PC board layout (with small copper foil area), and an above nominal current part. Under those conditions, a part may dissipate 2140 mW, reaching a $T_J = 170^\circ\text{C}$ worst-case (admittedly a rare occurrence). Proper system design includes the measurement or calculation of T_J max. to guarantee function under worst-case operation. Like all devices with failure modes modeled by the Arrhenius model, the high chip reliability is further enhanced by keeping the die temperature mercifully below the absolute maximum rating.

A direct method of measuring operating junction temperature is to measure the V_{BE} voltage on pin 18, which is always available under all operating modes. The graph of *Figure 25* may be used to find T_J , knowing V_{BE} at the operating point in question and V_{BE} at $T_A = T_J = 25^\circ\text{C}$. V_{BE} is found by powering up a chip (in RX mode) that has been dissipating zero power at some T_A for some time and measuring V_{BE} in less than 1 s (for better than 5°C accuracy).

Alternately, T_J may be calculated using:

$$T_J = T_A + \theta_{JA} P_D \quad (1)$$

where θ_{JA} is 75°C/W for the plastic (N) package using a socket. That θ_{JA} value is for a high confidence level; nomi-



TL/H/6750-23

FIGURE 24. Oscilloscope revealing signals at several important nodes under weak signal ($0.5 \text{ mV}_{\text{RMS}}$) conditions with SCR spikes on an otherwise quiet 115 V, 60 Hz power line. The signals are: 1) transmitted data, 2) RX carrier on the tuned transformer, 3) demodulated signal from the PLL after passing thru circuit of *Figure 22*, 4) signal after RC lowpass, 5) data at impulse noise filter integrator, and 6) received data. Horizontal scale is 10 ms per div.

Thermal Considerations (Continued)

nal θ_{JA} for an N package is $60^{\circ}\text{C}/\text{W}$, lower with good PC board layout. Since P_D is a relatively strong function of T_J , an iterative solution process starting with an initial guess for T_J is used. With the estimated T_J , find the total supply current found in the typical performance characteristics.

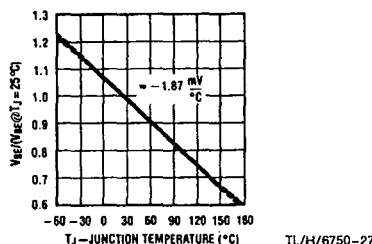


FIGURE 25. T_J may be found by using the temperature coefficient of pin 18 V_{BE} if V_{BE} is known at 25°C

Transmit-To-Receive Switch-Over Time

An important figure-of-merit for a half-duplex CCT link, affecting effective data rate, is the TX-to-RX switch time T_{TR} . Using the recommended component values gives this part a nominal 2 bit-time (1 bit time = $1/[2f_{DATA}]$) over a wide range of operating conditions, where the receiver requires 1 data transition. T_{TR} cannot be decreased significantly but does increase as noise filtering, especially via C_M , is increased. Impulse noise at switch, signals near the limiting sensitivity, poor F_O match between receiver and transmitter because of poor trim or worst-case conditions, and the statistical nature of PLL signal acquisition may all contribute to increase T_{TR} to possibly 4 bit-times.

T_{TR} is lower when a pair of LM1893's handshake rapidly. The receiver was designed to "remember" the RX-mode DC operating points on C_M and C_F while in the TX mode. Under noisy worst case conditions, C_M will discharge to the point of false operation after 35 bit-times in the TX mode (1400 bit times with no noise and a nominal part, $f_{DATA} = 180 \text{ Hz}$). T_{TR} is about 0.8 ms (proportional to the selected F_O) plus $\frac{1}{2}$ bit-time.

The major components of T_{TR} are described below for a nominal 125 kHz F_O , 180 Hz f_{DATA} , lightly-loaded tank with a Q of 20, and the circuit of Figure 4. The remote CCT has been operating in the TX mode with a 26.6 V_{PP} tank swing and is now selected as a receiver. An incoming signal requiring the ultimate receiver sensitivity immediately is placed on the line.

First, the tank stored energy at the transmit frequency must decay to a level below the 2.8 mV_{PP} swing caused by the 0.14 mV_{RMS} incoming line signal containing the information to be received.

$$\text{decay time} = \frac{Q}{\pi F_O} \ln \left(\frac{V_1}{V_O} \right) = \frac{20}{\pi \times 125\,000} \ln \left(\frac{26.6}{0.0028} \right) = 0.466 \text{ ms} \quad (2)$$

That is 0.47 ms of delay (proportional to $1/F_O$ and Q).

Second, the PLL must acquire the signal; it must lock and settle. Acquisition time is statistical and may take any length of time, but average acquisition time depends on the loop filter components C_F and R_F and the difference in center frequencies, ΔF_O , of the TX/RX pair. Using the recom-

mended C_F and R_F (47 nF and 6.2 k Ω) with a $\pm 4.4\%$ ΔF_O (a $\pm 100 \text{ mV}$ DC offset on C_F and R_F), lock was measured to take less than 50 cycles of F_O . That is a 0.40 ms delay (proportional to $1/F_O$).

Acquisition is incomplete until the second order PLL loop settles. For the above-mentioned C_F and R_F , the loop natural frequency F_N and damping factor are found to be 2.3 kHz and 1.0 respectively. Settling to within $\pm 25 \text{ mV}$ of the $\pm 100 \text{ mV}$ DC offset change requires 2.7 periods of F_N , or 1.2 ms (a function of C_F and R_F).

Third, the RC lowpass filter introduces a 0.12 ms delay.

Fourth, C_M must charge up to $\pm (5\%)100 = 83 \text{ mV}$ depending on the polarity of F_O . Borderline data squaring with zero noise immunity is possible with only $\pm (5\%) 50 \text{ mV}$ of charging. C_M charge current is an asymptotic function approximated by assuming a 50 μA charge current and the full 83 mV charge voltage. C_M charge time is then 1.7 ms (proportional to $1/f_{DATA}$).

Fifth, the impulse noise filter adds a $\frac{1}{2}$ bit-time delay. Total T_{TR} is 3.9 ms plus $\frac{1}{2}$ bit-time for a total of 1.9 bit-times at 360 Baud.

Receive-To-Transmit Switch-Over Time

Assume the chip has been in the RX mode and the TX mode is now selected. In less than 10 μs , full output current is exponentially building tank swing. 50% of full swing is achieved in less than 10 cycles - or under 80 μs at 125 kHz. In the same 10 μs that the output amp went on, the phase detector and loop filter are disconnected and the modulator input is enabled. FSK modulation is produced in 10 μs after switching to TX mode.

Power Line Impedance

Irrespective of how wide the limits on power line impedance Z_L are placed, there are no guarantees. However, since the CCT design requires an estimate of the lowest expected line impedance Z_{LN} encountered for the most efficient transmitter-to-line coupling, line impedance should be measured and Z_L limits fixed to a given confidence level. Reasonable values for T_1 turns ratio, loaded Q, and tank resonant frequency pull F_O may be found to enable a CCT system design that functions with the overwhelming majority of power lines.

A limited sampling of Z_L was made, during the LM1893 design, of residential and commercial 115V 60 Hz power line. Data was also drawn from the research of Nicholson and Malack (reference 1), among others, to produce Figures 26 and 27. All measured impedances are contained within the shaded portions of Figure 27. A nominal 3.5, 7.0 and 14 Ω Z_{LN} is used throughout the application information with a nominal 45° phase angle (0° is sometimes used for simplicity).

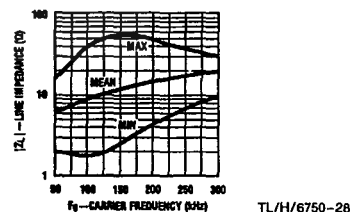


FIGURE 26. Measured line impedance range for residential and commercial 115V, 60 Hz lines

Power Line Impedance (Continued)

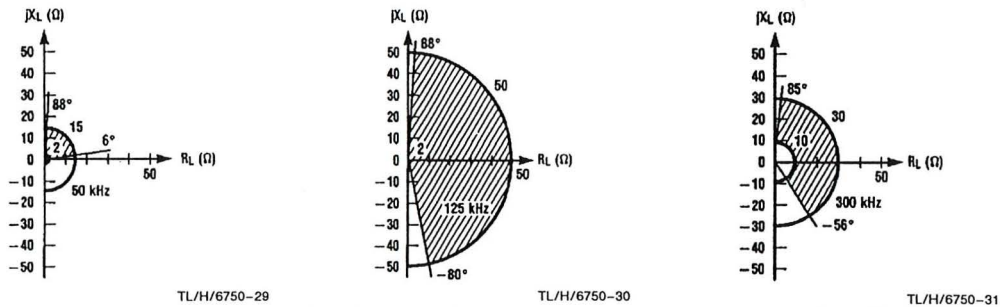


FIGURE 27. Complex-plane plots of measured 115V, 60 Hz line impedance where $Z_L = R_L + jX_L$

Power Line Attenuation

The wiring in most US buildings is a flat 3 conductor cable called Amerflex, BX, or Romex. All referenced line impedances refer to hot-to-neutral impedances with a grounded center conductor. The cable has a 100 Ω characteristic impedance, a 125 kHz quarter-wavelength of 600 m (250 m at 300 kHz), and a measured 7 dB attenuation for a 50 m run with a 10 Ω termination. Generally, line loads may be treated as lumped impedances. Instrument line cords exhibit about 0.7 μ H and 30 pF per meter.

Limited tests of CCT link range using this chip show extensive coverage while remaining on one phase of a distribution transformer (100's of m), with link failure often occurring across transformer phases or through transformers unless coupling networks are utilized. Total line attenuation allowed from full signal to limiting sensitivity is more than 70 dB. Typically, signal is coupled across transformer phases by parasitic winding capacitance, typically giving 40 dB attenuation between phased 115 V windings. Coupling capacitors may be installed for improved link operation across phases. Power factor correcting capacitor banks on industrial lines or filter capacitors across the power lines of some electronic gear short carrier signal and should be isolated with inductors. Increasing range is sometimes accomplished by electing to install the isolating inductors (Figure 28) and coupling capacitors, as well as by electing to use the boost option. Frequency translating or time division multiplexed repeaters will also increase range.

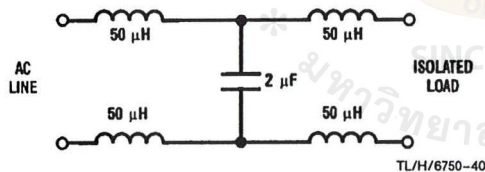


FIGURE 28. An isolation network to prevent: 1) noise from some device from polluting the AC line, and 2) to stop some low impedance device (measured at F_0) from shorting carrier signal. Component values given as an example for $F_0 = 125$ kHz on residential power lines

The Coupling Transformer

The design arrived at for T_1 is the result of an unhappy compromise - but a workable one. The goals of 1) building

T_1 with a stable resonant frequency, F_0 , that is little affected by the de-tuning effect of the line impedance Z_L , and of 2) building a tightly line-coupled transformer for transmitted carrier with loose coupling for transients, are somewhat mutually exclusive. The tradeoffs are exposed in the following example for the CCT designer attempting a new boost-capable, or different core, transformer design.

The compromises are eased by separating the TX output and RX input in the LM2893. An untuned TX coupling transformer with only core coupling (not air-coupled solenoid windings) would employ a high permeability, high magnetic field, low loss, square saturating, toroidal core. The resonant RX path would be isolated from line-pull problems by a unilateral amplifier that operates at line voltages with much more than 110 dB of dynamic range, or by a capacitively coupled pulse transformer driving a unilateral amplifier and filter, for increased selectivity. See the LM2893-specific applications section.

For a LM1893-style transformer application, first, choose the turns ratio N based on an estimated lowest Z_L likely encountered, Z_{LN} . Figure 29 shows graphically how N affects line signal. N should be as large as possible to drive Z_{LN} with full signal. If T_1 has an unloaded Q , Q_U , of well less than 35, a guess of N somewhat high should be used and later checked for accuracy. The recommended transformers have secondary taps giving a choice of $N = 7.07$, 10, and 14.1 (nominally) for driving Z_{LN} 's of 14, 7.0, and 3.5 Ω respectively (at $T_J = 25^\circ\text{C}$, $V_+ = 18\text{V}$, and $Q_U = 35$).

The resonating inductance of the tuned primary, L_1 , is sought. Note that, while standard transformer design gives a transformer self-inductance with an impedance at operating frequency well above load impedance, the tuned transformer requires a low L_1 for adequate Q_U and minimum line pull. Result: relatively poor mutual coupling.

$$L_1 = \frac{R}{2\pi F_0 Q} \quad (3)$$

It is known that resonant frequency $F_Q = F_0$ and some minimum bandwidth, or maximum Q , will be required to pass signal under full load conditions.

$$L_1 = \frac{R_Q \parallel |Z_{LN}'|}{2\pi F_0 Q_L} \quad (4)$$

$|Z_{LN}'|$ is the reflected Z_{LN} , Q_L is the loaded Q , and parallel resistance R_Q models all transformer losses and sets Q_0 . $R_Q \parallel |Z_{LN}'|$ is found knowing that it absorbs full rated power.

The Coupling Transformer (Continued)

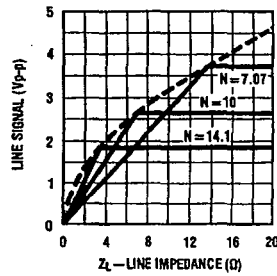


FIGURE 29. Impressed line voltage for a given Z_L for each of the 3 taps available on the recommended transformers

$$P_O = I_O V_O = \frac{I_{OPP}}{2\sqrt{2}} \left[\frac{2(-V_{ALC} + V_+)}{2\sqrt{2}} \right] = \frac{(-4.7 + V_+) I_O}{4} \quad (5)$$

where I_O is in amps peak-to-peak at an elevated T_J

$$P_O = \frac{(18 - 4.7) 0.06}{4} = 0.200 \text{ W} \quad (6)$$

$$R_Q \| |Z_{LN}|' = \frac{V_O^2}{P_O} = \frac{(-V_{ALC} + V_+) \sqrt{2}}{I_O} = 442 \Omega \quad (7)$$

R_Q is found using Z_{LN} and the value for N found when assuming $Q_U = 35$.

$$|Z_{LN}|' = N^2 Z_{LN} = (7.07)^2 13.9 = 695 \Omega \quad (8)$$

$$R_Q = \frac{1}{\frac{1}{R_Q \| |Z_{LN}|'} + \frac{1}{|Z_{LN}|'}} = \frac{1}{\frac{1}{442} + \frac{1}{695}} = 1210 \Omega \quad (9)$$

$$R_{QS} = \frac{R_Q}{1 + Q_U^2} = \frac{1210}{1 + 35^2} = 1 \Omega \quad (10)$$

Only Q_L remains to be found to calculate L_1 . Q_L is related to the -3 dB (half-power) bandwidth by

$$Q_L = \frac{1}{\text{BW (\% of } F_O)} \quad (11)$$

An iterative solution is forced where line pull, ΔF_Q , must be guessed to find Q_L and L_1 . L_1 is then used to check the line pull guess; a large error requires a new guess. Try a BW of 8.7% - that is 4.4% for deviation, 1% for TC of F_O , and 3.3% for ΔF_Q - giving $Q_L = 11.5$.

$$L_1 = \frac{442}{2\pi \times 125\,000 \times 11.5} = 49.0 \mu\text{H} \quad (12)$$

Knowing the core inductance per turn, L , and L_1 , the number of turns is found.

$$T_1 = \sqrt{\frac{L_1}{L}} = \sqrt{\frac{49.0 \mu\text{H}}{20 \text{ nH/T}}} = 49 \frac{1}{2} \text{ turns} \quad (13)$$

T is normally an integer, but these transformers require so few turns that half-turns are specified, remembering that the remaining $\frac{1}{2}$ turn is completed on the P.C. board and is loosely coupled. The secondary turns are calculated

$$T_2 = \frac{T_1}{N} = \frac{49.5}{7.07} = 7.00 = 7 \text{ turns} \quad (15)$$

giving an L_2 of $0.98 \mu\text{H}$. Note that the recommended 125 kHz transformer mirrors these specifications. The resonant capacitor is

$$C_Q = \frac{1}{(2\pi F_Q)^2 L_1} = 33.1 \times 10^{-9} = 33 \text{ nF} \quad (16)$$

Line pull ΔF_Q was calculated (reference 3) for a Z_L magnitude of 14Ω and up with any phase angle from -90° to 90° . ΔF_Q was 6.4% - well above the 3.3% estimate. Referring to (11), an 11.8% bandwidth is required, forcing L_1 to be reduced to reduce Q . That fix was not implemented; some signal attenuation under worst-case drift and ΔF_Q is allowed. L_1 is already so small that the 31 gauge winding conducts a $\frac{1}{4}$ ARMS circulating current.

Line Carrier Detection

While the addition of a carrier detection circuit (for a mute or squelch function) will only decrease receiver ultimate sensitivity, there is sometimes good reason to employ it to free the controller from watching for RX signal when no carrier is incoming, or to employ it to reduce the probability of line collisions (when multiple transmitters operate simultaneously to cause one or more transmissions to fail). Unless the detector is heavily filtered or uses a high carrier amplitude threshold, there will be false outputs that force the controller to have Data Out data checking capability just as is required when using no carrier detector. If false triggering is minimized, the probability of line collisions is increased due to the inability to sense low carrier amplitudes and because of sense delay. The property of the LM1893 to change output state infrequently (although the polarity is undefined) when in the RX mode, with no incoming carrier, reduces the desire to implement carrier detection and preserves the full ultimate sensitivity. Also, many impulse-noise insensitive transmission schemes, like handshaking, are easily modified to recover from line collisions.

Regarding this, it should be stated that for very complicated industrial systems with long signal runs and high line noise levels, it is probably wise to use a protocol which is inherently collision free so that no carrier detect hardware or software is needed. A token passing protocol is an example of such a system.

Figure 30 shows a low cost carrier amplitude detection circuit.

Audio Transmission

The LM1893 is designed to allow analog data transmission and reception. Base-band audio-bandwidth signals FM modulate the carrier passing through the tuned transformer (placing a limit on the usable percent modulation) onto the power line to be linearly demodulated by the receiver PLL. Because the receiver data path beyond the phase detector will pass only digital signal, external audio filtering and amplification is required. Figure 31 shows a simple audio transmitter and receiver circuit utilizing a carrier detection mute circuit. A single LM339 quad. comparator may be used to build the carrier detect and mute. Filter bandwidth is held to a minimum to minimize noise, especially line-related correlated noise.

Communication and System Protocols

The development of communication and system protocols has historically been the single most time consuming element in design of carrier current systems. The protocols are defined as the following:

1. *Communication protocol*: a software method of encoding and decoding data that remains constant for every transmis-

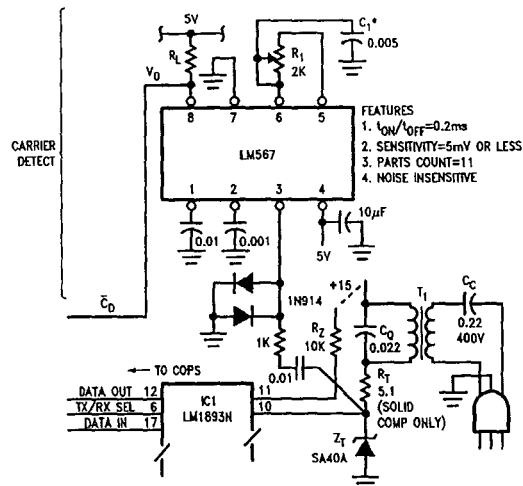


FIGURE 30. A simple carrier amplitude detector with output low when carrier is detected

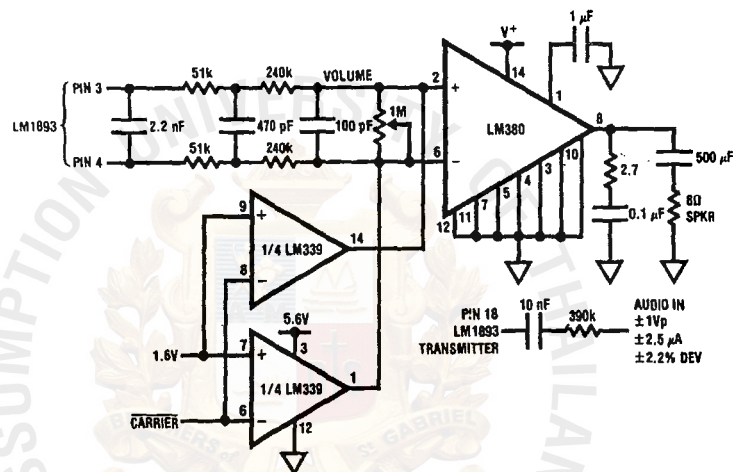


FIGURE 31. A simple linear analog audio transmitter and receiver are shown. The carrier and 1.6V inputs are derived from the carrier detector of Figure 30. The remaining 2 LM339 comparators may be used to build the carrier detector circuit.

Communication and System Protocols (Continued)

sion in a system. Its first purpose is to put data in a baseband digital form that is more easily recognized as a real message at the receive end. Secondly, it incorporates encoding techniques to ensure that noise induced errors do not easily occur; and when they do, they can always be detected. Lastly, the software algorithms that are used on the receive end to decode incoming data prevent the reception of noise induced "phantom" messages, and insure the recovery of real messages from an incoming bit stream that has been altered by noise.

2. System protocol: the manner in which messages are coordinated between nodes in a system. Its first purpose is to

ensure message retransmission to correct errors (handshake). Secondly it coordinates messages for maximum utilization and efficiency on the network. Lastly, it ensures that messages do not collide on the network. Common system protocols include master-slave, carrier detect multiple access, and token passing. Token passing and master slave have been found to be the most useful since they are inherently collision free.

Both protocols usually reside as software in a single microcontroller that is connected to the LM1893/2893 I/O. In any case, some sort of intelligence is needed to process incoming and outgoing messages. UARTs have no usefulness in

Communication and System Protocols (Continued)

carrier current applications since they do not have the intelligence needed to distinguish between real messages and noise induced phantoms.

The difficulty in designing special protocols arises out of the special nature of the AC line, an environment laden with the worst imaginable noise conditions. The relatively low data rates possible over the AC line (typically less than 9600 baud) make it even more imperative that systems utilize the most sophisticated means available to ensure network efficiency.

With these facts in mind, the designer is referred to a publication intended to aid in the development of carrier current systems. This is literature #570075 The Bi-Line Carrier Current Networking System, a 200 pp. book that functions as the "bible" of Bi-Line system design. It has sections on LM1893 circuit optimization, protocol design, evaluation kit usage, critical component selection, and the Datachecker/DTS case study.

Basic Data Encoding (please refer to the previously mentioned publications for advanced techniques)

At the beginning of a received transmission, the first 0 to 2 bits may be lost while the chip's receiver settles to the DC bias point required for the given transmitter/receiver pair carrier frequency offset. With proper data encoding, dropped start bits can be tolerated and correct communication can take place. One simple data encoding scheme is now discussed.

Generally, a CCT system consists of many transceivers that normally listen to the line at all times (or during predetermined time windows), waiting for a transmission that directs one or more of the receivers to operate. If any receiver finds its address in the transmitted data packet, further action such as handshaking with the transmitter is initiated. The receiver might tell the transmitter, via retransmission, that it received this data, waiting for acknowledgement before acting on the received command. Error detecting and correcting codes may be employed throughout. The transmitter must have the capability to retransmit after a time if no response from the receiver is heard - under the assumption that the receiver didn't detect its address because of noise, or that the response was missed because of noise or a line collision. (A line collision happens when more than 1 transmitter operates at one time - causing one or more of the communications to fail). After many re-transmissions the transmitter might choose to give up. Collision recovery is achieved by waiting some variable amount of time before re-

transmission, using a random number of bits delay or a delay based on each transmitter's address, since each transceiver has a unique address.

An example of a simple transmission data packet is shown in Figure 32. The 8 bit 50% duty-cycle preamble is long enough to allow receiver biasing with enough bits left over to allow the receiver controller to detect the square-wave that signals the start of a transmission. If there had been no transmission for some time, the receiver would simply need to note that a data transition had occurred and begin its watch for a square-wave. If the receive controller detected the alternating-polarity data square-wave it would then use the sync. bit to signal that the address and data were immediately following. The address data would then be loaded, assuming the fixed format, and tested against its own. If the address was correct, the receiver would then load and store the data. If the address was not correct, either the transmission was not meant for this receiver or noise has fooled the receiver. In the former case, when the transmission was not meant for the receiver, the controller should immediately return to watching the incoming data for its address. If the later case were true, then the receive controller would continue to detect edges, tying itself up by loading false data and being forced to handshake. The square-wave detection and address load and check routines should be fast to minimize the time spent in loops after being false-triggered by noise. If the controller detects an error (a received data bit that does not conform to the pre-defined encoding format) it should immediately resume watching the LM1893's Data Out for transmissions, the next bit would be shifted in and the process repeated.

A line-synchronous CCT system passing 3 bits per half-cycle may replace the long 8 bit preamble and sync pulse with a 2 bit start-of-transmission bias preamble. The receive controller might then assume that preamble always starts after bit 1 (the first bit after zero-crossing) so that any data transition at a zero crossing must be the start of the address bits and is tested as such. The line synchronous receiver operates with a simpler controller than an asynchronous system. Discussion has assumed that the controller has always known when the Data Out is high or low. The controller must sample at the proper time to check the Data Out state. Since noise shows itself as pulse width jitter, symmetrically placed about the no-noise switch-points, optimum Data Out sampling is done in the center of the received data pulse. The receive data path has a time delay that, at low data rates, is dominated by the impulse noise filter integrator and is nominally $\frac{1}{2}$ bit. At a 2 kHz data rate, an additional delay of approximately $\frac{1}{10}$ bit is added because of the cumulative delay of the remainder of the receiver. Figure 33 shows that Data Out sampling occurs conveniently at the transmitted

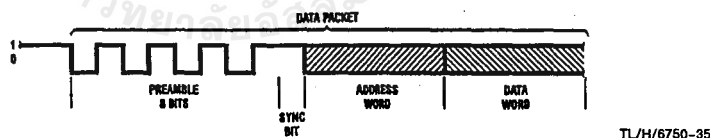


FIGURE 32. A simple encoded data packet, generated by the transmit controller is shown. The horizontal axis is time where 1 bit time is $1/(2f_{DATA})$

(Continued)



FIGURE 33. Operating waveforms of a line-synchronized transceiver pair are shown. The diagram shows how the transmitted data transitions may be used as received data sampling points

data edges for the line synchronous data transmission scheme mentioned in the previous paragraph. With the asynchronous system suggested, the receive controller must sample the Data Out pin often to determine, with several bits of accuracy, where the square-wave data transitions take place, average their positions assuming a known data rate, and calculate where the center of the data bits are and will continue to be as the address and data are read. A long preamble is helpful. Software that continuously updates the center-of-bit time estimate, as address and data are received, works even better. Alternatively, a coding scheme employing an embedded clock can be used.

LM2893 Application Hints

The LM2893 is intended for advanced applications where special circuitry is used in the transmit and receive paths. The LM2893 makes this possible by featuring separate transmit output and receive input pins.

Examples of enhancements that can be added to the basic LM1893/2893 circuit include separate transmit and receive windings on the coupling transformer, high quality ceramic or LC filters in the receive path, and simple impulse noise blanking circuits.

In many applications, the additional performance to be gained outweighs the extra cost of the additional circuitry. More than likely, high performance industrial applications such as building energy management will fit into this category, since they require the utmost in reliability.

Because of the specialized nature of individual LM2893 applications, it is not possible to give one circuit that will satisfy all requirements for performance and cost effectiveness. Therefore no specific application examples will be given. Instead the subsequent text describes in general terms the types of circuits that can be used to increase performance along with their advantages and disadvantages. It is intended to be a springboard for ideas.

LM2893 COUPLING NETWORKS

The main disadvantages of the typical LM1893 coupling network are that it functions as the bandpass filter, has loose coupling between primary and secondary, and has a single secondary. The LM1893 coupling network was designed this way mainly because of the restraint that the carrier input and output are tied together.

Because the coupling transformer is used as a filter, the LM1893 circuit is susceptible to pulling of the center frequency under conditions of changing line impedances or when several LM1893 circuits are close in proximity on the AC line. Because the tuned transformer has a high value of "Q", ringing also occurs in the presence of impulsive noise. This ringing occurs at the center frequency and increases the error rate of transmissions, especially at relatively high data rates (> 2000 baud). Because it is the only tuned circuit in the system, the selectivity characteristics leave a lot to be desired.

The LM2893, having separate receive input and transmit output pins, removes the limitations on coupling transformer design, allowing the design of circuits devoid of the previous limitations.

The first enhancement that can be made with the LM2893 circuit is the use of a high permeability ferrite toroid for line coupling along with a separate filter. The transformer would be of broadband design (untuned) with two secondaries, one for coupling to the transmit output and one for coupling to the receive input. This allows impedance matching of both the transmitter and receiver, with the result of quite a bit more receive sensitivity.

Because of the increased signal and separate receive signal path, a 3 or 6 db pad can be used before the selective stages to eliminate pulling of the center frequency due to changes in line impedance.

Another advantage of the toroidal transformer is that it can be designed for use at very low line impedances due to its inherent tight coupling.

SEPARATE FILTER

Because of the separate receive path of the LM2893, a relatively high quality bandpass filter can be used for selectivity. Inexpensive ceramic filters are available that have bandpass and center frequency characteristics compatible with carrier current operation. Furthermore, the use of these filters allows multichannel operation, previously made difficult by the single tuned network of the LM1893. These filters are easily cascaded for even more off-frequency rejection. If the pad is added before the filter, there will be negligible pulling due to changes in line impedance reflected through the coupling transformer.

Alternatively, a Butterworth/Chebyshev bandpass LC filter or an active filter can be used in place of the ceramic filter.

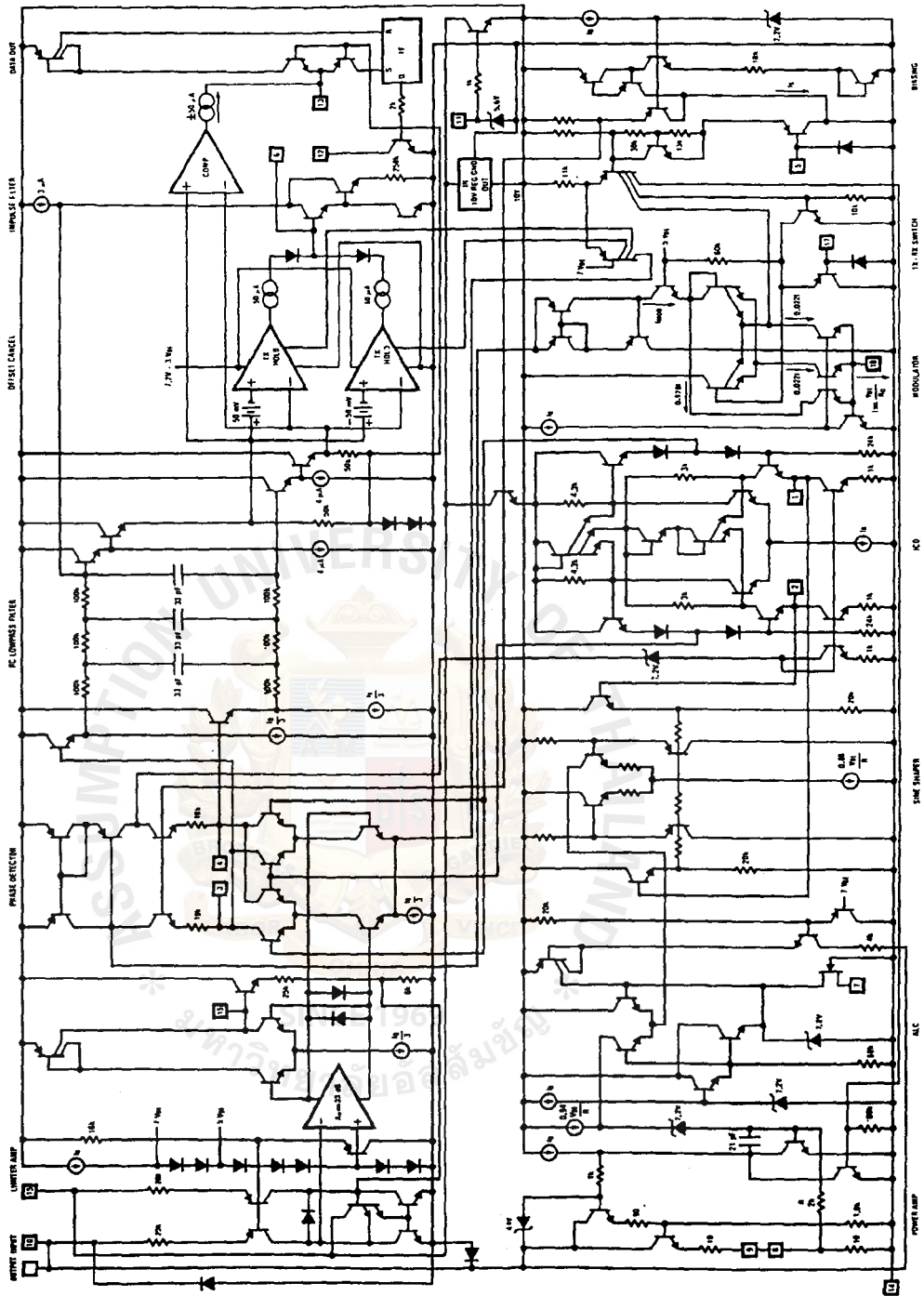
IMPULSE NOISE BLANKER

Although the LM2893 has adequate impulse noise rejection for most applications, there is reason to employ impulse blanking to improve error rates in severe AC line environments. Typically, errors occur due to pulse jitter in the LM2893/2893 data output that originates when the internal time domain filter smooths out an incoming noise pulse.

The solution involves removing the impulse completely and not simply trying to filter it. Moreover, the pulse should be removed in the receive signal path before the selective portions of the circuit to eliminate ringing. This also allows the receiver filter to smooth out the blanks that also occur in the desired incoming carrier signal.

If a carrier detect circuit is desired in conjunction with the LM2893 it can be located after the filter and impulse blanker. Because impulse noise is removed, the false triggering that plagues these circuits will be greatly reduced.

Simplified Schematic



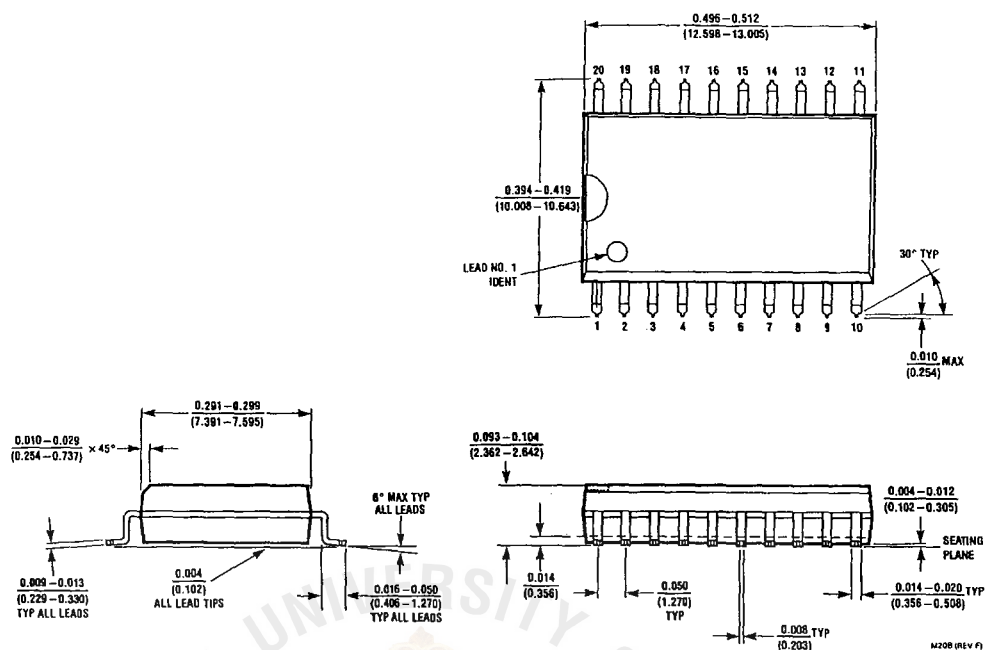
TL/H/6750-37

References

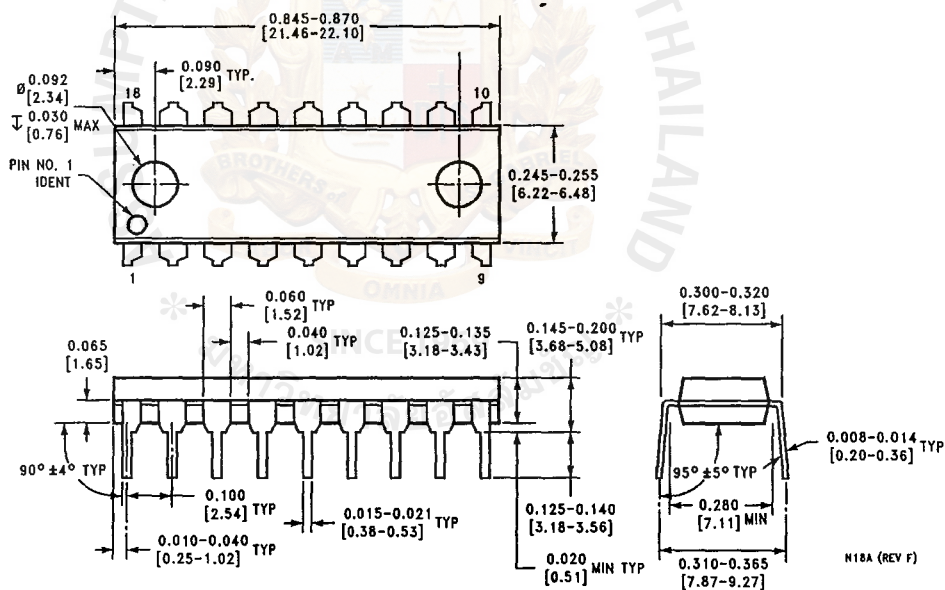
1. Nicholson, J.R. and J.A. Malack; "RF Impedance of Power Lines and Line Impedance Stabilization Network in Conducted Interference Measurements;" IEEE Transactions on Electromagnetic Compatibility; May 1973; (line impedance data)
2. Southwick, R.A.; "Impedance Characteristics of Single-Phase Power Lines;" Conference Rec.; 1973 IEEE Int. Symp. on Electromagnetic Compatibility; (line impedance data)
3. Hayt, William H. Jr. and Jack E. Kemmerly; "Engineering Circuit Analysis;" McGraw-Hill Books; 1971; pp. 447-453; (linear transformer reflected impedance)
4. FCC, "Notice of Proposed Rule Making," Docket 20780, adopted Apr. 14, 1976, (Proposed regulation)
5. Monticelli, Dennis M. and Michael E. Wright; "A Carrier Current Transceiver IC for Data Transmission Over the AC Power Lines;" IEEE J. Solid-State Circuits; vol. SC-17; Dec. 1982; pp. 1158-1165; (LM1893 circuit description)
6. Lee, Mitchell; "A New Carrier Current Transceiver IC;" IEEE Trans. on Consumer Electronics; vol. CE-28; Aug. 1982; pp. 409-414; (Application of LM1893)



Physical Dimensions inches (millimeters)



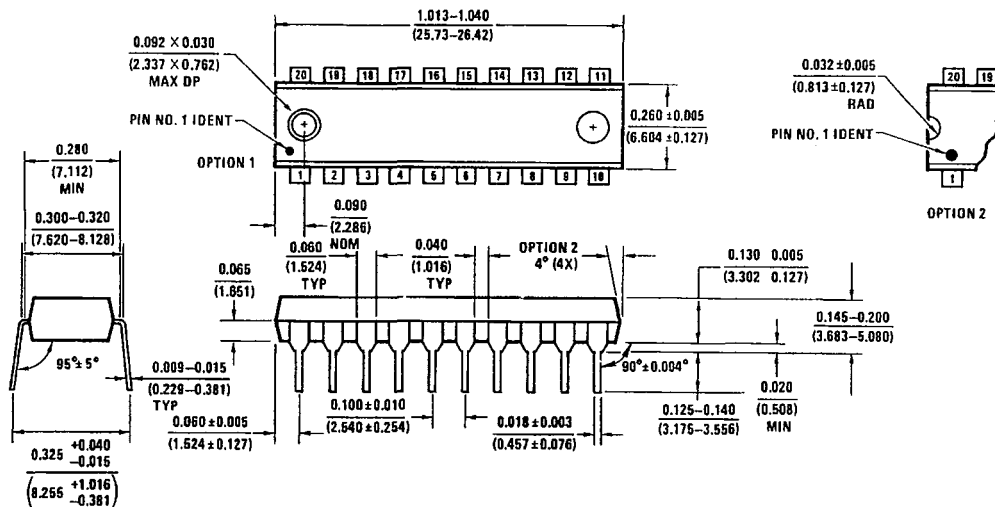
Molded Small Outline Package (M)
Order Part LM2893M
NS Package Number M20B



Molded Dual-In-Line Package (N)
Order Part LM1893N
NS Package Number N18A

Physical Dimensions inches (millimeters) (Continued)

Lit. # 107664



N20A (REV G)

Molded Dual-In-Line Package (N)
Order Part LM2893N
NS Package Number N20A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor
Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor
Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch: Tel: (+49) 0-180-530 85 85
English: Tel: (+49) 0-180-532 78 32
Français: Tel: (+49) 0-180-532 93 58
Italiano: Tel: (+49) 0-180-534 16 80

National Semiconductor
Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor
Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.

4-Digit LED Display, Programmable Up/Down Counter

August 1997

Features

- Four Decade, Presetable Up-Down Counter with Parallel Zero Detect
- Settable Register with Contents Continuously Compared to Counter
- Directly Drives Multiplexed 7 Segment Common Anode or Common Cathode LED Displays
- On-Board Multiplex Scan Oscillator
- Schmitt Trigger On Count Input
- TTL Compatible BCD I/O Port, Carry/Borrow, Equal, and Zero Outputs
- Display Blank Control for Lower Power Operation; Quiescent Power Dissipation <5mW
- All Terminals Fully Protected Against Static Discharge
- Single 5V Supply Operation

Description

The ICM7217 is a four digit, presetable up/down counter with an onboard presetable register continuously compared to the counter. The ICM7217 is intended for use in hard-wired applications where thumbwheel switches are used for loading data, and simple SPDT switches are used for chip control.

This circuit provides multiplexed 7 segment LED display outputs, with common anode or common cathode configurations available. Digit and segment drivers are provided to directly drive displays of up to 0.8 inch character height (common anode) at a 25% duty cycle. The frequency of the onboard multiplex oscillator may be controlled with a single capacitor, or the oscillator may be allowed to free run. Leading zeros can be blanked. The data appearing at the 7 segment and BCD outputs is latched; the content of the counter is transferred into the latches under external control by means of the Store pin.

The ICM7217 (common anode) and ICM7217A (common cathode) versions are decade counters, providing a maximum count of 9999, while the ICM7217B (common anode) and ICM7217C (common cathode) are intended for timing purposes, providing a maximum count of 5959.

This circuit provides 3 main outputs; a CARRY/BORROW output, which allows for direct cascading of counters, a ZERO output, which indicates when the count is zero, and an EQUAL output, which indicates when the count is equal to the value contained in the register. Data is multiplexed to and from the device by means of a three-state BCD I/O port. The CARRY/BORROW, EQUAL, ZERO outputs, and the BCD port will each drive one standard TTL load.

To permit operation in noisy environments and to prevent multiple triggering with slowly changing inputs, the count input is provided with a Schmitt trigger.

Input frequency is guaranteed to 2MHz, although the device will typically run with f_{IN} as high as 5MHz. Counting and comparing (EQUAL output) will typically run 750kHz maximum.

Ordering Information

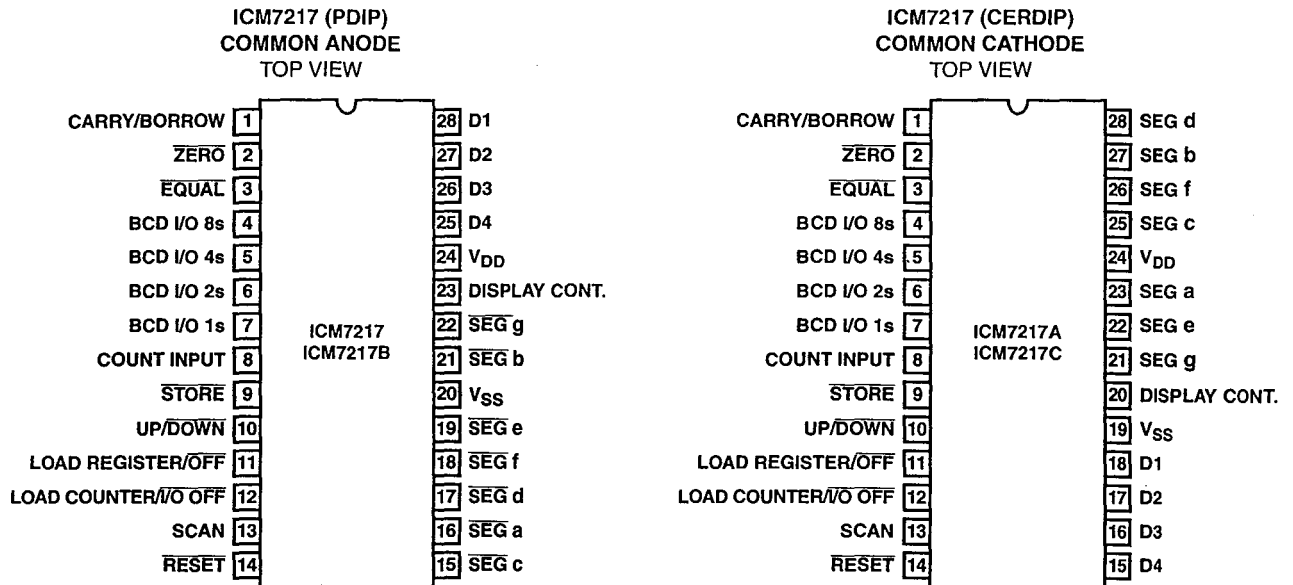
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	DISPLAY DRIVER TYPE	COUNT OPTION/ MAX COUNT	PKG. NO.
ICM7217AIP1	-25 to 85	28 Ld PDIP	Common Cathode	Decade/9999	E28.6
ICM7217CIP1	-25 to 85	28 Ld PDIP	Common Cathode	Timing/5959	E28.6
ICM7217IJ1	-25 to 85	28 Ld CERDIP	Common Anode	Decade/9999	F28.6
ICM7217BIJ1	-25 to 85	28 Ld CERDIP	Common Anode	Timing/5959	F28.6

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

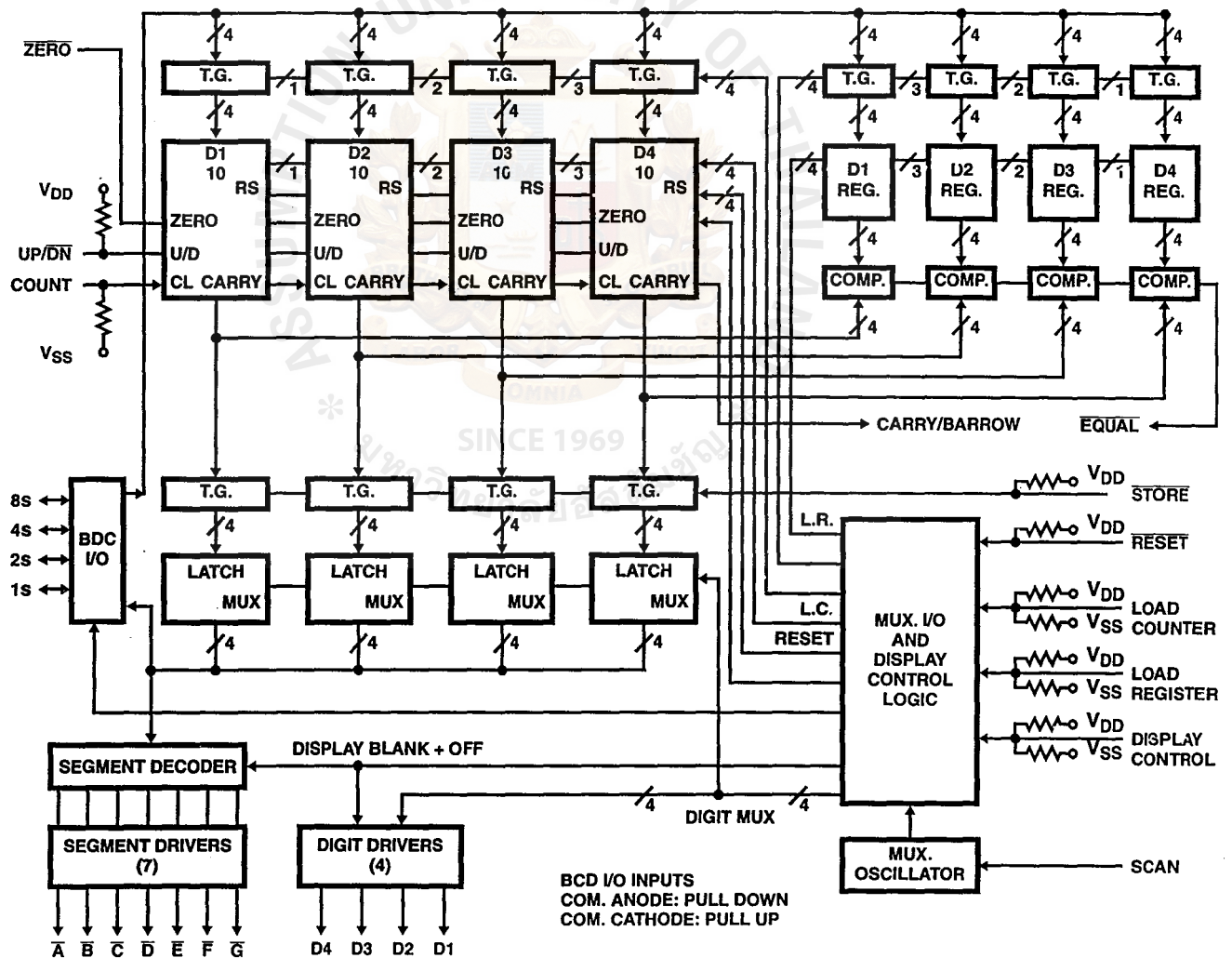
Copyright © Harris Corporation 1997

File Number **3167.1**

Pinouts



Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage ($V_{DD} - V_{SS}$) 6V
 Input Voltage (Any Terminal) ($V_{SS} - 0.3V$) to ($V_{DD} + 0.3V$)
 (Note 1)

Operating Conditions

Temperature Range -25°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W) θ_{JC} (°C/W)
 Cerdip Package 55 14
 PDIP Package 55 N/A
 Maximum Junction Temperature
 PDIP Package 150°C
 Cerdip Package 175°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering, 10s) 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

- Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason it is recommended that the power supply to the device be established before any inputs are applied and that in multiple systems the supply to the ICM7217 be turned on first.
- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{DD} = 5V$, $V_{SS} = 0V$, $T_A = 25^\circ C$, Display Diode Drop 1.7V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current (Lowest Power Mode), I_{DD} (7217)	Display Off, LC, DC, UP/DN, ST, RS, BCD I/O Floating or at V_{DD} (Note 1)	-	350	500	μA
Supply Current, OPERATING, I_{OP}	Common Anode, Display On, all "8's"	140	200	-	mA
Supply Current, OPERATING, I_{OP}	Common Cathode, Display On, all "8's"	50	100	-	mA
V_{SUPPLY} , V_{DD}		4.5	5	5.5	V
Digit Driver Output Current, I_{DIG}	Common Anode, $V_{OUT} = V_{DD} - 2.0V$	140	200	-	mA _{PEAK}
SEGment Driver Output Current, I_{SEG}	Common Anode, $V_{OUT} = +1.5V$	20	35	-	mA _{PEAK}
Digit Driver, Output Current, I_{DIG}	Common Cathode, $V_{OUT} = +1.0V$	-50	-75	-	mA _{PEAK}
SEGment Driver Output Current, I_{SEG}	Common Cathode $V_{OUT} = V_{DD} - 2V$	-9	-12.5	-	mA _{PEAK}
ST, RS, UP/DN Input Pullup Current, I_P	$V_{IN} = V_{DD} - 2V$ (Note 1)	5	25	-	μA
3 Level Input Impedance, Z_{IN}		40	-	350	k Ω
BCD I/O Input, High Voltage VBIH	ICM7217 Common Anode (Note 2)	1.5	-	-	V
	ICM7217 Common Cathode (Note 2)	4.40	-	-	V
BCD I/O Input, Low Voltage VBIL	ICM7217 Common Anode (Note 2)	-	-	0.60	V
	ICM7217 Common Cathode (Note 2)	-	-	3.2V	V
BCD I/O Input, Pullup Current IBPU	ICM7217 Common Cathode $V_{IN} = V_{DD} - 2V$ (Note 2)	5	25	-	μA
BCD I/O Input Pulldown Current, IBPD	ICM7217 Common Anode $V_{IN} = +2V$ (Note 2)	5	25	-	μA
BCD I/O, ZERO, EQUAL Outputs Output High Voltage, V _{OH}	$I_{OH} = -100\mu A$	3.5	-	-	V
BCD I/O, CARRY/BORROW ZERO, EQUAL Outputs Output Low Voltage, V _{OL}	$I_{OL} = 1.6mA$	-	-	0.4	V
Count Input Frequency, f_{IN}	-20°C to 70°C	-	5	-	MHz
	Guaranteed	0	-	2	MHz
Count Input Threshold, V _{TH}	(Note 3)	-	2	-	V
Count Input Hysteresis, V _{HYS}	(Note 3)	-	0.5	-	V
Count Input LO, VCIL		-	-	0.40	V
Count Input HI, VCIH		3.5	-	-	V
Display Scan Oscillator Frequency, f_{DS}	Free-running (SCAN Terminal Open Circuit)	-	2.5	10	kHz

Switching Specifications $V_{DD} = 5V$, $V_{SS} = 0V$, $T_A = 25^\circ C$

PARAMETER	MIN	TYP	MAX	UNIT
UP/DOWN Setup Time, t_{UCS}	300	-	-	ns
UP/DOWN Hold Time, t_{UCH}	1500	750	-	ns
COUNT Pulse Width High, t_{CWH}	250	100	-	ns
COUNT Pulse Width Low, t_{CWL}	250	100	-	ns
COUNT to CARRY/BORROW Delay, t_{CB}	-	750	-	ns
CARRY/BORROW Pulse Width t_{BW}	-	100	-	ns
COUNT to \overline{EQUAL} Delay, t_{CE}	-	500	-	ns
COUNT to \overline{ZERO} Delay, t_{CZ}	-	300	-	ns
RESET Pulse Width, t_{RST}	1000	500	-	ns

NOTES:

1. In the ICM7217 the UP/DOWN, STORE, RESET and the BCD I/O as inputs have pullup or pulldown devices which consume power when connected to the opposite supply. Under these conditions, with the display off, the device will consume typically 750 μA .
2. These voltages are adjusted to allow the use of thumbwheel switches for the ICM7217. Note that a high level is taken as an input logic zero for ICM7217 common-cathode versions.
3. Parameters not tested (Guaranteed by Design).

Timing Waveforms

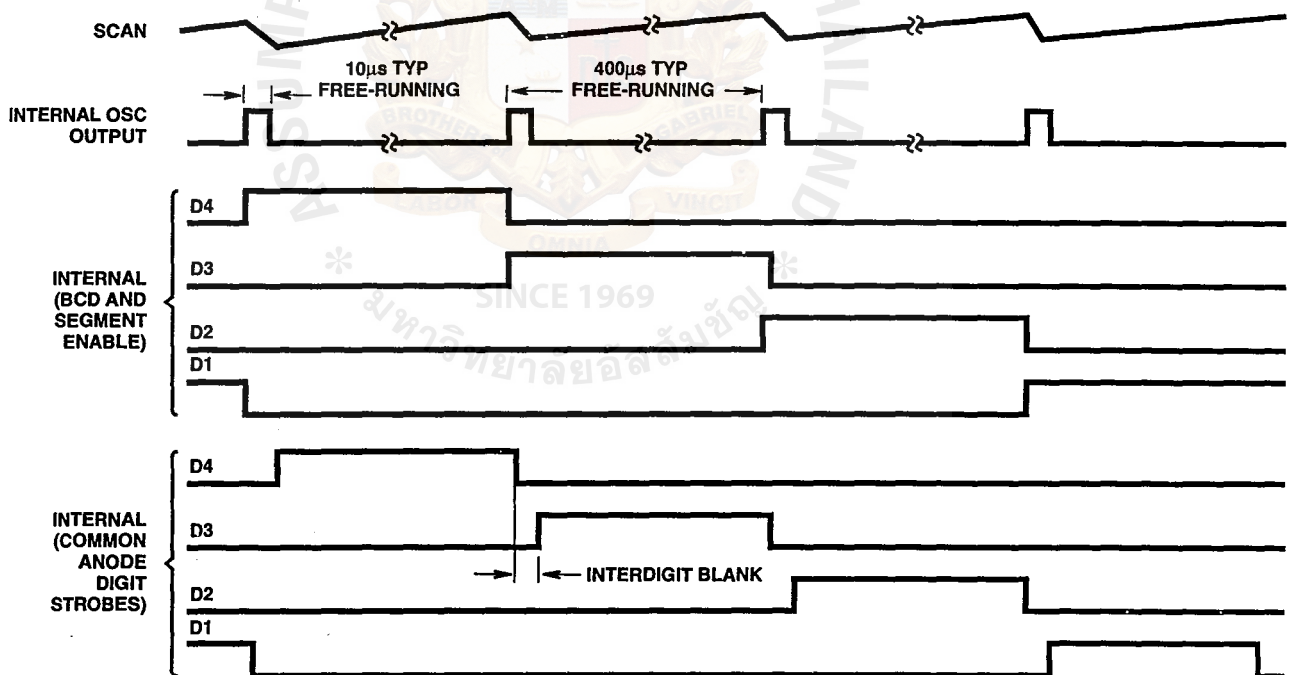


FIGURE 1. MULTIPLEX TIMING

Timing Waveforms

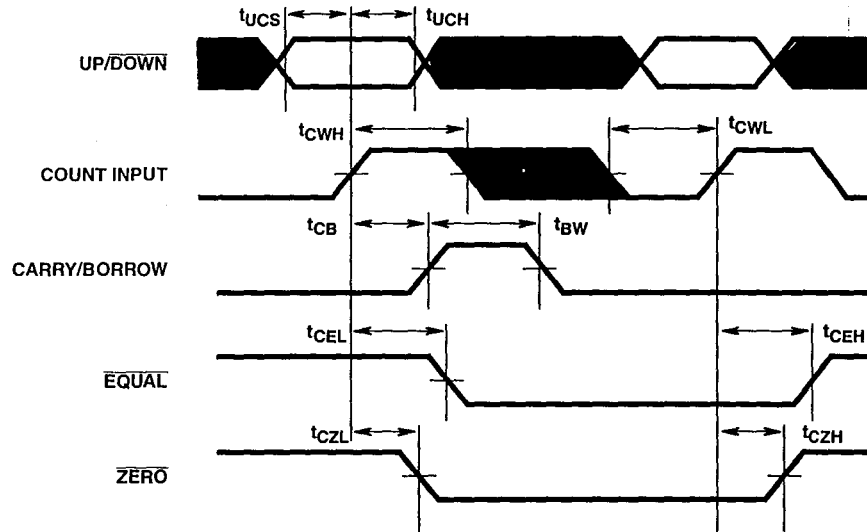


FIGURE 2. COUNT AND OUTPUTS TIMING

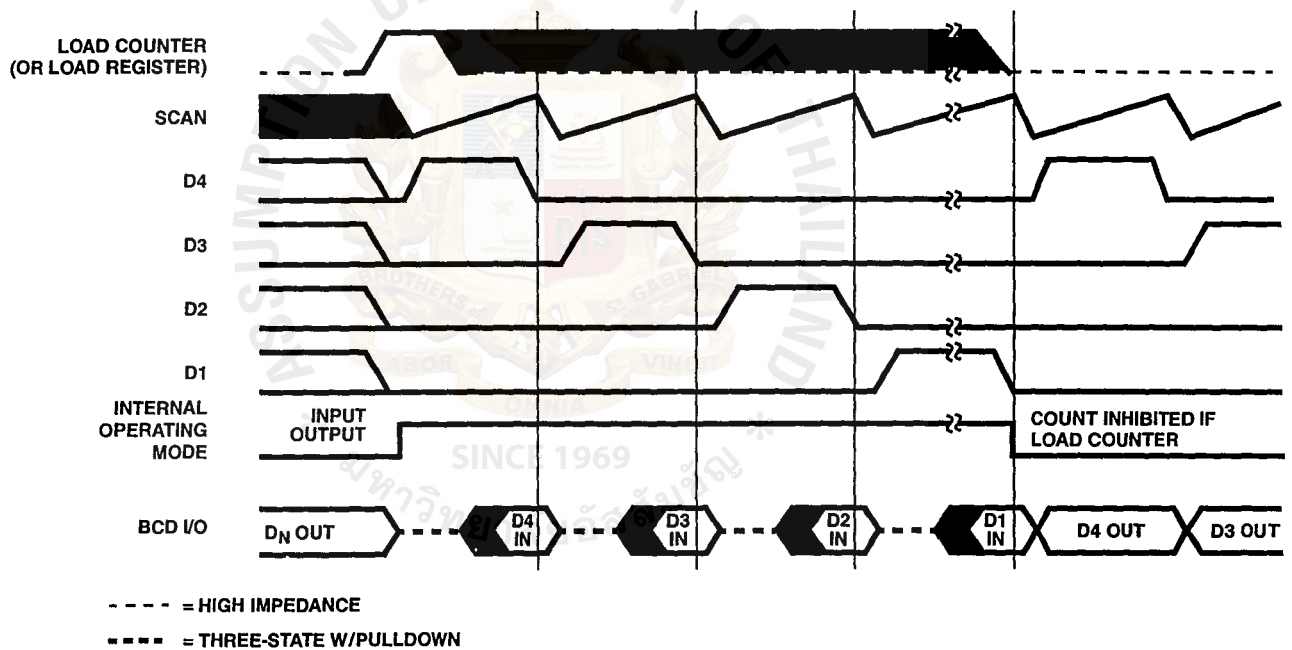


FIGURE 3. BCD I/O AND LOADING TIMING

Typical Performance Curves

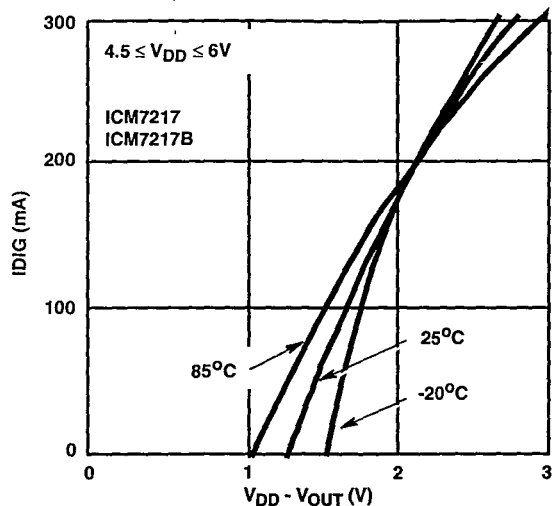


FIGURE 4. TYPICAL IDIG vs V_+

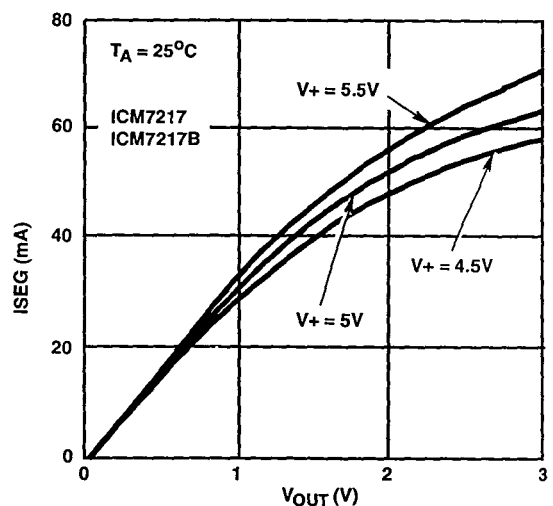


FIGURE 5. TYPICAL ISEG vs V_{OUT}

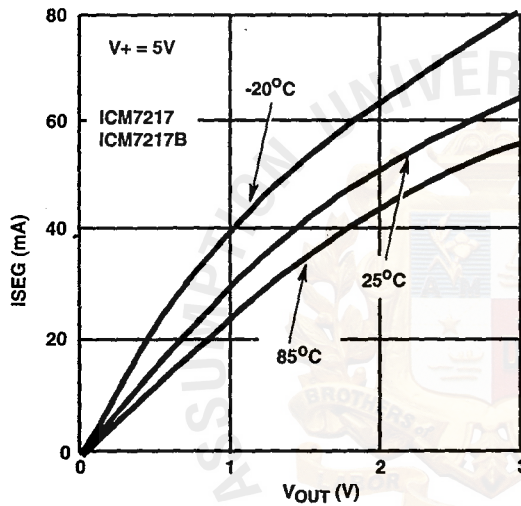


FIGURE 6. TYPICAL ISEG vs V_{OUT}

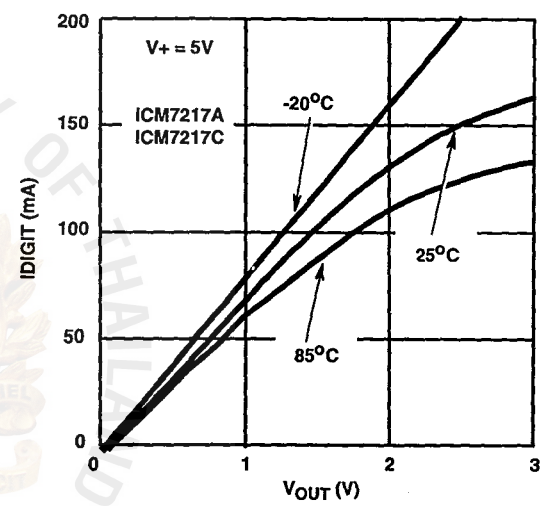


FIGURE 7. TYPICAL IDIGIT vs V_{OUT}

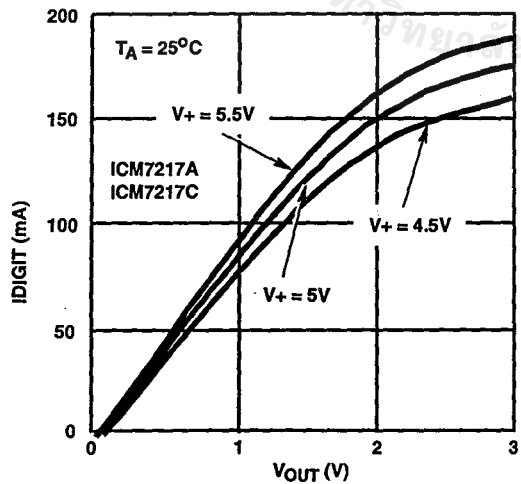


FIGURE 8. TYPICAL IDIGIT vs V_{OUT}

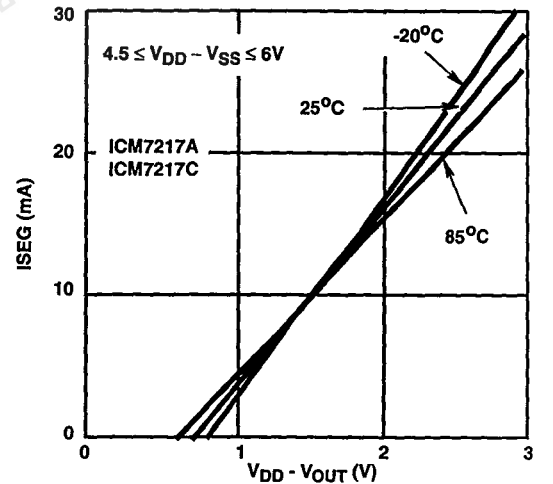


FIGURE 9. TYPICAL ISEG vs $V_{DD} - V_{OUT}$

Detailed Description

Control Outputs

The CARRY/BORROW output is a positive going pulse occurring typically 500ns after the positive going edge of the COUNT INPUT. It occurs when the counter is clocked from 9999 to 0000 when counting up and from 0000 to 9999 when counting down. This output allows direct cascading of counters. The CARRY/BORROW output is not valid during load counter and reset operation. When the count is 6000 or higher, a reset generates a CARRY/BORROW pulse.

The $\overline{\text{EQUAL}}$ output assumes a negative level when the contents of the counter and register are equal.

The $\overline{\text{ZERO}}$ output assumes a negative level when the content of the counter is 0000.

The CARRY/BORROW, $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs will drive a single TTL load over the full range of supply voltage and ambient temperature; for a logic zero, these outputs will sink 1.6mA at 0.4V and for a logic one, the outputs will source $>60\mu\text{A}$. A 10k Ω pull-up resistor to V_{DD} on the $\overline{\text{EQUAL}}$ or $\overline{\text{ZERO}}$ outputs is recommended for highest speed operation, and on the CARRY/BORROW output when it is being used for cascading. Figure 2 shows control outputs timing diagram.

Display Outputs and Control

The Digit and SEGment drivers provide a decoded 7-segment display system, capable of directly driving common anode LED displays at typical peak currents of 35mA/seg. This corresponds to average currents of 8mA/seg at 25% multiplex duty cycle. For the common cathode versions, peak segment currents are 12.5mA, corresponding to average segment currents of 3.1mA. Figure 1 shows the multiplex timing. The DISPLAY pin controls the display output using three level logic. The pin is self-biased to a voltage approximately $\frac{1}{2} (V_{DD})$; this corresponds to normal operation. When this pin is connected to V_{DD} , the segments are disabled and when connected to V_{SS} , the leading zero blanking feature is inhibited. For normal operation (display on with leading zero blanking) the pin should be left open. The display may be controlled with a 3 position SPDT switch; see Test Circuit.

Multiplex SCAN Oscillator

The on-board multiplex scan oscillator has a nominal free-running frequency of 2.5kHz. This may be reduced by the addition of a single capacitor between the SCAN pin and the positive supply. Capacitor values and corresponding nominal oscillator frequencies, digit repetition rates, and loading times are shown in Table 1.

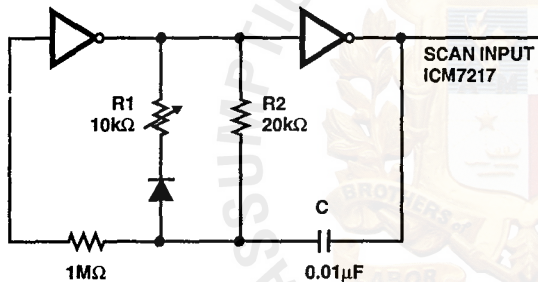


FIGURE 10A.

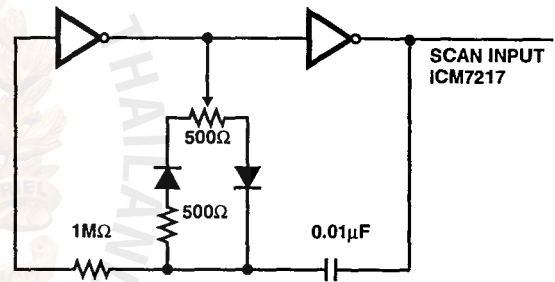


FIGURE 10B.

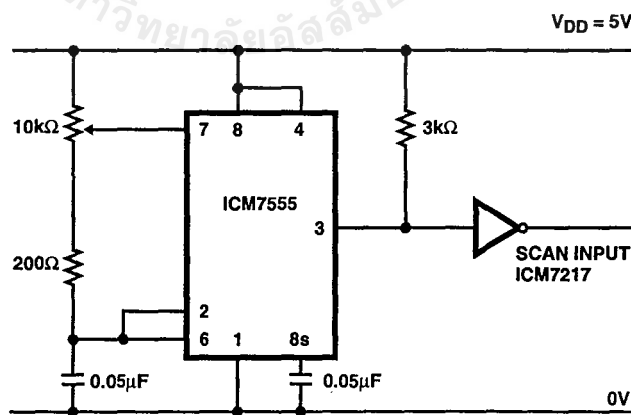


FIGURE 10C.

FIGURE 10. BRIGHTNESS CONTROL CIRCUITS

TABLE 1. ICM7217 MULTIPLEXED RATE CONTROL

SCAN CAPACITOR	NOMINAL OSCILLATOR FREQUENCY	DIGIT REPETITION RATE	SCAN CYCLE TIME (4 DIGITS)
None	2.5kHz	625Hz	1.6ms
20pF	1.25kHz	300Hz	3.2ms
90pF	600Hz	150Hz	8ms

The internal oscillator output has a duty cycle of approximately 25:1, providing a short pulse occurring at the oscillator frequency. This pulse clocks the four-state counter which provides the four multiplex phases. The short pulse width is used to delay the digit driver outputs, thereby providing inter-digit blanking which prevents ghosting. The digits are scanned from MSD (D4) to LSD (D1). See Figure 1 for the display digit multiplex timing.

During load counter and load register operations, the multiplex oscillator is disconnected from the SCAN input and is allowed to free-run. In all other conditions, the oscillator may be directly overdriven to about 20kHz, however the external oscillator signal should have the same duty cycle as the internal signal, since the digits are blanked during the time the external signal is at a positive level (see Figure 1). To insure proper leading zero blanking, the interdigit blanking time should not be less than about 2 μ s. Overdriving the oscillator at less than 200Hz may cause display flickering.

The display brightness may be altered by varying the duty cycle. Figure 10 shows several variable-duty-cycle oscillators suitable for brightness control at the ICM7217 SCAN input. The inverters should be CMOS CD4000 series and the diodes may be any inexpensive device such as IN914.

Counting Control, **STORE**, **RESET**

As shown in Figure 2, the counter is incremented by the rising edge of the COUNT INPUT signal when UP/DOWN is high. It is decremented when UP/DOWN is low. A Schmitt trigger on the COUNT INPUT provides hysteresis to prevent double triggering on slow rising edges and permits operation in noisy environments. The COUNT INPUT is inhibited during reset and load counter operations.

The **STORE** pin controls the internal latches and consequently the signals appearing at the 7-Segment and BCD outputs. Bringing the **STORE** pin low transfers the contents of the counter into the latches.

The counter is asynchronously reset to 0000 by bringing the **RESET** pin low. The circuit performs the reset operation by forcing the BCD input lines to zero, and "presetting" all four decades of counter in parallel. This affects register loading; if LOAD REGISTER is activated when the **RESET** input is low, the register will also be set to zero. The **STORE**, **RESET** and UP/DOWN pins are provided with pullup resistors of approximately 75k Ω .

BCD I/O Pins

The BCD I/O port provides a means of transferring data to and from the device. The ICM7217 versions can multiplex data into the counter or register via thumbwheel switches,

depending on inputs to the LOAD COUNTER or LOAD REGISTER pins; (see below). When functioning as outputs, the BCD I/O pins will drive one standard TTL load. Common anode versions have internal pull down resistors and common cathode versions have internal pull up resistors on the four BCD I/O lines when used as inputs.

LOADing the COUNTER and REGISTER

The BCD I/O pins, the LOAD COUNTER (LC), and LOAD REGISTER (LR) pins combine to provide presetting and compare functions. LC and LR are 3-level inputs, being self-biased at approximately $\frac{1}{2}V_{DD}$ for normal operation. With both LC and LR open, the BCD I/O pins provide a multiplexed BCD output of the latch contents, scanned from MSD to LSD by the display multiplex.

When either the LOAD COUNTER (Pin 12) or LOAD REGISTER (Pin 11) is taken low, the drivers are turned off and the BCD pins become high-impedance inputs. When LC is connected to V_{DD} , the count input is inhibited and the levels at the BCD pins are multiplexed into the counter. When LR is connected to V_{DD} , the levels at the BCD pins are multiplexed into the register without disturbing the counter. When both are connected to V_{DD} , the count is inhibited and both register and counter will be loaded.

The LOAD COUNTER and LOAD REGISTER inputs are edge-triggered, and pulsing them high for 500ns at room temperature will initiate a full sequence of data entry cycle operations (see Figure 3). When the circuit recognizes that either or both of the LC or LR pins input is high, the multiplex oscillator and counter are reset (to D4). The internal oscillator is then disconnected from the SCAN pin and the preset circuitry is enabled. The oscillator starts and runs with a frequency determined by its internal capacitor, (which may vary from chip to chip). When the chip finishes a full 4-digit multiplex cycle (loading each digit from D4 to D3 to D2 to D1 in turn), it again samples the LOAD REGISTER and LOAD COUNTER inputs. If either or both is still high, it repeats the load cycle, if both are floating or low, the oscillator is reconnected to the SCAN pin and the chip returns to normal operation. Total load time is digit "on" time multiplied by 4. If the Digit outputs are used to strobe the BCD data into the BCD I/O inputs, the input must be synchronized to the appropriate digit (Figure 3). Input data must be valid at the trailing edge of the digit output.

When LR is connected to GROUND, the oscillator is inhibited, the BCD I/O pins go to the high impedance state, and the segment and digit drivers are turned off. This allows the display to be used for other purposes and minimizes power consumption. In this display off condition, the circuit will continue to count, and the CARRY/BORROW, EQUAL, ZERO, UP/DOWN, RESET and STORE functions operate as normal. When LC is connected to ground, the BCD I/O pins are forced to the high impedance state without disturbing the counter or register. See "Control Input Definitions" (Table 2) for a list of the pins that function as three-state self-biased inputs and their respective operations.

Note that the ICM7217 and ICM7217B have been designed to drive common anode displays. The BCD inputs are high true, as are the BCD outputs.

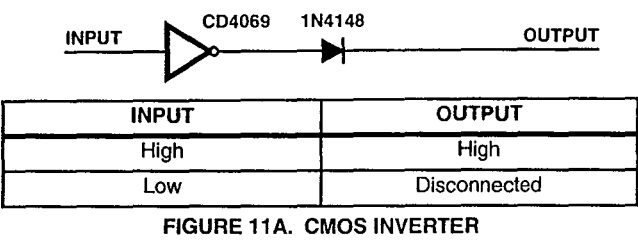


FIGURE 11A. CMOS INVERTER

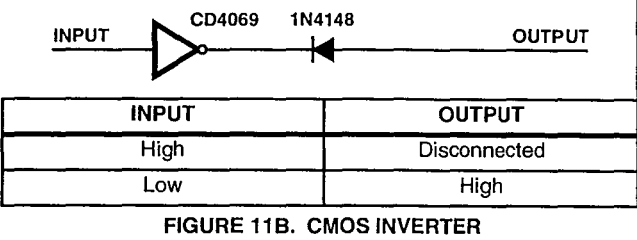


FIGURE 11B. CMOS INVERTER

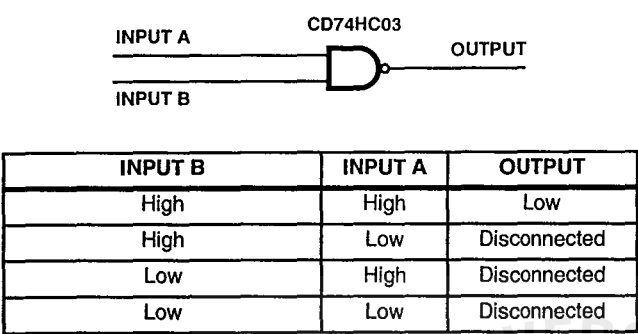


FIGURE 11C. CMOS OPEN DRAIN

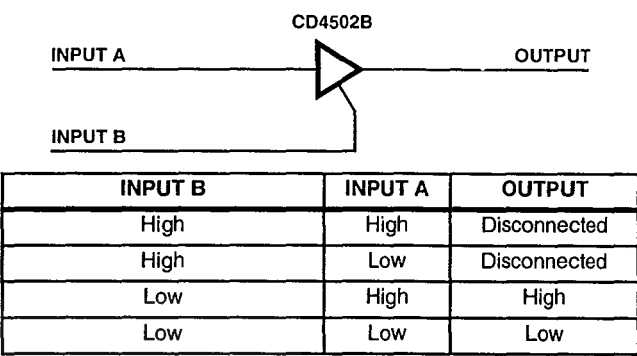


FIGURE 11D. CMOS THREE-STATE BUFFER

FIGURE 11. DRIVING 3-LEVEL INPUTS OF ICM7217

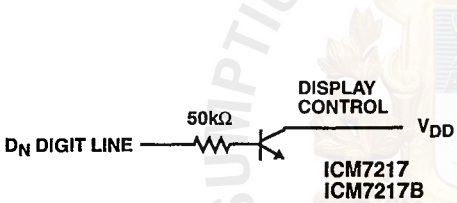


FIGURE 12A. COMMON ANODE

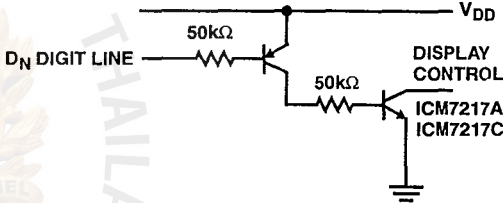


FIGURE 12B. COMMON CATHODE

FIGURE 12. FORCING LEADING ZERO DISPLAY

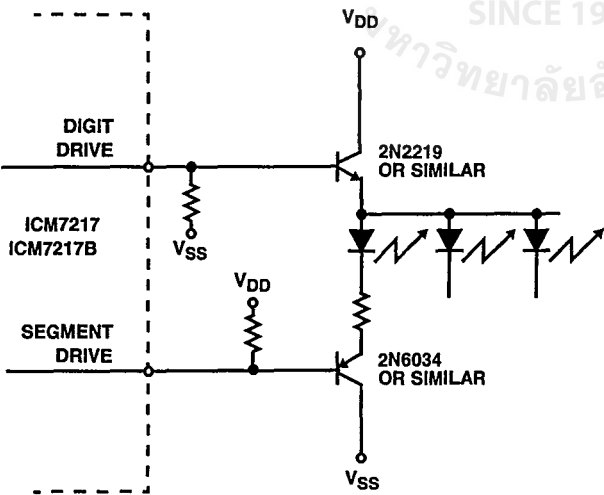


FIGURE 13A. COMMON ANODE DISPLAY

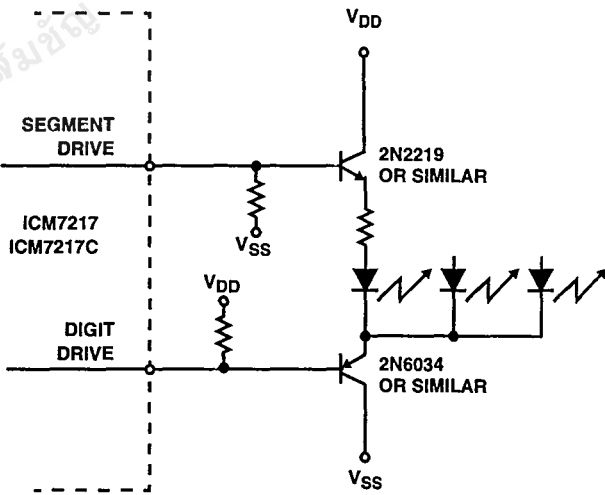


FIGURE 13B. COMMON CATHODE DISPLAY

FIGURE 13. DRIVING HIGH CURRENT DISPLAYS

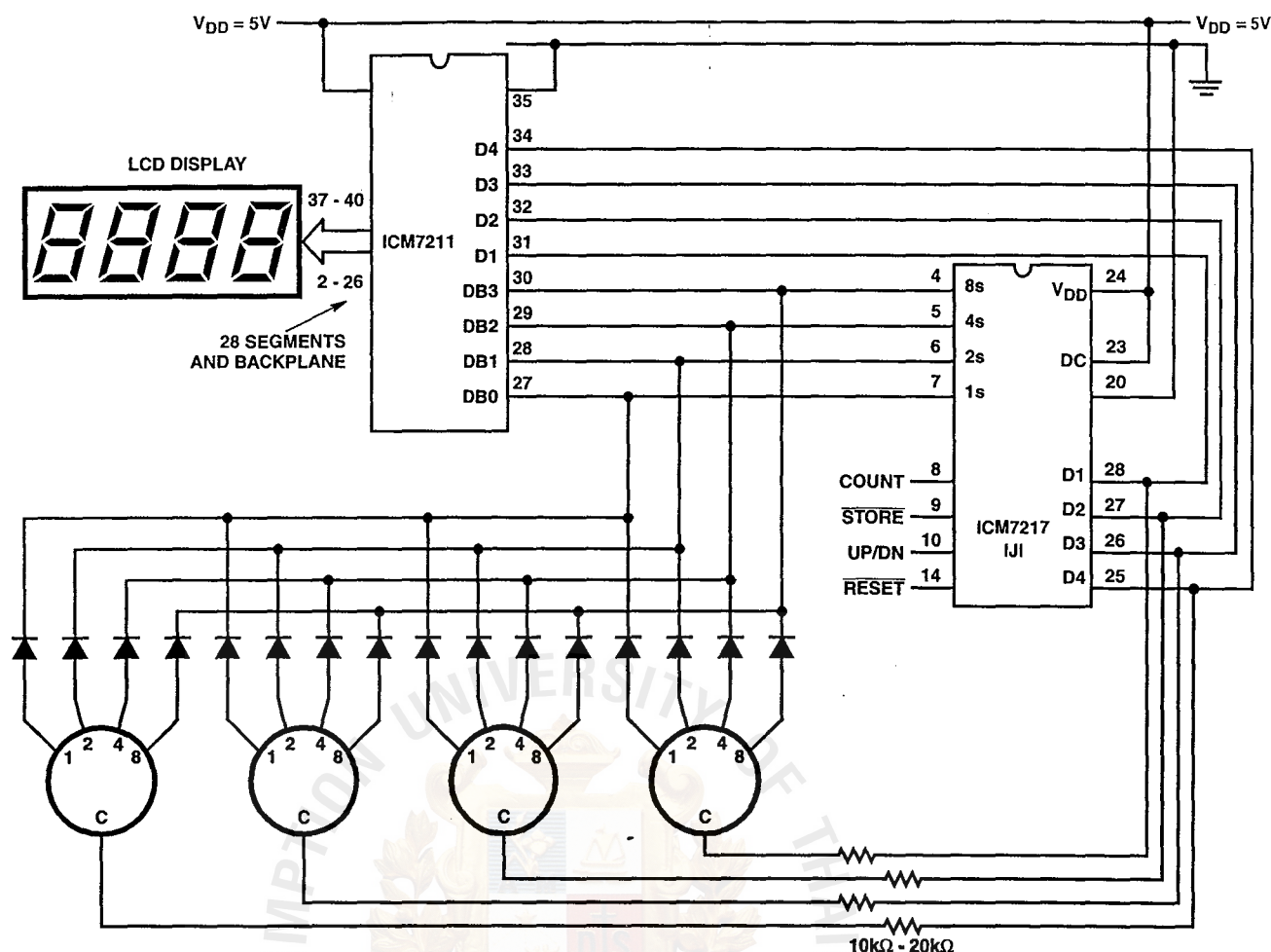


FIGURE 14. LCD DISPLAY INTERFACE (WITH THUMBWHEEL SWITCHES)

The ICM7217A and the ICM7217C are used to drive common cathode displays, and the BCD inputs are low true. BCD outputs are high true.

Notes on Thumbwheel Switches and Multiplexing

As it was mentioned, the ICM7217 is basically designed to be used with thumbwheel switches for loading the data to the device. See Figure 14 and Figure 17.

The thumbwheel switches used with these circuits (both common anode and common cathode) are TRUE BCD coded; i.e. all switches open corresponds to 0000. Since the thumbwheel switches are connected in parallel, diodes must be provided to prevent crosstalk between digits. In order to maintain reasonable noise margins, these diodes should be specified with low forward voltage drops (IN914). Similarly, if the BCD outputs are to be used, resistors should be inserted in the Digit lines to avoid loading problems.

Output and Input Restrictions

LOAD COUNTER and LOAD REGISTER operations take 1.6ms typical (5ms maximum) after LC or LR are released. During this load period the EQUAL and ZERO outputs are not valid (see Figure 3). Since the Counter and register are compared by XOR gates, loading the counter or register can

cause erroneous glitches on the EQUAL and ZERO outputs when codes cross.

LOAD COUNTER or LOAD REGISTER, and RESET input can not be activated at the same time or within a short period of each other. Operation of each input must be delayed 1.6ms typical (5ms for guaranteed proper operation) relating to the preceding one.

Counter and register can be loaded together with the same value if LC and LR inputs become activated exactly at the same time.

Notice the setup and hold time of UP/DOWN input when it is changing during counting operation. Violation of UP/ DOWN hold time will result in incrementing or decrementing the counter by 1000, 100 or 10 where the preceding digit is transitioning from 5 to 6 or 6 to 5.

The RESET input may be susceptible to noise if its input rise time is greater than about 500μs. This will present no problems when this input is driven by active devices (i.e., TTL or CMOS logic) but in hardwired systems adding virtually any capacitance to the RESET input can cause trouble. A simple circuit which provides a reliable power-up reset and a fast rise time on the RESET input is shown on Figure 15.

When using the circuit as a programmable divider (\div by n with equal outputs) a short time delay (about $1\mu s$) is needed from the $\overline{\text{EQUAL}}$ output to the $\overline{\text{RESET}}$ input to establish a pulse of adequate duration. (See Figure 16).

When the circuit is configured to reload the counter or register with a new value from the BCD lines (upon reaching $\overline{\text{EQUAL}}$), loading time will be digit "on" time multiplied by four. If this load time is longer than one period of the input count, a count can be lost. Since the circuit will retain data in the register, the register need only be updated when a new value is to be entered. $\overline{\text{RESET}}$ will not clear the register.

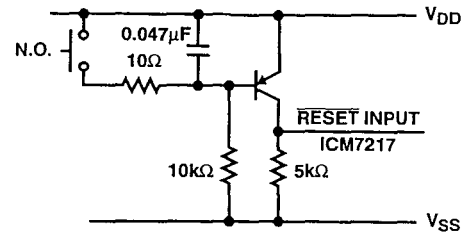


FIGURE 15. POWER ON RESET

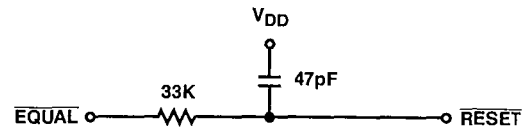
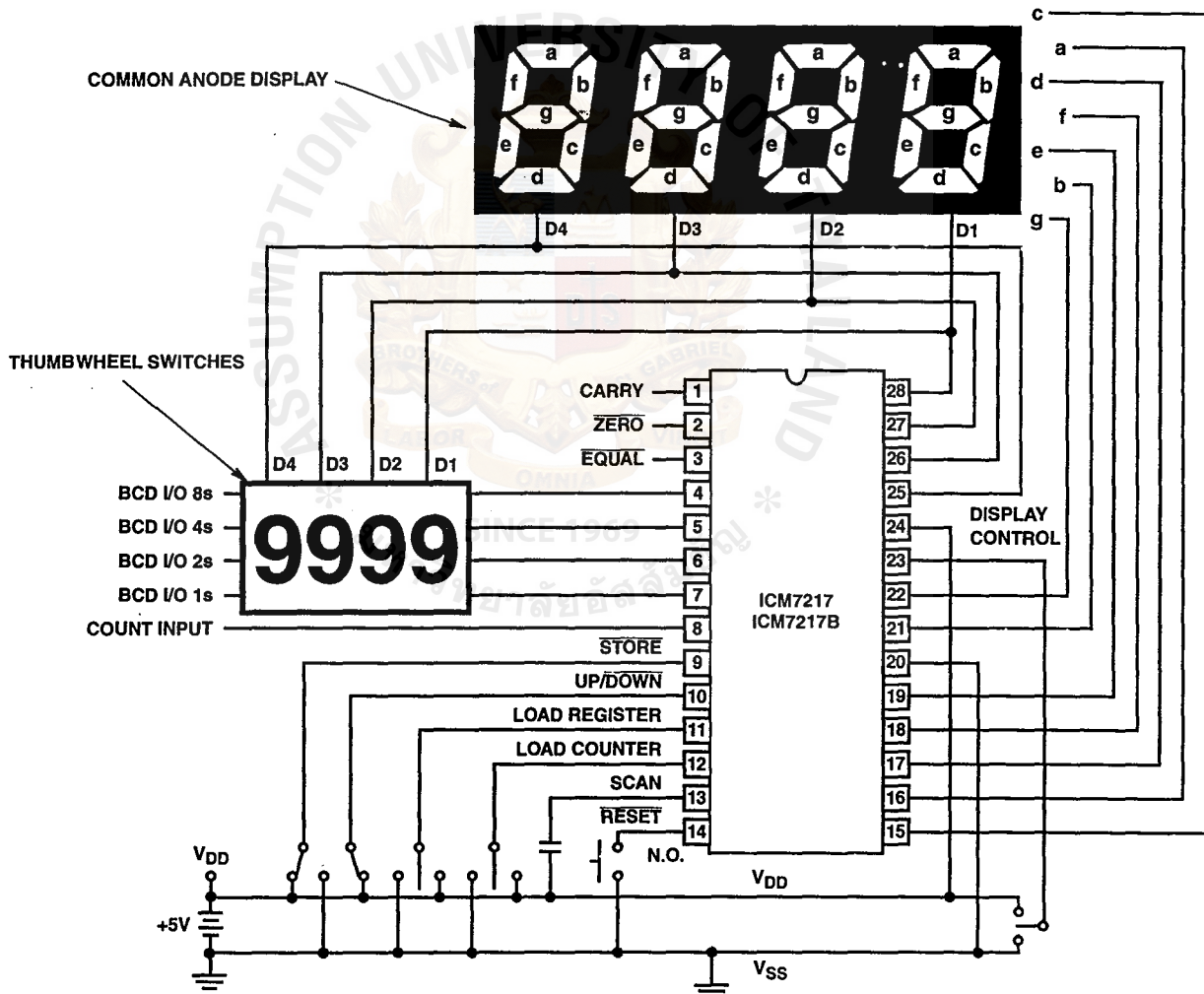


FIGURE 16. EQUAL TO RESET DELAY

Test Circuit



Applications

3-Level Inputs

ICM7217 has three inputs with 3-level logic states; High, Low and Disconnected. These inputs are: LOAD REGISTER/OFF, LOAD COUNTER/I/O OFF and DISPLAY CONT.

The circuits illustrated on Figure 11 can be used to drive these inputs in different applications.

Fixed Decimal Point

In the common anode versions, a fixed decimal point may be activated by connecting the DP segment lead from the appropriate digit (with separate digit displays) through a 39 Ω series resistor to Ground. With common cathode devices, the DP segment lead should be connected through a 75 Ω series resistor to V_{DD} .

To force the device to display leading zeroes after a fixed decimal point, use a bipolar transistor and base resistor in a configuration like that shown in Figure 12 with the resistor connected to the digit output driving the DP for left hand DP displays, and to the next least significant digit output for right hand DP display.

Driving Larger Displays

For displays requiring more current than the ICM7217 can provide, the circuits of Figure 13 can be used.

LCD Display Interface

The low-power operation of the ICM7217 makes an LCD interface desirable. The Harris ICM7211 4-digit, BCD-to-LCD display driver easily interfaces to the ICM7217 as shown in Figure 14. Total system power consumption is less than 5mW. System timing margins can be improved by using capacitance to ground to slow down the BCD lines.

The 10k Ω - 20k Ω resistors on the switch BCD lines serve to isolate the switches during BCD output.

Unit Counter with BCD Output

The simplest application of the ICM7217 is a 4-digit unit counter (Figure 18). All that is required is an ICM7217, a power supply and a 4 digit display. Add a momentary switch for reset, an SPDT center-off switch to blank the display or view leading zeroes, and one more SPDT switch for up/down control. Using an ICM7217A with a common-cathode calculator-type display results in the least expensive digital counter/display system available.

Inexpensive Frequency Counter/ Tachometer

This circuit uses the low power ICM7555 (CMOS 555) to generate the gating, STORE and RESET signals as shown in Figure 19. To provide the gating signal, the timer is configured as an a stable multivibrator, using R_A , R_B and C to provide an output that is positive for approximately one second and negative for approximately 300 μ s - 500 μ s. The positive waveform time is given by $t_{WP} = 0.693 (R_A + R_B)C$ while the negative waveform is given by $t_{WN} = 0.693 R_B C$. The system is calibrated by using a 5M Ω potentiometer for R_A as a "coarse" control and a 1k Ω potentiometer for R_B as

a "fine" control. CD40106Bs are used as a monostable multivibrator and reset time delay.

Tape Recorder Position Indicator/controller

The circuit in Figure 20 shows an application which uses the up/down counting feature of the ICM7217 to keep track of tape position. This circuit is representative of the many applications of up/down counting in monitoring dimensional position.

In the tape recorder application, the LOAD REGISTER, EQUAL and ZERO outputs are used to control the recorder. To make the recorder stop at a particular point on the tape, the register can be set with the stop point and the EQUAL output used to stop the recorder either on fast forward, play or rewind.

To make the recorder stop before the tape comes free of the reel on rewind, a leader should be used. Resetting the counter at the starting point of the tape, a few feet from the end of the leader, allows the ZERO output to be used to stop the recorder on rewind, leaving the leader on the reel.

The 1M Ω resistor and 0.0047 μ F capacitor on the COUNT INPUT provide a time constant of about 5ms to debounce the reel switch. The Schmitt trigger on the COUNT INPUT of the ICM7217 squares up the signal before applying it to the counter. This technique may be used to debounce switch-closure inputs in other applications.

Precision Elapsed Time/Countdown Timer

The circuit in Figure 21 uses an ICM7213 precision one minute/one second timebase generator using a 4.1943MHz crystal for generating pulses counted by an ICM7217B. The thumbwheel switches allow a starting time to be entered into the counter for a preset-countdown type timer, and allow the register to be set for compare functions. For instance, to make a 24-hour clock with BCD output the register can be preset with 2400 and the EQUAL output used to reset the counter. Note the 10K resistor connected between the LOAD COUNTER terminal and Ground. This resistor pulls the LOAD COUNTER input low when not loading, thereby inhibiting the BCD output drivers. This resistor should be eliminated and SW4 replaced with an SPDT center-off switch if the BCD outputs are to be used.

This technique may be used on any 3-level input. The 100k Ω pullup resistor on the count input is used to ensure proper logic voltage swing from the ICM7213. For a less expensive (and less accurate) timebase, an ICM7555 timer may be used in a configuration like that shown in Figure 19 to generate a 1Hz reference.

8-Digit Up/Down Counter

This circuit (Figure 22) shows how to cascade counters and retain correct leading zero blanking. The NAND gate detects whether a digit is active since one of the two segments \bar{a} or \bar{b} is active on any unblanked number. The flip flop is clocked by the least significant digit of the high order counter, and if this digit is not blanked, the Q output of the flip flop goes high and turns on the NPN transistor, thereby inhibiting leading zero blanking on the low order counter.

It is possible to use separate thumbwheel switches for presetting, but since the devices load data with the oscillator free-running, the multiplexing of the two devices is difficult to synchronize.

Precision Frequency Counter/Tachometer

The circuit shown in Figure 23 is a simple implementation of a four digit frequency counter, using an ICM7207A to provide the one second gating window and the STORE and RESET signals. In this configuration, the display reads hertz directly. With Pin 11 of the ICM7207A connected to V_{DD} , the gating time will be 0.1s; this will display tens of hertz at the least significant digit. For shorter gating times, an ICM7207 may be used (with a 6.5536MHz crystal), giving a 0.01s gating with Pin 11 connected to V_{DD} , and a 0.1s gating with Pin 11 open.

To implement a four digit tachometer, the ICM7207A with one second gating should be used. To get the display to read directly in RPM, the rotational frequency of the object to be

measured must be multiplied by 60. This can be done electronically using a phase-locked loop, or mechanically by using a disc rotating with the object with the appropriate number of holes drilled around its edge to interrupt the light from an LED to a photo-detector. For faster updating, use 0.1s gating, and multiply the rotational frequency by 600.

Auto-Tare System

This circuit uses the count-up and count-down functions of the ICM7217, controlled via the EQUAL and ZERO outputs, to count in SYNC with an ICL7109A and ICL7109D Converter as shown in Figure 24. By RESETing the ICM7217 on a "tare" value conversion, and STORE-ing the result of a true value conversion, an automatic fare subtraction occurs in the result.

The ICM7217 stays in step with the ICL7109 by counting up and down between 0 and 4095, for 8192 total counts, the same number as the ICL7109 cycle. See applications note No. A047 for more details.

TABLE 2. CONTROL INPUT DEFINITIONS ICM7217

INPUT	TERMINAL	VOLTAGE	FUNCTION
STORE	9	V_{DD} (or floating) V_{SS}	Output Latches Not Updated Output Latches Updated
UP/DOWN	10	V_{DD} (or floating) V_{SS}	Counter Counts Up Counter Counts Down
RESET	14	V_{DD} (or floating) V_{SS}	Normal Operation Counter Reset
LOAD COUNTER/ I/O OFF	12	Unconnected V_{DD} V_{SS}	Normal Operation Counter Loaded with BCD data BCD Port Forced to Hi-Z Condition
LOAD REGISTER/ OFF	11	Unconnected V_{DD} V_{SS}	Normal Operation Register Loaded with BCD Data Display Drivers Disabled; BCD Port Forced to Hi-Z Condition, mpx Counter Reset to D4; mpx Oscillator Inhibited
DISPLAY CONTROL	23 Common Anode 20 Common Cathode	Unconnected V_{DD} V_{SS}	Normal Operation Segment Drivers Disabled Leading Zero Blanking Inhibited

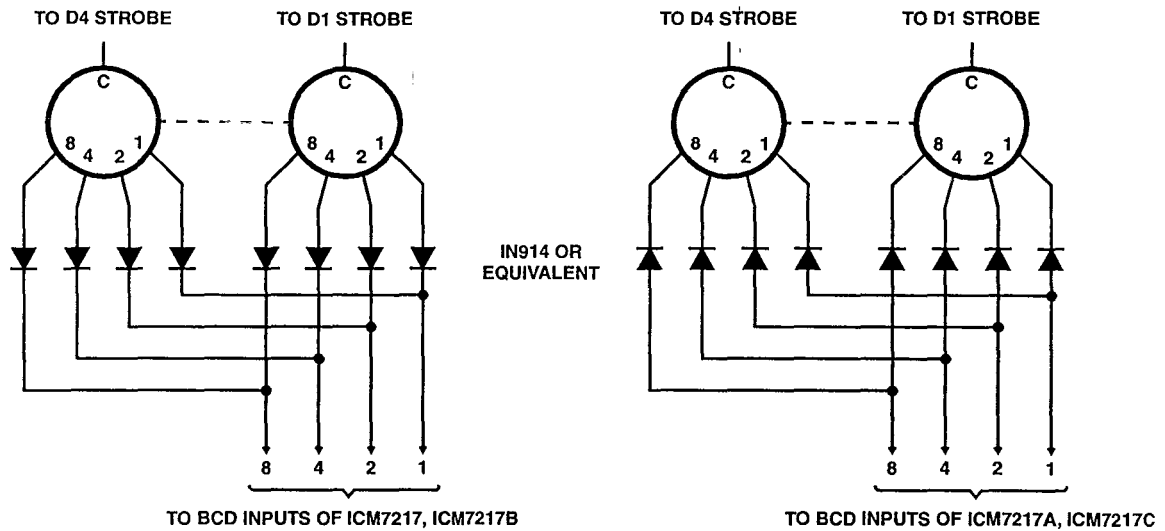


FIGURE 17. THUMBWHEEL SWITCH/DIODE CONNECTIONS

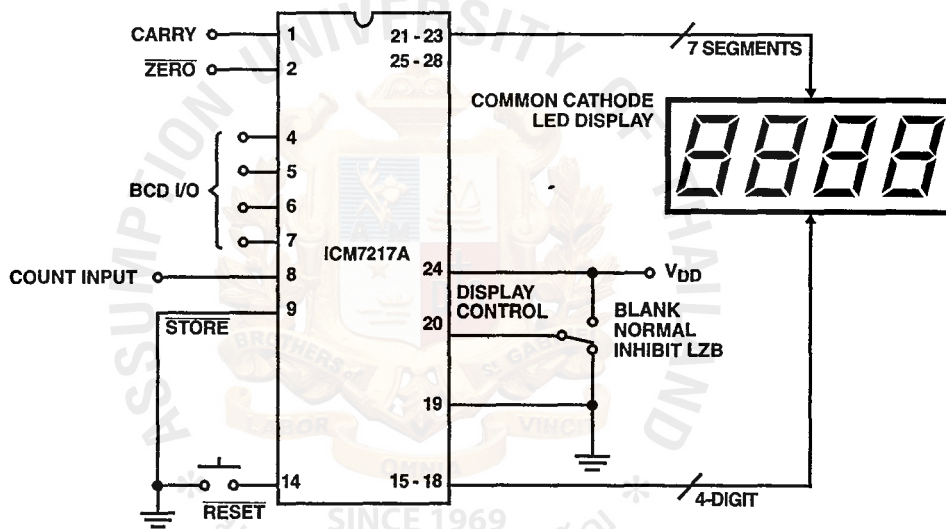


FIGURE 18. UNIT COUNTER

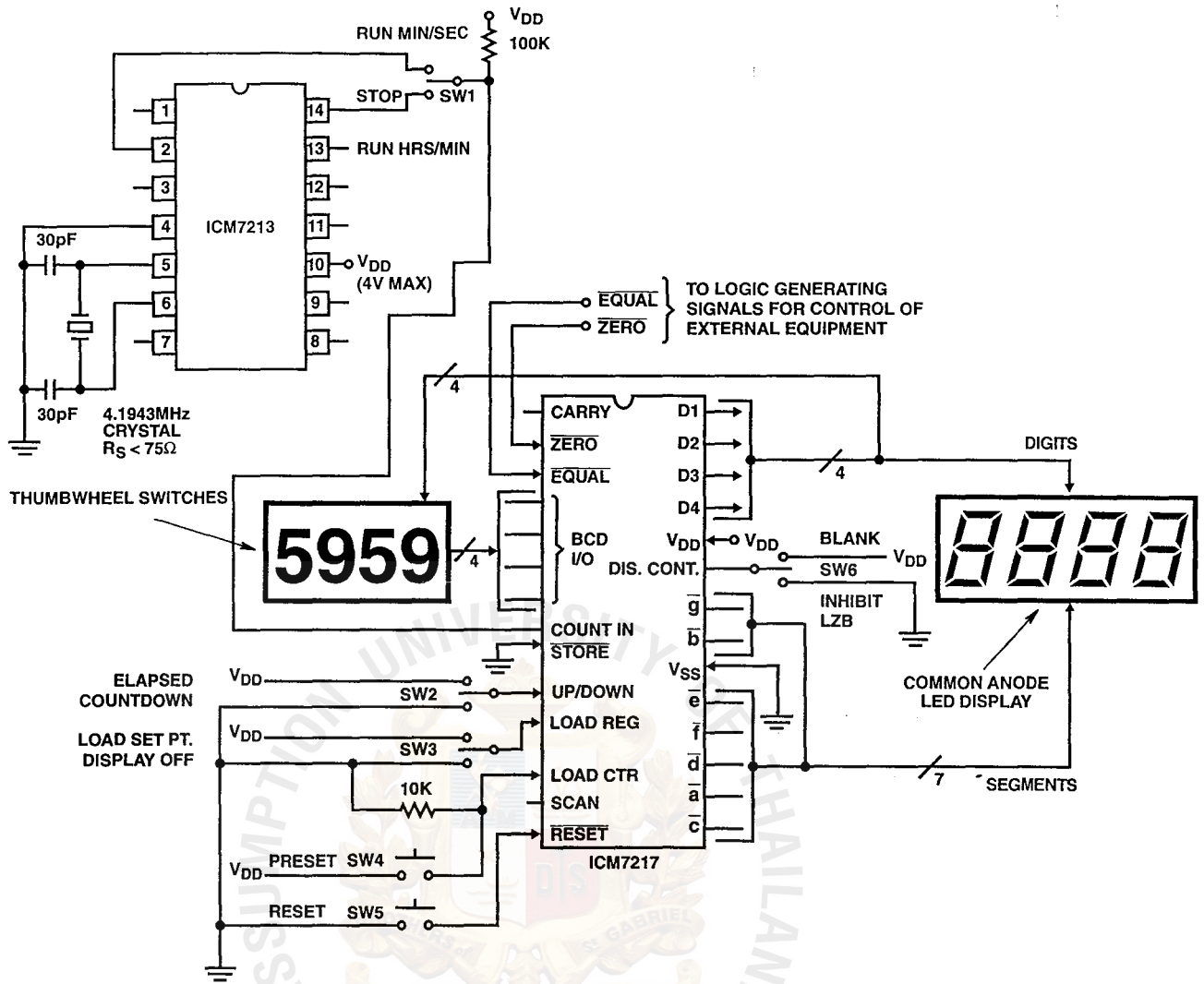


FIGURE 21. PRECISION TIMER

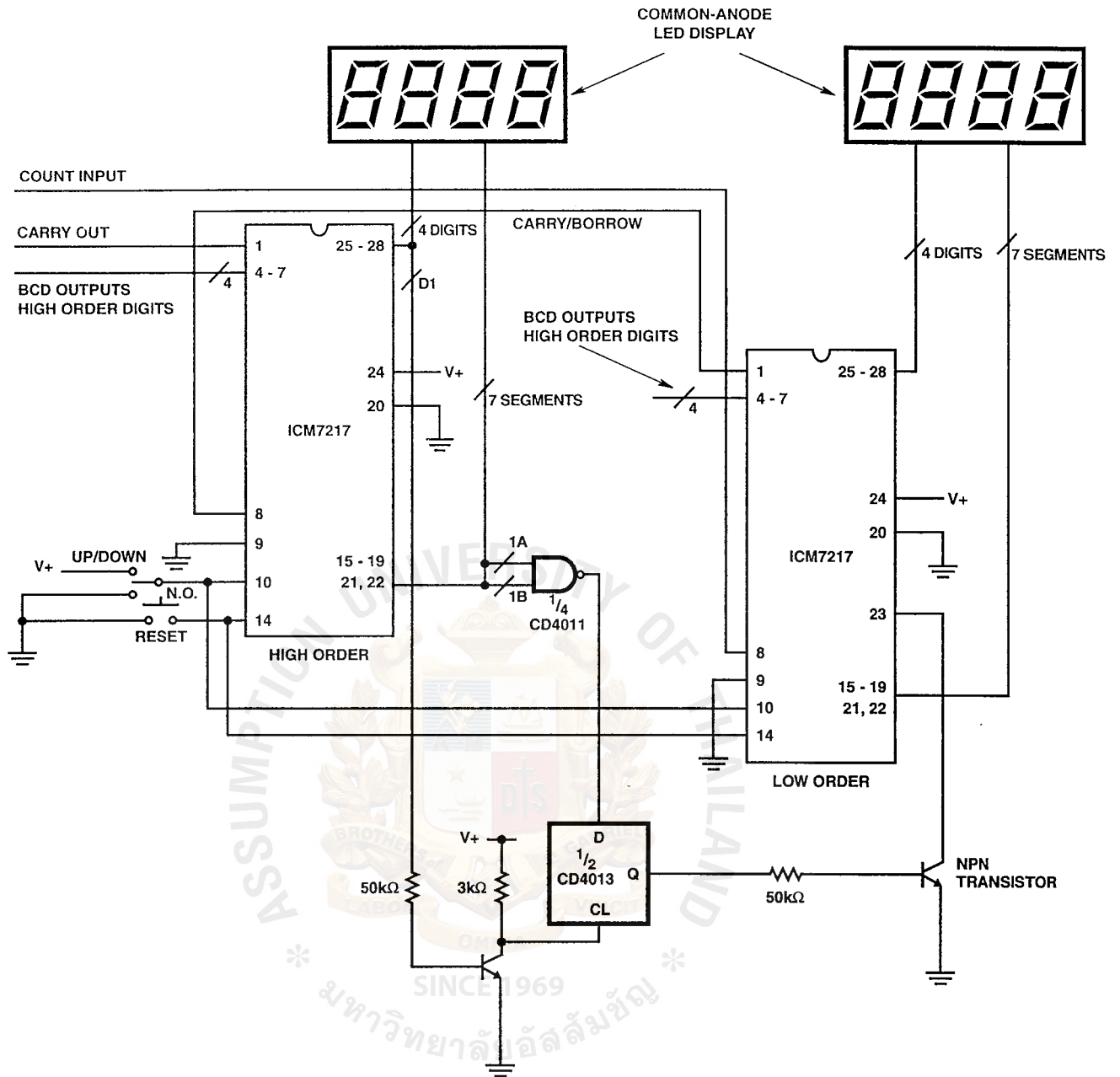


FIGURE 22. 8-DIGIT UP/DOWN COUNTER

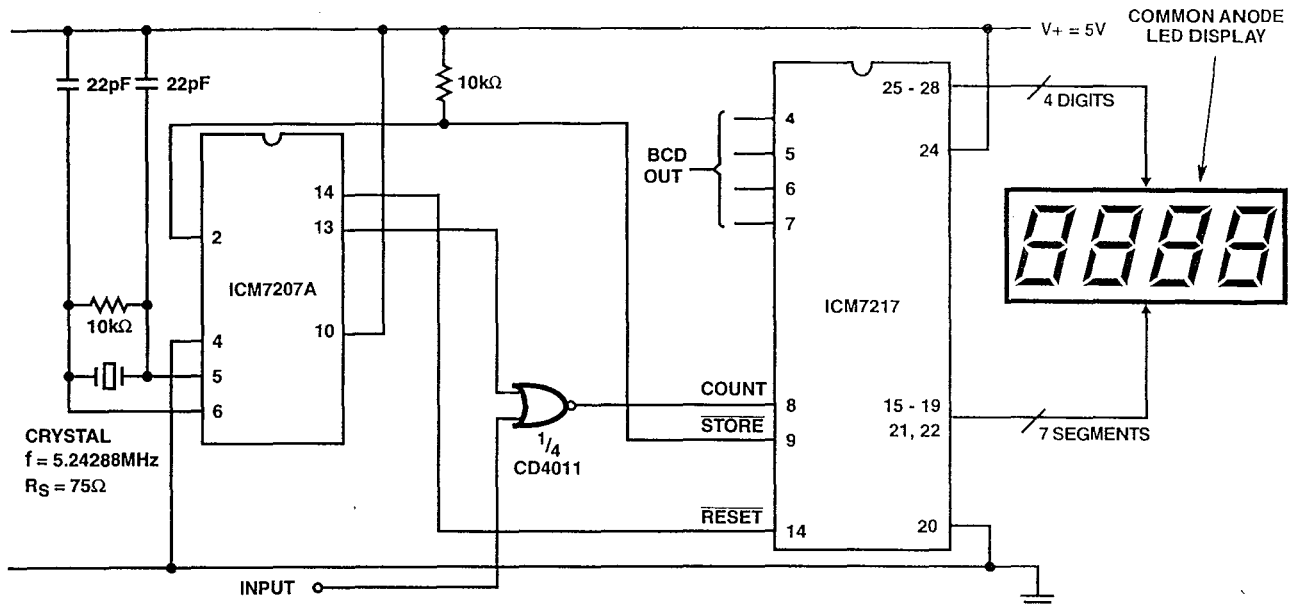


FIGURE 23. PRECISION FREQUENCY COUNTER (MHz MAXIMUM)

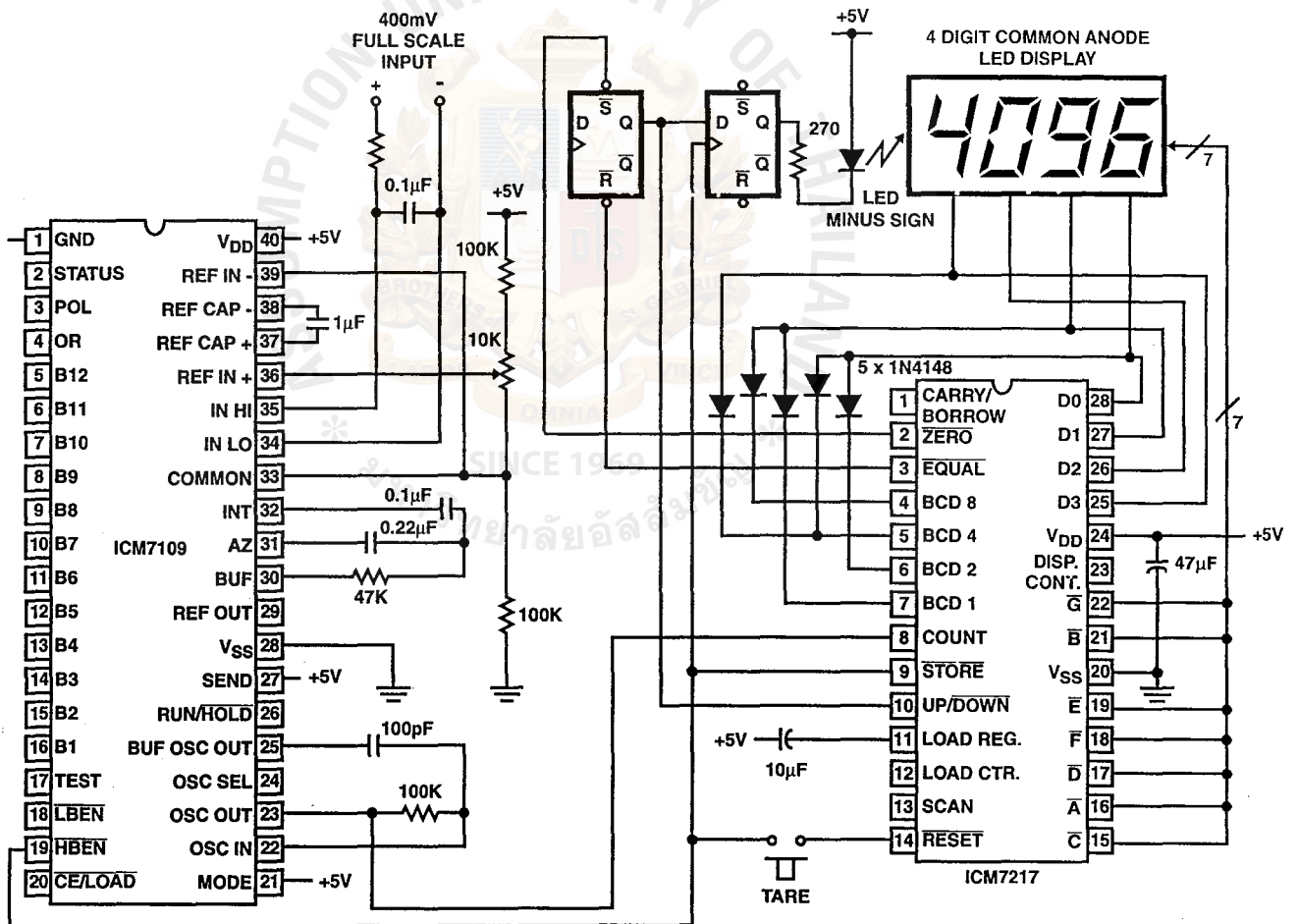


FIGURE 24. AUTO-TARE SYSTEM FOR A/D CONVERTER

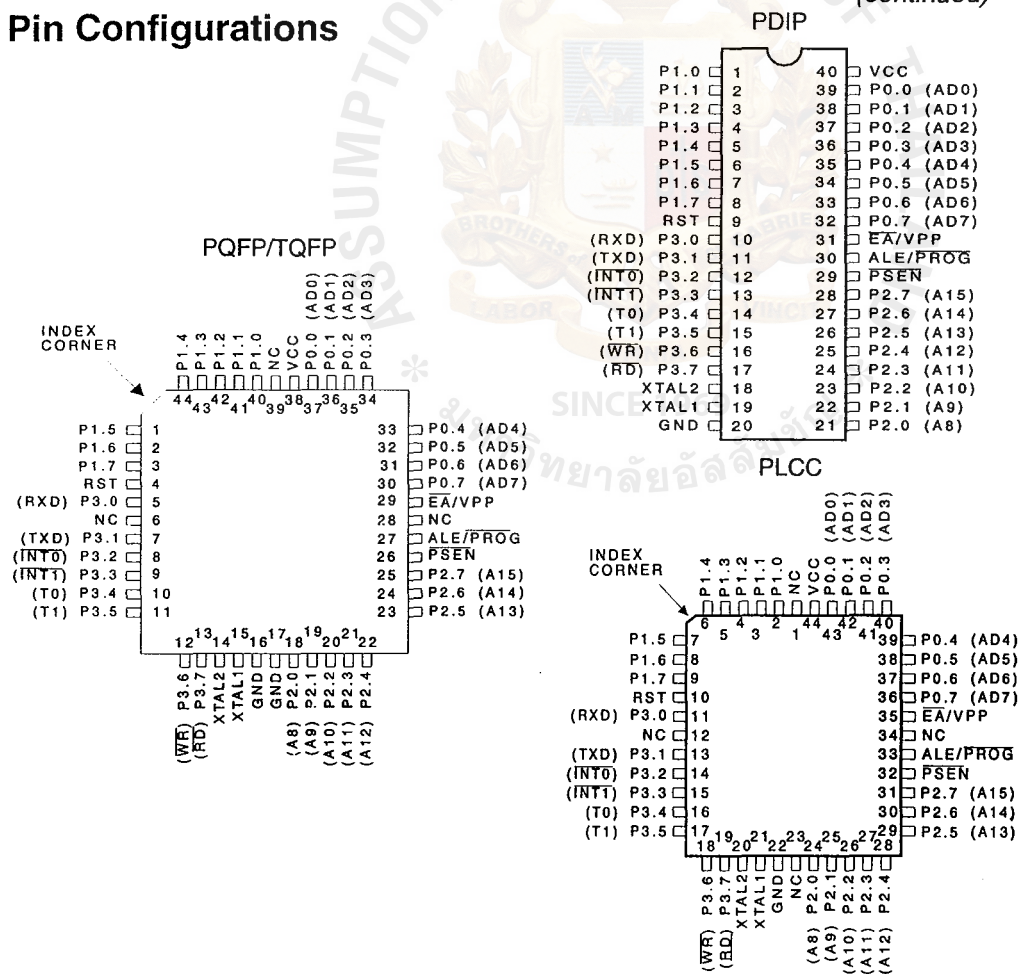
Features

- Compatible with MCS-51™ Products
- 4K Bytes of In-System Reprogrammable Flash Memory
 - Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

Description

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash Programmable and Erasable Read Only Memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

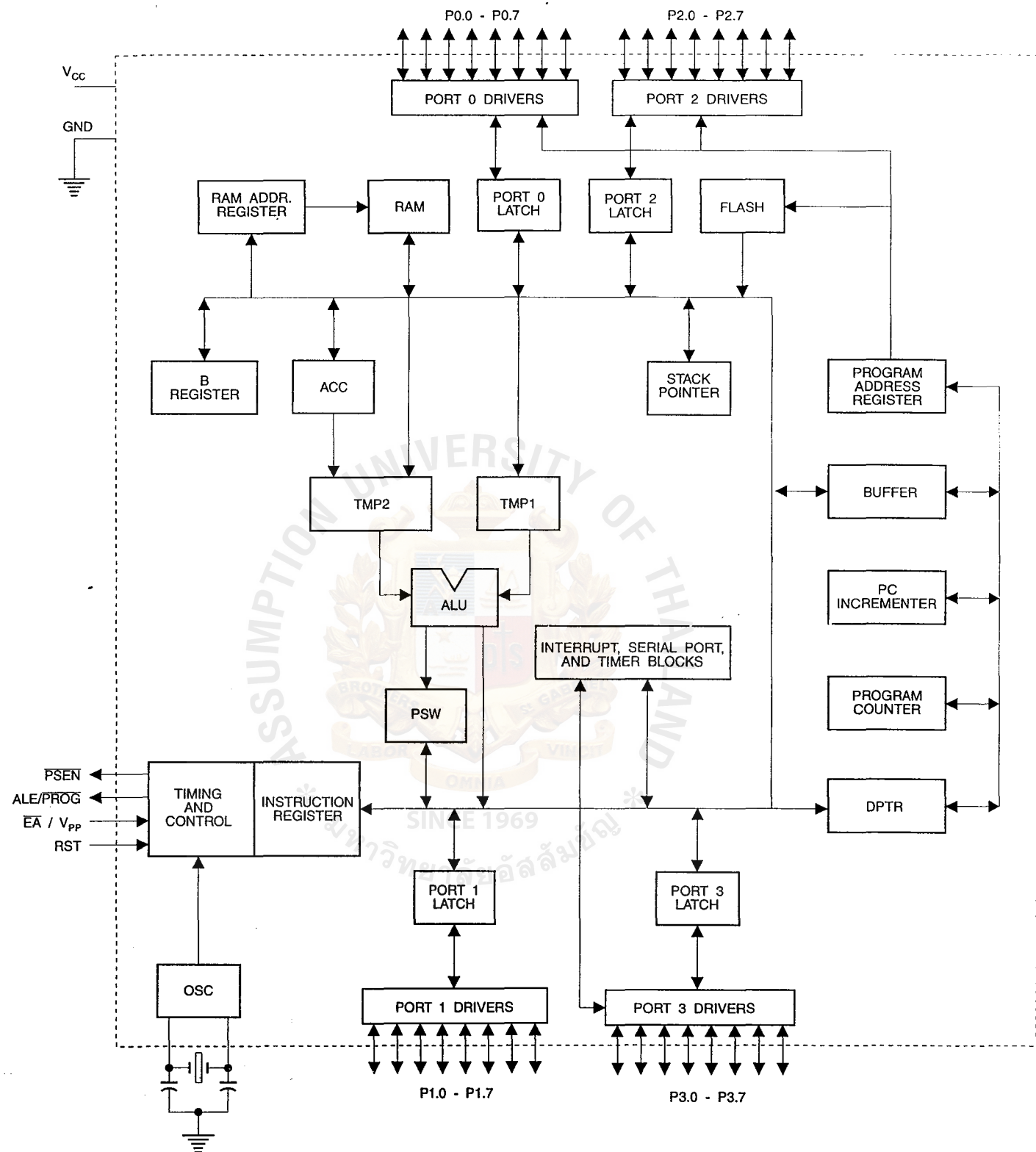
Pin Configurations



0265F-A-12/97



Block Diagram



The AT89C51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

Pin Description

V_{CC}
Supply voltage.

GND
Ground.

Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 may also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application it uses strong internal pullups

when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/PROG

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

PSEN

Program Store Enable is the read strobe to external program memory.

When the AT89C51 is executing code from external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory.

$\overline{\text{EA}}/\text{V}_{\text{PP}}$

External Access Enable. $\overline{\text{EA}}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{\text{EA}}$ will be internally latched on reset.

$\overline{\text{EA}}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming, for parts that require 12-volt V_{PP} .

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Oscillator Characteristics

XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

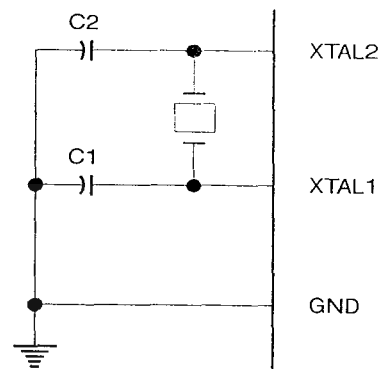
In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Status of External Pins During Idle and Power Down Modes

Mode	Program Memory	ALE	$\overline{\text{PSEN}}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

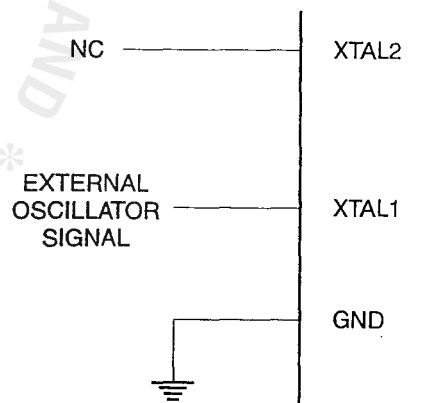
It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections



Note: $\text{C1}, \text{C2} = 30 \text{ pF} \pm 10 \text{ pF}$ for Crystals
 $= 40 \text{ pF} \pm 10 \text{ pF}$ for Ceramic Resonators

Figure 2. External Clock Drive Configuration



Power Down Mode

In the power down mode the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Lock Bit Protection Modes

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, \overline{EA} is sampled and latched on reset, and further programming of the Flash is disabled.
3	P	P	U	Same as mode 2, also verify is disabled.
4	P	P	P	Same as mode 3, also external execution is disabled.

Programming the Flash

The AT89C51 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage (V_{CC}) program enable signal. The low voltage programming mode provides a convenient way to program the AT89C51 inside the user's system, while the high-voltage programming mode is compatible with conventional third party Flash or EPROM programmers.

The AT89C51 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

	$V_{PP} = 12V$	$V_{PP} = 5V$
Top-Side Mark	AT89C51 xxxx yyww	AT89C51 xxxx-5 yyww
Signature	(030H)=1EH (031H)=51H (032H)=FFH	(030H)=1EH (031H)=51H (032H)=05H

The AT89C51 code memory array is programmed byte-by-byte in either programming mode. *To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.*

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

When lock bit 1 is programmed, the logic level at the \overline{EA} pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of \overline{EA} be in agreement with the current logic level at that pin in order for the device to function properly.

Programming Algorithm: Before programming the AT89C51, the address, data and control signals should be set up according to the Flash programming mode table and Figures 3 and 4. To program the AT89C51, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise \overline{EA}/V_{PP} to 12V for the high-voltage programming mode.
5. Pulse ALE/\overline{PROG} once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Data Polling: The AT89C51 features Data Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. Data Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/BSY output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/PROG low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H,

031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.


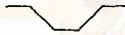



(030H) = 1EH indicates manufactured by Atmel
 (031H) = 51H indicates 89C51
 (032H) = FFH indicates 12V programming
 (032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

Mode		RST	PSEN	ALE/PROG	EA/V _{pp}	P2.6	P2.7	P3.6	P3.7
Write Code Data		H	L		H/12V	L	H	H	H
Read Code Data		H	L	H	H	L	L	H	H
Write Lock	Bit - 1	H	L		H/12V	H	H	H	H
	Bit - 2	H	L		H/12V	H	H	L	L
	Bit - 3	H	L		H/12V	H	L	H	L
Chip Erase		H	L	 (1)	H/12V	H	L	L	L
Read Signature Byte		H	L	H	H	L	L	L	L

Note: 1. Chip Erase requires a 10-ms PROG pulse.

Figure 3. Programming the Flash

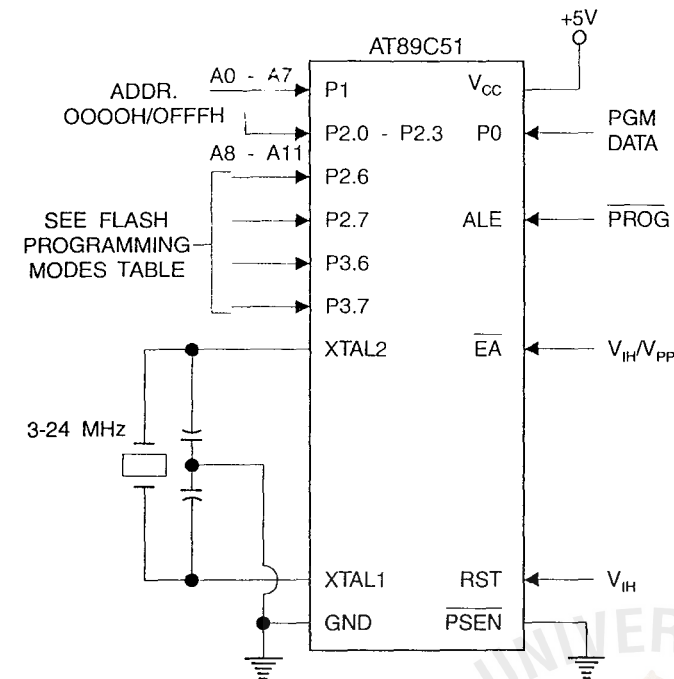
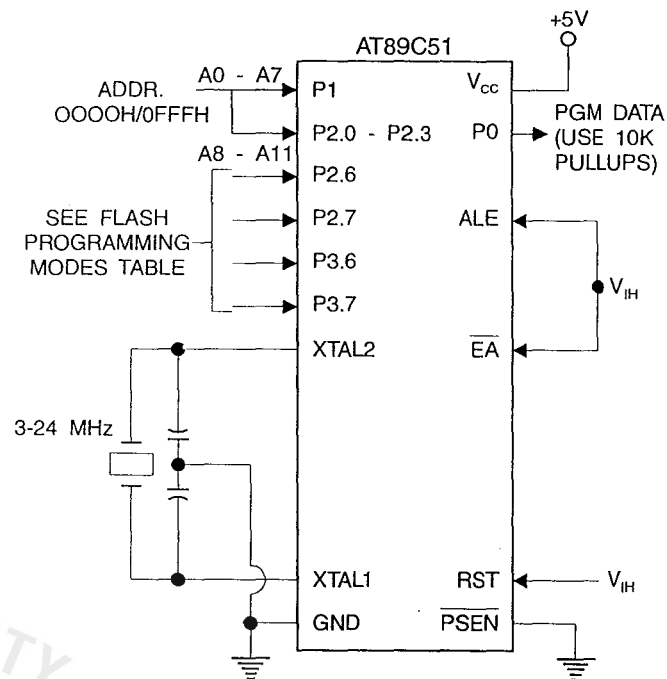


Figure 4. Verifying the Flash



Flash Programming and Verification Characteristics

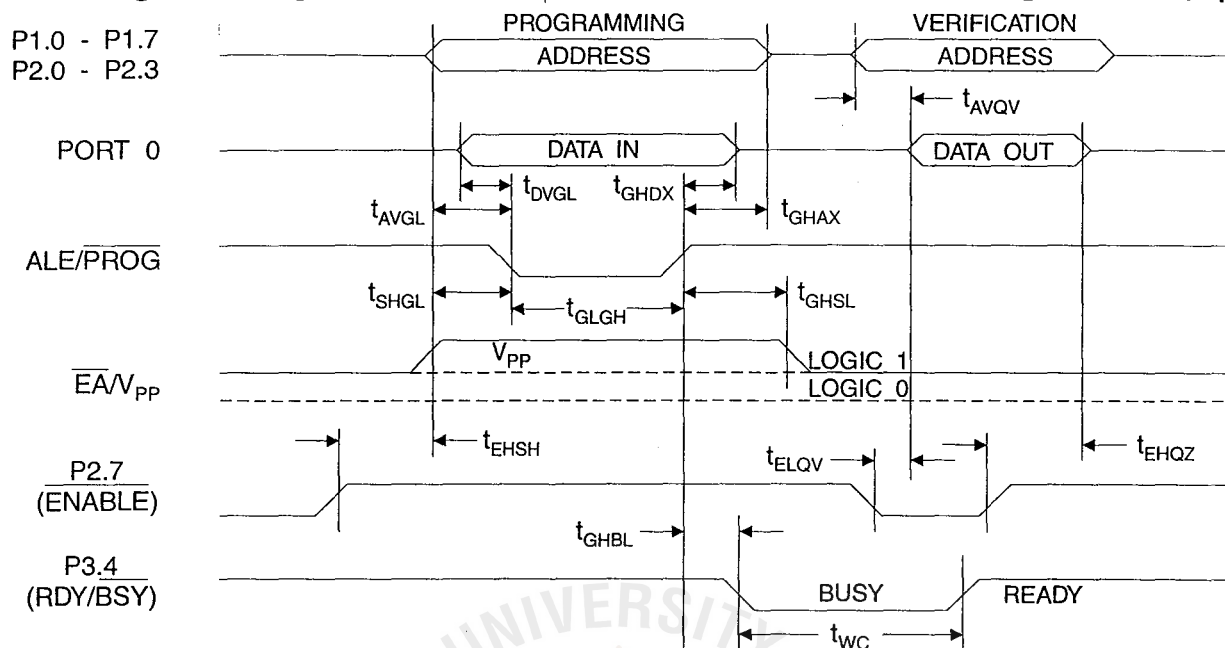
$T_A = 0^{\circ}\text{C}$ to 70°C , $V_{CC} = 5.0 \pm 10\%$

Symbol	Parameter	Min	Max	Units
$V_{PP}^{(1)}$	Programming Enable Voltage	11.5	12.5	V
$I_{PP}^{(1)}$	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{AVGL}	Address Setup to \overline{PROG} Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After \overline{PROG}	$48t_{CLCL}$		
t_{DVGL}	Data Setup to \overline{PROG} Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After \overline{PROG}	$48t_{CLCL}$		
t_{EHS}	P2.7 (\overline{ENABLE}) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to \overline{PROG} Low	10		μs
$t_{GHSL}^{(1)}$	V_{PP} Hold After \overline{PROG}	10		μs
t_{GLGH}	\overline{PROG} Width	1	110	μs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	\overline{ENABLE} Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After \overline{ENABLE}	0	$48t_{CLCL}$	
t_{GHL}	\overline{PROG} High to \overline{BUSY} Low		1.0	μs
t_{WC}	Byte Write Cycle Time		2.0	ms

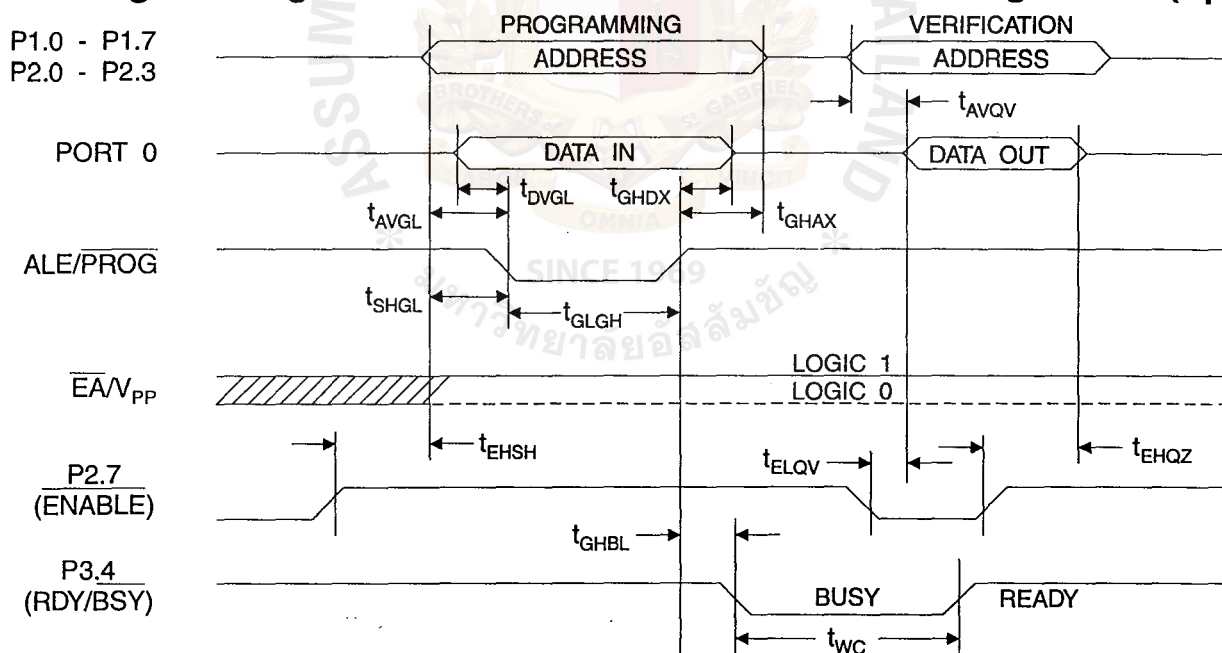
Note: 1. Only used in 12-volt programming mode.



Flash Programming and Verification Waveforms - High Voltage Mode ($V_{PP} = 12V$)



Flash Programming and Verification Waveforms - Low Voltage Mode ($V_{PP} = 5V$)



Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage.....	6.6V
DC Output Current.....	15.0 mA

***NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = -40^\circ\text{C}$ to 85°C , $V_{CC} = 5.0\text{V} \pm 20\%$ (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except \overline{EA})	-0.5	$0.2 V_{CC} - 0.1$	V
V_{IL1}	Input Low Voltage (\overline{EA})		-0.5	$0.2 V_{CC} - 0.3$	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	$0.2 V_{CC} + 0.9$	$V_{CC} + 0.5$	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	$0.7 V_{CC}$	$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage ⁽¹⁾ (Ports 1,2,3)	$I_{OL} = 1.6 \text{ mA}$		0.45	V
V_{OL1}	Output Low Voltage ⁽¹⁾ (Port 0, ALE, PSEN)	$I_{OL} = 3.2 \text{ mA}$		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, PSEN)	$I_{OH} = -60 \mu\text{A}$, $V_{CC} = 5\text{V} \pm 10\%$	2.4		V
		$I_{OH} = -25 \mu\text{A}$	$0.75 V_{CC}$		V
		$I_{OH} = -10 \mu\text{A}$	$0.9 V_{CC}$		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	$I_{OH} = -800 \mu\text{A}$, $V_{CC} = 5\text{V} \pm 10\%$	2.4		V
		$I_{OH} = -300 \mu\text{A}$	$0.75 V_{CC}$		V
		$I_{OH} = -80 \mu\text{A}$	$0.9 V_{CC}$		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	$V_{IN} = 0.45\text{V}$		-50	μA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	$V_{IN} = 2\text{V}$, $V_{CC} = 5\text{V} \pm 10\%$		-650	μA
I_{LI}	Input Leakage Current (Port 0, \overline{EA})	$0.45 < V_{IN} < V_{CC}$		± 10	μA
RRST	Reset Pulldown Resistor		50	300	$\text{K}\Omega$
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, $T_A = 25^\circ\text{C}$		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
	Power Down Mode ⁽²⁾	$V_{CC} = 6\text{V}$		100	μA
		$V_{CC} = 3\text{V}$		40	μA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

Maximum I_{OL} per port pin: 10 mA

Maximum I_{OL} per 8-bit port: Port 0: 26 mA

Ports 1, 2, 3: 15 mA

Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V_{CC} for Power Down is 2V.



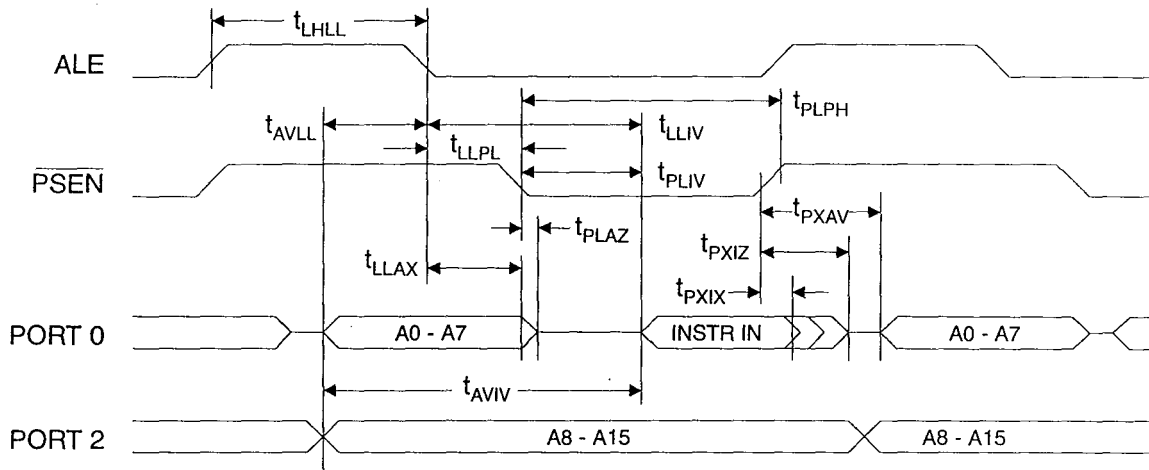
AC Characteristics

(Under Operating Conditions; Load Capacitance for Port 0, ALE/ $\overline{\text{PROG}}$, and $\overline{\text{PSEN}}$ = 100 pF; Load Capacitance for all other outputs = 80 pF)

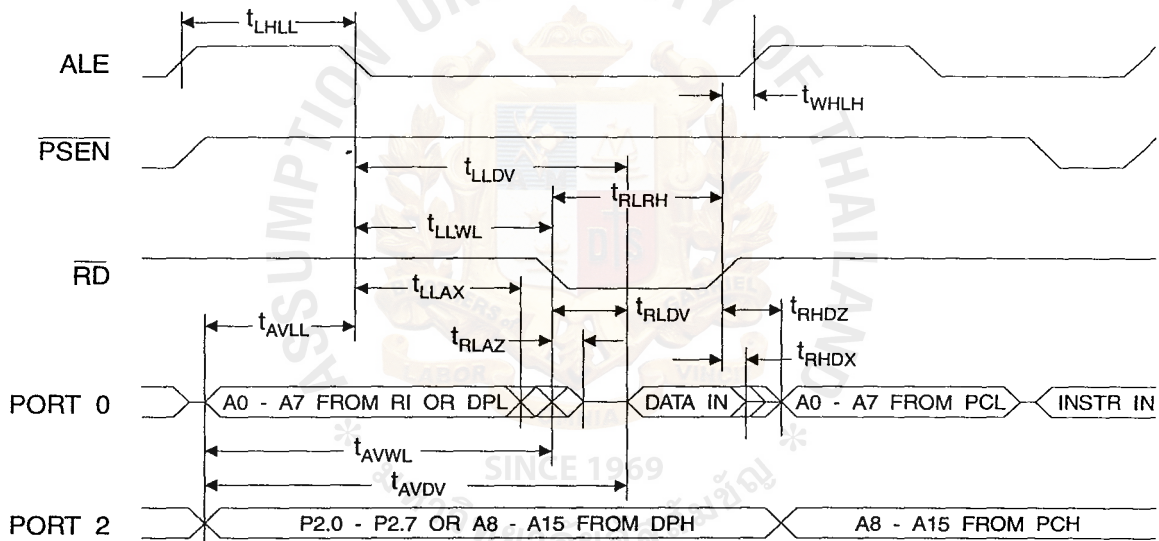
External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		16 to 24 MHz Oscillator		Units
		Min	Max	Min	Max	
$1/t_{\text{CLCL}}$	Oscillator Frequency			0	24	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{\text{CLCL}}-40$		ns
t_{AVLL}	Address Valid to ALE Low	43		$t_{\text{CLCL}}-13$		ns
t_{LLAX}	Address Hold After ALE Low	48		$t_{\text{CLCL}}-20$		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{\text{CLCL}}-65$	ns
t_{LLPL}	ALE Low to $\overline{\text{PSEN}}$ Low	43		$t_{\text{CLCL}}-13$		ns
t_{PLPH}	$\overline{\text{PSEN}}$ Pulse Width	205		$3t_{\text{CLCL}}-20$		ns
t_{PLIV}	$\overline{\text{PSEN}}$ Low to Valid Instruction In		145		$3t_{\text{CLCL}}-45$	ns
t_{PXIX}	Input Instruction Hold After $\overline{\text{PSEN}}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{\text{PSEN}}$		59		$t_{\text{CLCL}}-10$	ns
t_{PXAV}	$\overline{\text{PSEN}}$ to Address Valid	75		$t_{\text{CLCL}}-8$		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{\text{CLCL}}-55$	ns
t_{PLAZ}	$\overline{\text{PSEN}}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{\text{RD}}$ Pulse Width	400		$6t_{\text{CLCL}}-100$		ns
t_{WLWH}	$\overline{\text{WR}}$ Pulse Width	400		$6t_{\text{CLCL}}-100$		ns
t_{RLDV}	$\overline{\text{RD}}$ Low to Valid Data In		252		$5t_{\text{CLCL}}-90$	ns
t_{RHDX}	Data Hold After $\overline{\text{RD}}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{\text{RD}}$		97		$2t_{\text{CLCL}}-28$	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{\text{CLCL}}-150$	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{\text{CLCL}}-165$	ns
t_{LLWL}	ALE Low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	200	300	$3t_{\text{CLCL}}-50$	$3t_{\text{CLCL}}+50$	ns
t_{AVWL}	Address to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	203		$4t_{\text{CLCL}}-75$		ns
t_{QVWX}	Data Valid to $\overline{\text{WR}}$ Transition	23		$t_{\text{CLCL}}-20$		ns
t_{QVWH}	Data Valid to $\overline{\text{WR}}$ High	433		$7t_{\text{CLCL}}-120$		ns
t_{WHQX}	Data Hold After $\overline{\text{WR}}$	33		$t_{\text{CLCL}}-20$		ns
t_{RLAZ}	$\overline{\text{RD}}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE High	43	123	$t_{\text{CLCL}}-20$	$t_{\text{CLCL}}+25$	ns

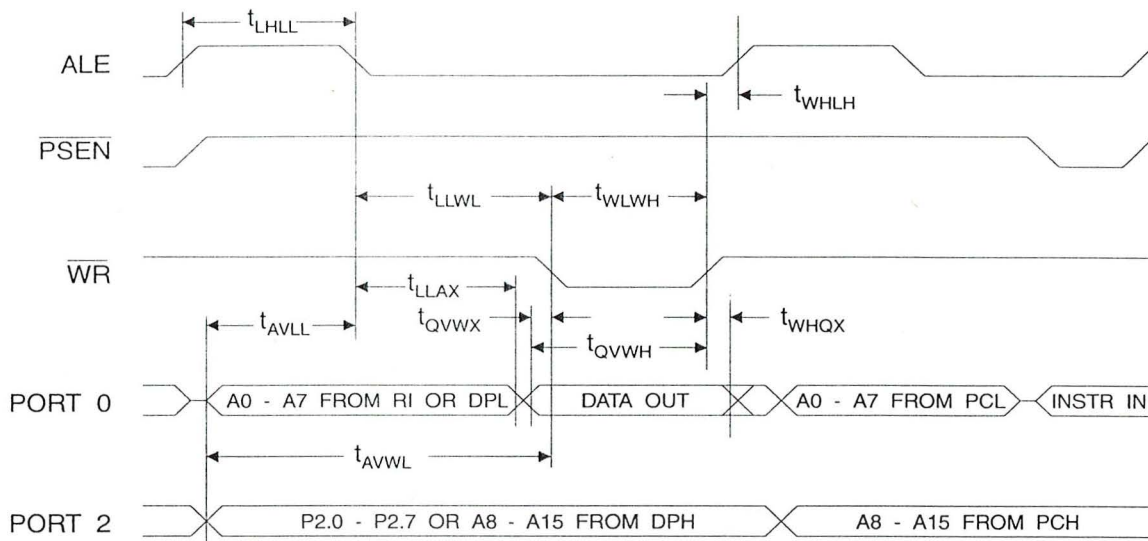
External Program Memory Read Cycle



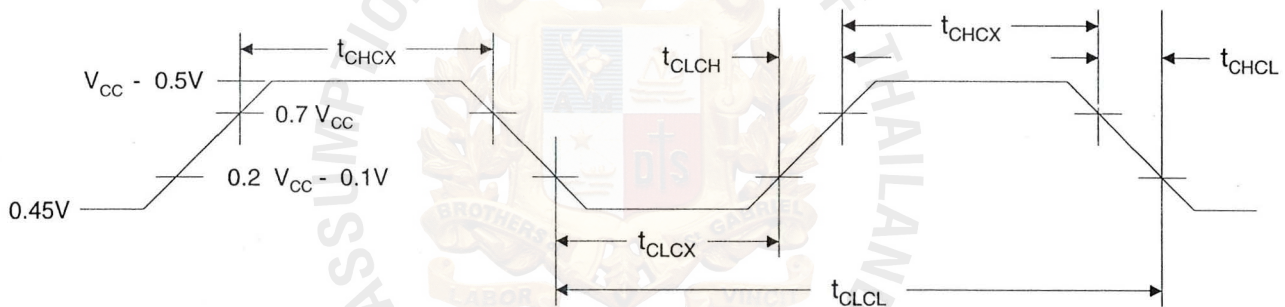
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

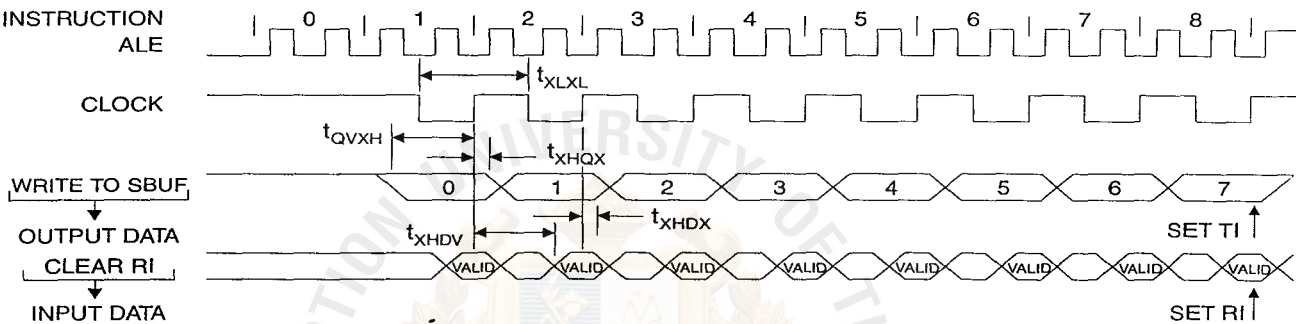
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

($V_{CC} = 5.0\text{ V} \pm 20\%$; Load Capacitance = 80 pF)

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		μs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}-133$		ns
t_{XHGX}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}-117$		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDX}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}-133$	ns

Shift Register Mode Timing Waveforms



AC Testing Input/Output Waveforms⁽¹⁾ Float Waveforms⁽¹⁾



- Note: 1. AC Inputs during testing are driven at $V_{CC} - 0.5\text{V}$ for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.
- Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	5V ± 20%	AT89C51-12AC	44A	Commercial (0°C to 70°C)
		AT89C51-12JC	44J	
		AT89C51-12PC	40P6	
		AT89C51-12QC	44Q	
		AT89C51-12AI	44A	Industrial (-40°C to 85°C)
		AT89C51-12JI	44J	
		AT89C51-12PI	40P6	
		AT89C51-12QI	44Q	
		AT89C51-12AA	44A	Automotive (-40°C to 105°C)
		AT89C51-12JA	44J	
		AT89C51-12PA	40P6	
		AT89C51-12QA	44Q	
16	5V ± 20%	AT89C51-16AC	44A	Commercial (0°C to 70°C)
		AT89C51-16JC	44J	
		AT89C51-16PC	40P6	
		AT89C51-16QC	44Q	
		AT89C51-16AI	44A	Industrial (-40°C to 85°C)
		AT89C51-16JI	44J	
		AT89C51-16PI	40P6	
		AT89C51-16QI	44Q	
		AT89C51-16AA	44A	Automotive (-40°C to 105°C)
		AT89C51-16JA	44J	
		AT89C51-16PA	40P6	
		AT89C51-16QA	44Q	
20	5V ± 20%	AT89C51-20AC	44A	Commercial (0°C to 70°C)
		AT89C51-20JC	44J	
		AT89C51-20PC	40P6	
		AT89C51-20QC	44Q	
		AT89C51-20AI	44A	Industrial (-40°C to 85°C)
		AT89C51-20JI	44J	
		AT89C51-20PI	40P6	
		AT89C51-20QI	44Q	

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	5V ± 20%	AT89C51-24AC	44A	Commercial (0°C to 70°C)
		AT89C51-24JC	44J	
		AT89C51-24PC	44P6	
		AT89C51-24QC	44Q	
		AT89C51-24AI	44A	Industrial (-40°C to 85°C)
		AT89C51-24JI	44J	
		AT89C51-24PI	44P6	
		AT89C51-24QI	44Q	



Package Type	
44A	44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44Q	44 Lead, Plastic Gull Wing Quad Flatpack (PQFP)



