Physical Layer for Wireless LAN at 915 MHz (RF Part)

by

Myint Shwe

Faculty of Engineering
March 2000

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(RF Part)

A thesis

submitted to the Faculty of Engineering

by

Myint Shwe

in partial fulfillment of the requirements

for the degree of

Master of Engineering in Broadband Telecommunications

Advisor: Dr. Sudhiporn Patumtaewapibal

Assumption University

Bangkok, Thailand

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ABSTRACT

This thesis is a hardware design for the Physical Layer of 915 MHz wireless Local Area Network (wireless LAN), RF part. In transmitting mode, this design receives Direct Sequence Spread Spectrum (DSSS) signal with Quadrature Phase Shift Keying (QPSK) modulation at 80MHz IF frequency. This signal is filtered, upconverted to 915 MHz, amplified and transmitted by using monopole antenna. In receiving mode, the signal received by the monopole antenna is filtered, amplified, and downconverted to 80 MHz. This thesis also includes Dual Frequency Synthesizer design, which is very important in wireless communication.

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CHAPTER 1. INTRODUCTION

1.1 What is Wireless LANs

Traditional LANs link PCs and other computers to one another and to file servers, printers and other network equipment by using cables or fiber optics as the transmission medium. Figure 1.1 shows the standard Ethernet based LAN configuration.

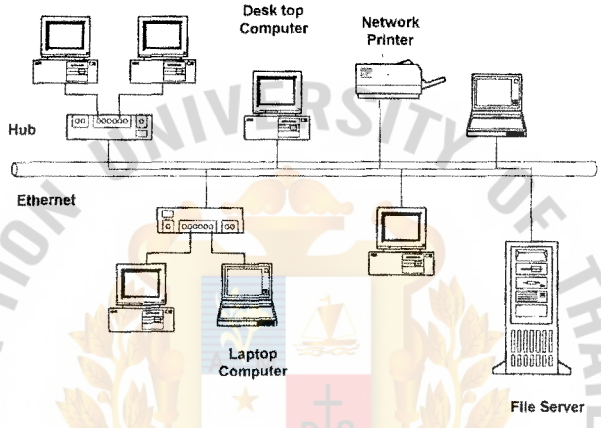

Figure 1.1 Ethernet Local Area Network Configuration

Wireless LANs provide an alternative to the traditional LANs that is based on twisted pair, coaxial cable, and fiber optic cable. The wireless LANs serve the same purpose as that of a wired or optical LANs to convey information among the devices attached to the LAN.

Wireless LANs use electromagnetic airwaves (radio or infrared) to communicate information from one point to another without relying on any physical connection. The data being transmitted is superimposed on the radio carrier so that it can be extracted at the receiving end. This is generally referred to as modulation of the carrier by the information being transmitted. Once data is modulated onto the radio carrier, the radio signal occupies more than a single frequency, since the frequency or bit rate of the modulating information adds to the carrier.

Wireless LANs have gained strong popularity in a number of markets, including the health-care, retail, manufacturing, warehousing, and academic. These industries have profited from the productivity gains of using hand-held terminals and notebook computers to transmit real-time information to centralized hosts for processing. The wireless LANs can be connected to an existing wired LANs as an extension, or can be form the basis of a new network. Figure 1.2 shows the configuration for the wireless network.

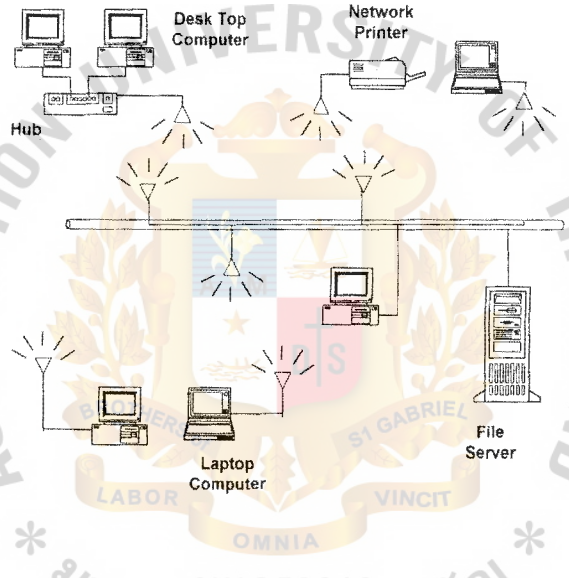

Figure 1.2 Wireless Local Area Network Configuration

While adaptable to both indoor and outdoor environments, wireless LANs are especially suited to indoor locations such as office buildings, manufacturing floors, hospitals and universities. The basic building block of the wireless LANs is the cell. The coverage area of a cell depends on the strength of the propagated radio signal and the type and construction of walls, partitions and other physical characteristics of the indoor environment. PC-based workstations, notebook and pen-based computers can move freely in the cell.

1.2 History of Wireless LANs

In 1971, the University of Hawaii was brought a research project called ALOHANET, which combined Network technologies and Radio communication together. The ALOHANET system enabled computer sites at seven campuses spread out over four islands to communicate with the central computer on Oahu without using the existing telephone line. ALOHANET offered bidirectional communications between the central computer and each of remote stations. The remote stations had to communicate with one another via the centralized computer.

In the 1980s amateur radio hobbyists design radio networking within the United State and Canada. That design used terminal node controller (TNCs) to interface their computers through ham radio equipment. TNCs converting the computer's digital signal into analog signal that ham radio can modulate and send over the air by using packet switching. Thus, hams have been utilizing wireless networking much earlier than commercial market. Figure 1.3 shows the Hams radio configurations.

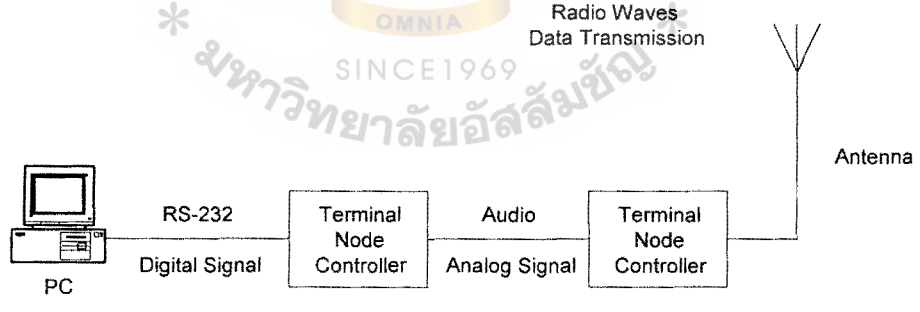

Figure 1.3 Hams Radio Network by Using Terminal Node Controller

In 1985, the Federal Communication Commission (FCC) allows users to operate wireless products without obtaining licenses in the Industrial, Scientific and Medical (ISM) bands. The ISM frequency band is shown in the figure 1.4. This band of

frequencies resides between 902 MHz and 5.85 GHz. The ISM band is very attractive to wireless network vendors because it provides a free spectrum for their products and the end users do not have to obtain FCC licenses to operate their products. The ISM band allocation has had a dramatic effect on the wireless industry, prompting the development of wireless LANs components.

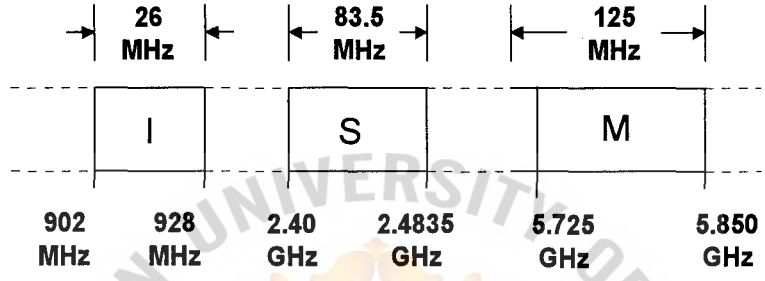

Figure 1.4 The ISM Frequency Band

The 900 MHz band has been the most popular for the early wireless LANs applications based on the availability of products introduced in the early 1990s. One of the disadvantages of 900 MHz is no interoperability. Vendors just apply their proprietary radio protocol. The 900 MHz band is more crowded than other frequency band. In the US this band is used for cordless telephones and internationally this band is widely used for cellular or military communications. Because of these reasons, the market has been slowly shifting to more recently develop 2.4 GHz products.

The bandwidth of 2.4 GHz band is three times larger than the 900 MHz band and it is possible to support faster rates. Transmission on the 2.4 GHz band is cleaner than 900 MHz because it carries less competing traffic. The wireless LANs standard such as 802.11 and WLIF OpenAir are based upon the 2.4 GHz frequency band.

Products based on the 5 GHz is still largely experimental. Although the 5 GHz band will support higher data rates than current systems, it must overcome challenges for range and power consumption.

1.4 Current Wireless LANs Technology

The wireless LANs standard working group, IEEE 802.11, was established in July 1990. The purpose of this group is to specify a medium access control protocol and physical layer implementations for wireless LANs.

At the physical layer, IEEE 802.11 defines the three physical characteristics for wireless LANs: diffused infrared, direct sequence spread spectrum (DSSS), and frequency hopping spread spectrum (FHSS).

The infrared physical layer operates at the baseband. Infrared physical layer is a optical based and used infrared light to transmit data. The infrared physical provides for 1 Mbps data rates with 2 Mbps rate for optional and relies on Pulse Position Modulation (PPM).

Both DSSS and FHSS artificially spread the transmission band so that the transmitted signal can be accurately received and decoded in the face of noise. Two radio based physical layers operate at the 2.4 GHz band.

Each of the physical layers uses their own unique header to synchronize the receiver and to determine signal modulation format and data packet length. The physical layer herders are always transmitting at 1 Mbps. The predefined fields in the headers provide the option to increase the data rate to 2 Mbps for actual data packet.

The distance that the RF and IR waves can communicate is a function of product design (including transmitted power and receiver design) and the propagation

path, especially in indoor environments. The building objects, including walls, metal, and even people, can affect to the energy propagation and thus affect to the range and coverage of a particular system. IR is blocked by solid objects and which provides additional limitations. Most wireless LANs systems use RF because radio waves can penetrate many indoor walls and surfaces. The range (or radius of coverage) for typical wireless LANs systems can vary from under 100 feet to more than 300 feet.

Like wired based 802.3, the 802.11 MAC layer used Carrier Sense Multiple Access (CSMA) protocol. But it used with Collision Avoidance (CA) instead of Collision Detection (CD) because it is very to detect collision in the radio channel. The CSMA/CA protocol allows for options that can minimize collisions by using request to send (RTS), clear to send (CTS), data and acknowledge (ACK) transmission frames, in a sequential fashion. Communications is established when one of the wireless nodes sends a short message RTS frame. The RTS frame includes the destination and the length of the message. The message duration is known as the network allocation vector (NAV). The NAV alerts all other is the medium to back off for the duration of the transmission.

The receiving station issues a CTS frame which echoes the senders address and the NAV. If the CTS frame is not received, it is assumed that a collision occurred and the RTS process starts over. After the data frame is received, an ACK frame is sent back verifying a successful data transmission. The CSMA/CA process is also known as "listen before talk scheme". This algorithm is shown in figure 1.5. A station wishing to transmit must first “listen” to the radio channel to determine if another station is transmitting. If the medium is not busy, the transmission may proceed.

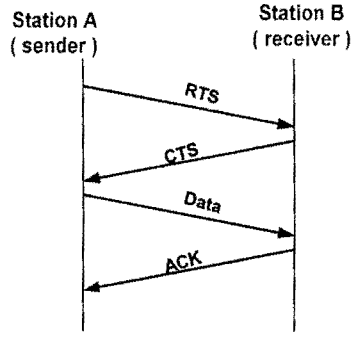

Figure 1.5 RTS/CTS Frame Algorithm

The CSMA/CA scheme implements a minimum time gap between frames from a given user. Once a frame has been sent from a given transmitting station, that station must wait until the time gap is completed to transmit again. Once the time has passed, the station selects a random amount of time (called a backoff interval) to wait before "listening" again to verify a clear channel on which to transmit. If the channel is still busy, another backoff interval is selected that is less than the first. This process is repeated until the waiting time approaches zero and the station is allowed to transmit.

1.4 Future Wireless LANs

The 802.11b is the extension of the IEEE standard 802.11-1997 with a higher data rate PHY in the 2.4 GHz band. The purpose of this project is to extend the performance and the range of applications of the existing 802.11 standard. The header of the two existing radio based PHYs can support data rate up to 4.5 Mbps for frequency hopping and up to 25.5 Mbps for direct sequence.

The 802.11 approved a proposal jointly developed by Lucent Technologies and Intersil (formerly known as Harris Semiconductor) for a throughput of up to 11 Mbps. The new specification will rely on direct sequence spread spectrum using a special coding scheme known as complementary code keying (CCK). CCK supports both 11 Mbps and 5.5 Mbps, using the same 2.4 GHz bandwidth and current 802.11 standard.

Accepted by the IEEE 802.11, several of the wireless industry's largest players have united to drive the adoption of standard for high-speed wireless LANs. These players include 3Com, Aironet, Intersil, Lucent Technologies, Nokia, and Symbol Technologies. Lucent and the five other companies have formed the Wireless Ethernet Compatibility Alliance (WECA). The goal of this organization is to promote the acceptance and standardization of IEEE 802.11 HR products.

To accelerate the acceptance of the IEEE 802.11 HR standard, the WECA is establishing an industry sanctioned test lab to test and certify the interoperability of any member's products. WECA will grant a seal of interoperability to vendors upon successful completion of the prescribed test suites.

802.11a is the extension of the IEEE standard 802.11-1997 with a higher data rate PHY in the 5 GHz band. This project was initiated to develop a high speed about 20 Mbps wireless PHY suitable for data, voice and image information services in fixed, moving or portable wireless LANs. This project concentrates on improving spectrum efficiency and will review the existing 802.11 MAC to ensure its capability to operate at the higher speeds.

1.5 Design Goal

The main objective of this thesis is to design and build high performance physical layer of wireless LAN with minimum possible cost. To get this goal 902-928 MHz ISM band is chosen for this thesis. This design is based on direct sequence spread spectrum for RF transceiving.

In chapter 2, physical layer architecture and IEEE 802.11 Direct Sequence Spread Spectrum (DSSS) physical layer standard will be described. Introduction to indoor propagation is also discussed in that chapter and use d_n model to calculate path loss for 915 MHz wireless LAN.

Chapter 3 presents the hardware design. This includes, link budget calculation, transmitter design, receiver design, dual frequency synthesizer design for 995 MHz and 160 MHz, VCO tuning designs. It also presents the synthesizer simulation by using Ansoft simulator.

The measurement results are shown in chapter 4. These have done at antenna port, 160 MHz local oscillator port and 80 MHz receiver port. These measurements have done by using 915 MHz carrier frequency as well as 904-926 MHz spread spectrum signals.

Chapter 5, conclusion chapter, discusses the performance of this hardware design, future work and suggestions for this thesis.

CHAPTER 2. IEEE 802.11 PHYSICAL LAYER

2.1 Physical Layer Architecture

The architecture of physical layer consists of the three components for each station. The first component is Physical Layer Management and it performs management function for physical layer.

The second component, Physical Layer Convergence Procedure (PLCP) sub layer received MAC Protocol Data Unit (MPDU) from MAC layer for transmission. It also delivers incoming frames from the wireless medium to the MAC layer.

The third component, Physical Medium Dependent (PMD) sub layer provides actual transmission and reception of physical layer entities between two station via the wireless medium. It provides modulation and demodulation of the frame transmissions.

The operation of the individual physical layers is very similar. To perform PLCP functions, the 802.11 standard specifies the use of state machine. Each state machine perform the following functions:

Carrier Sense: to determine the state of the medium

Transmit: to send the data frame

Receive: to receive data frame

The physical layer implements the carrier sense operation by detecting the PMD to check whether the medium is busy or idle. When the medium becomes busy, the PLCP will read the PLCP preamble and header of the frame to attempt synchronization of the receiver to the data of the signal.

PLCP will switch the PMD to transmit mode after receiving the request service from MAC layer. MAC layer sends the data frame and data rate instruction along with the request. The PMD respond by sending the preamble of the frame.

PLCP will switch the PMD to transmit mode after receiving the request service from MAC layer. MAC layer sends the data frame and data rate instruction along with the request. The PMD respond by sending the preamble of the frame.

The transmitter sends the preamble and header at 1 Mbps to provide a specific common data rate for the receiver to always listen. After sending the header, the transmitter changes the data rate of the transmission to what the header specifies. After transmission take place, the PLCP sends a confirm signal to the MAC layer, shuts off the transmitter and switches the PMD circuitry to receive mode.

If the PLCP discovers a busy medium and valid preamble of an incoming frame, it will monitor the header of the frame. If the header is error free, the PLCP will send a receiver start control signal to the MAC layer for notification of an incoming frame. After receiving the final octet, the PLCP send a receiver end control signal to the MAC layer to indicate the end of frame.

The received function will operate with single or multiple antenna diversities. Diversity is a method of improving reception by receiving the signal on multiple antennas.

2.2 IEEE 802.11 DSSS Physical Layer

The general idea of DSSS is to first digitally spread the basedband data frame (PPDU) and then modulate the spread data to a particular frequency.

The transmitter spreads the PPDU by combining with pseudo-noise (PN) code via the binary adder. The PN code sequence for DS systems consists of a service of plus and minus 1s. The specific PN code for 802.11 is the following 11chip sequence.

+1, -1, +1, +1, -1, +1, +1, +1, -1, -1, -1

The figure of merit for DSSS system is known as processing gain, which is equal to the data rate of the spread DSSS signal divided by the data rate of the initial PPDU. To minimize potential signal interference the IEEE 802.11 standard set the processing gain requirements at 11.

A balanced modulator modulates the spread PPDU by combining the spread PPDU with a carrier. The DSSS PMD transmits the initial PPDU at 1 or 2 Mbps using different modulation types. For 1 Mbps, the PMD uses differential phase shift keying (DBPSK) modulation.

For 2 Mbps, the PMD uses differential quardrature phase shift keying (DQPSK) modulation. In DQPSK 4 level modulation technique double the data rate while maintaining the same baud rate of 1 Mbps signal.

DSSS wireless LANs devices are capable of operating at relatively high data rates. Supporting applications that require more range and bandwidth within a single cell. But DSSS products costing more than other wireless technologies, so that the total prices of the system to be higher than others.

2.3 Indoor RF Propagation

The actual path loss is difficult to calculate for an indoor environment. Because of the variety of physical barriers and material within the indoor structure, the signal does not lose energy as predict. The path between receiver and transmitter is usually block by walls, ceilings and other obstacles. Depending on the building construction and layout, the signal propagation is different for different buildings. In some case, transmitted signals may have a direct path (Line of Sight, LOS) to the receiver. In most cases, the signal is obstructed.

Due to the multipath the signal fading is occur when the different path signals arrive to the antenna with out of phase and they cancel each other out. In an indoor environment, multipath is always present and the signal strength change rapidly over small distance travel. Because of multipath, the signal reduction can be more than 30 dB. Figure 2.1 shows the multipath signals for the indoor radio wave propagation.

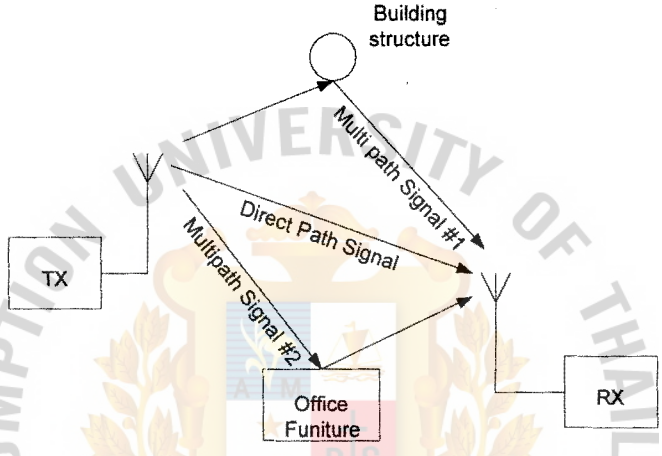

Figure 2.1 LOS and Multipath Signals between Tx and Rx

2.4 Indoor Propagation Loss

Large scale fading analysis is concerned with predicting the mean signal strength as a function of Transmitter–Receiver (T-R) separation with distance (d). Path loss is the term used to quantify the difference (in dB) between the transmitted power, P_t (in dBm) and received power P_r (in dBm). The equation (2.1) used d_n model that predict the mean path loss at T-R separation with distance d.

$$\overline{PL}(d)[dB] = \overline{PL}(d_0)[dB] + 10n\log(\frac{d}{d_0}) \qquad (2.1)$$

Where

PL(d) = Path loss at distance d meter

$PL(d_0)$ = Path loss at distance d_0 meter

n = Path loss exponent or empirical quantity

For n=2 the path loss is same as free space received signal. The reference distance d_0 is chosen to be in the far field of the antenna. At the same time the distance should be chosen close enough to the transmitter so that the multipath and diffraction are negligible and the propagation can be considered as in free space. Typically, d_0 is chosen to be 1 m for indoor environments. $PL(d_0)$ can be calculated as follow

$$\overline{PL}(d_0)[dB] = 20\log(\frac{4\pi d_0}{\lambda}) \qquad (2.2)$$

Where

$$\lambda = \frac{c}{f}$$

λ = The wavelength of transmitted signal

c = The speed of light $3 * 10^8$ m/s

f = The frequency of the transmitted signal in Hz

For 915 MHz wireless LANs application:

$$\lambda = \frac{c}{f} = \frac{3*10^8}{915*10^6} = 0.328m$$

For d_0 =1m and the free pace path loss at 1m can be calculated by using equation (2.2)

$$\overline{PL}(d_0)[dB] = 20\log(\frac{4\pi d_0}{\lambda}) = 31.67dB$$

By using equation (2.1), the comparisons between free space path loss and indoor propagation path loss are shown in figure 2.2. The path loss component n is taken 3 for office environment. From this figure, we can see that the indoor propagation loss has 10 dB more than free space loss for only 10 m distance. This is due to the multipath fading.

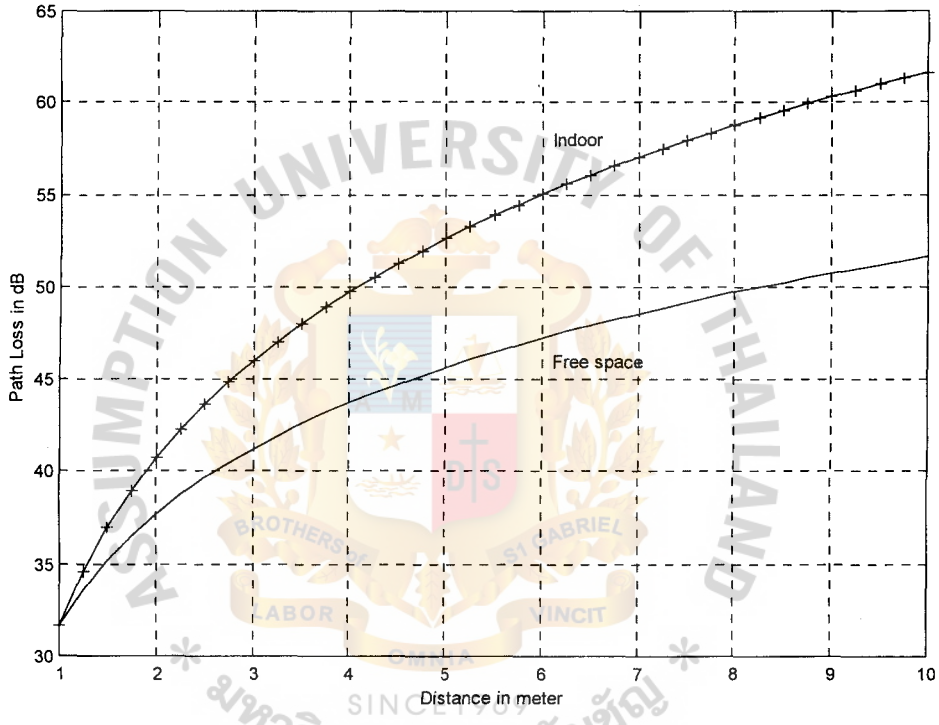

Figure 2.2 Comparison between Free Space and Indoor Propagation Loss

CHAPTER 3. HARDWARE DESIGN

3.1 The Architecture

A basic architecture of Physical Layer for wireless LAN at 915 MHz band RF part is shown as a block diagram in figure 3.1. In this design, single antenna is used although two antennas are supported for diversity to reduce the effects of multipath fading.

In received mode, the signal received from the antenna is applied to the filter FL1. This filter is a two pole dielectric design. It rejects interfered signal outside the 915 MHz ISM Band and provides image rejection.

The output signal of FL1 is fed to the SA630 T/R (Transmitter/Receiver) switch. In received mode, the T/R switch transfers the signal to Low Noise Amplifier (LNA), MAX2630. The output of MAX2630 is fed into three LNAs MAX2631, MAX2630 and MAX2650 one after another.

Next, the amplified signal is filtered by FL2, which is 2-pole monolithic LC bandpass filter used to suppress image noise. The signal then entered to the MAX2681, down converter. High side local oscillator injection is used to mix down to the intermediate frequency (IF), 80 MHz. The output of down converter is filtered by FL3 which is simple LC bandpass filter to suppress the local oscillator noise.

In transmit mode, this design received filtered IF signal and it is fed into the up converter mixer, MAX2661, to convert to 902–928 MHz band. Again high side local oscillator injection is used. The mixer output is filtered with FL4, 2 pole monolithic LC bandpass filter. This filter suppress the local oscillator feed through from the mixer. The filtered signal is amplified by using low noise amplifiers MAX2630 and MAX2650.

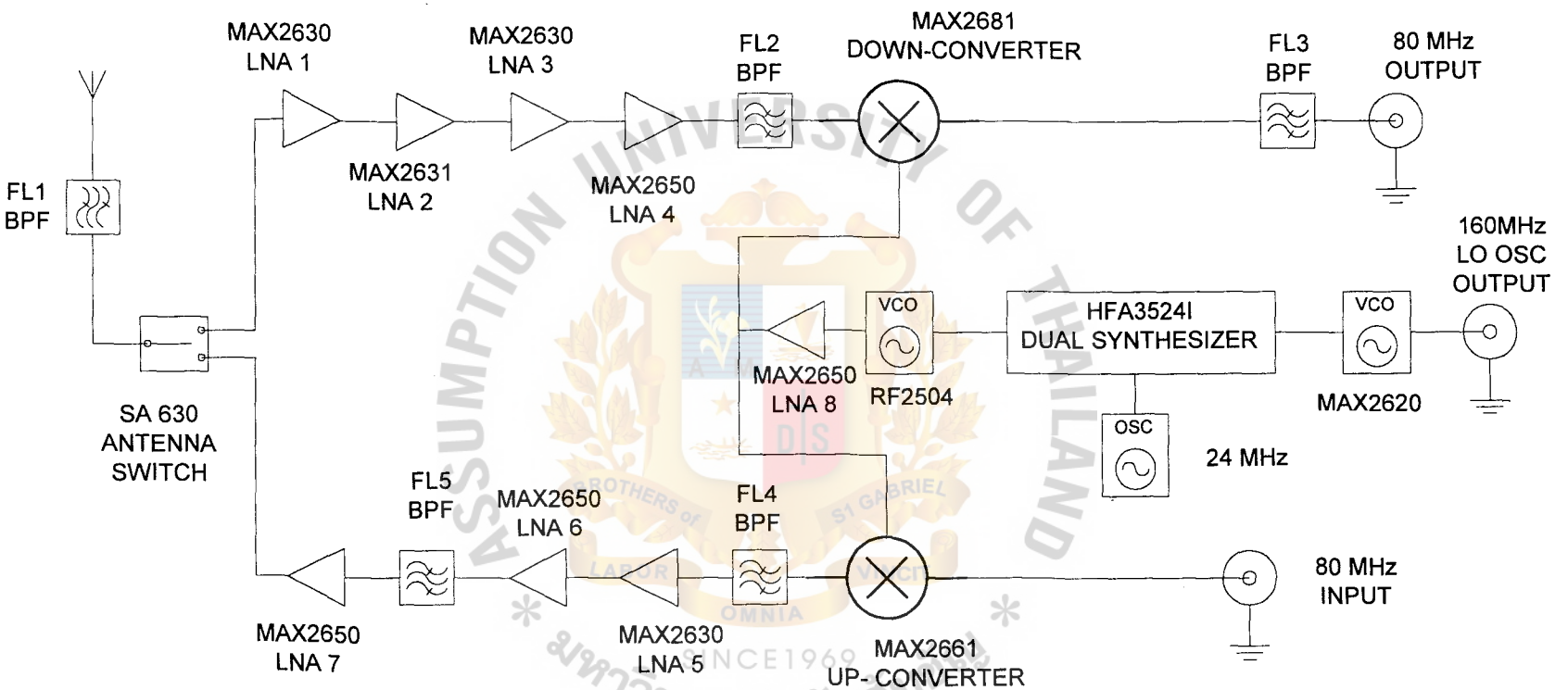

Figure 3.1 Block Diagram for Physical Layer of Wireless LAN RF Part

The amplified signal is filtered again by using FL5 which is two pole dielectric bandpass filter, used to further suppress both transmit local oscillator leakage and undesired sideband.

The filtered signal is amplified by using low noise amplifier MAX2650. This amplified signal is pass through the T/R switch SA630. The output of T/R switch is filter by using FL1 to suppress out of band noise. Finally the filtered signal is transmitted by using monopole antenna.

3.2 Link Budget Calculation

The DSSS system used 11:1 ratio between the chip rate and the data rate. For 2 Mbps data rate, the signal is transmitting 22 Mcps. Because of DQPSK modulation, the occupied bandwidth of the transmitter would be 22 MHz. This 22 MHz is used to calculate the thermal noise floor. The thermal noise floor N of the receiver is

$$N = KT_0BF \tag{3.1a}$$

$$N(dBm) = -174(dBm) + 10\log_{10} B + F(dB) \tag{3.1b}$$

Where

K = $1.38*10^{-23}$ J/K Boatsman's constant

T_0 = 290 K is standard temperature

B = The receiver bandwidth in Hz

F = The noise figure of the receiver in dB

The thermal noise floor for wireless LAN card design can be calculated by using equation (3.1b).

$$\begin{aligned} N(dBm) &= -174(dBm) + 10\log_{10} B + F(dB) \\ &= -174 + 10\log_{10}(22*10^6) + 7.93 \\ &= -92.65\ dBm \end{aligned}$$

By using DQPSK modulation technique the required E_b/N_o to achieve a 10^{-6} BER is 11dB. The required signal-to-noise ratio (SNR) can be calculated by using equation (3.2).

$$\frac{E_b}{N_o} = 11\ dB = 12.59$$

$$SNR = (\frac{E_b}{N_o}) * (\frac{R}{B_T}) \qquad (3.2)$$

$$= 12.59 * (\frac{2Mbps}{2MHz}) = 12.59$$

$$= 11\ dB$$

The receiver sensitivity can be calculated by using equation (3.3).

$$\text{Receiver Sensivity} = P_{rx} = \text{Receiver Noise floor} + SNR \qquad (3.3)$$

$$= -92.65 + 11$$

$$= -81.65\ dBm$$

The path loss PL(d) at 3 m away from the transmitter can be calculated by using equation (2.1).

$$\overline{PL}(d)[dB] = \overline{PL}(d_0)[dB] + 10n\log(\frac{d_1}{d_0})$$

$$= 31.67 + 10 * 3 * \log_{10}(3)$$

$$= 45.98\ dBm$$

To overcome the effect of fading, 30dB is allocated for Fade Margin. The required transmitted power P_{tx} to cover 3 m range could be calculated by using the following equation (3.4).

$$P_{tx} = P_{rx} - G_{tx} - G_{rx} + PL(d) + \text{Fade Margin} \qquad (3.4)$$

$$= -81.65 - 0 - 0 + 45.98 + 30$$

$$= -5.66\ dBm$$

$$= 0.27\ mW$$

3.3 Transmitter Design

The transmitter performance analysis is shown in table 3.1. The function block diagram is described in the left side. Across the top, the parameters lists are shown, including Gain, output P_{1dB} and Power output.

Table 3.1 Stage Properties of Transmitter

	Gain (dB)	OP_{1dB} (dBm)	Power out (dBm)
Input			-53.5
MAX2661 Mixer	7	-6	-46.5
FL4 Murata RF Filter	-3	100	-49.5
MAX2630 LNA 5	13.4	-11	-36.1
MAX2650 LNA 6	18.3	-1	-17.8
FL5 Toko RF Filter	-2	100	-19.8
MAX2650 LNA 7	18.3	-1	-1.5
SA630	-2	33	-3.5
FL1 TOKO RF Filter	-2	100	-5.5
Total	48	-5.12	-5.5

The total gain at the transmitter path, $G_{Tx,TOT}$, can be calculated by using equation (3.5). In this equation all gain are in dB.

$$G_{Tx,TOT}(dB) = G_{mixer} + G_{FL4} + G_{LNA5} + G_{LNA6} + G_{FL5} + G_{LNA7} + G_{ANT\,SW} + G_{FL1} \quad (3.5)$$

$$= 7 - 3 + 13.4 + 18.3 - 2 + 18.3 - 2 - 2$$
$$= 48\,dB$$

Using the total gain in transmitter path, we can get the transmitted output power of –5 dBm for –53.5 dBm input power. The P_{1dB} compression point is the point at which the output power minus the input power in dBm is equal to the small signal power gain minus 1 dB. The output P_{1dB} can be calculated by using equation (3.6). The gain and P_{1dB} in equation (3.6) are linear, not the decibel.

$$OP_{1dB} = \frac{G_{Tx,TOT}}{\frac{G_{mixer}}{P_{1dB\ mixer}} + \frac{G_{mixer} \times G_{FL4}}{P_{1dB\ FL4}} + \frac{G_{mixer} \times G_{FL4} \times G_{LNA5}}{P_{1dB\ LNA5}} + \frac{G_{mixer} \times G_{FL4} \times G_{LNA5} \times G_{LNA6}}{P_{1dB\ LNA6}} \cdots} \cdots$$

$$\cdots \frac{1}{+ \frac{G_{mixer} \times G_{FL4} \times G_{LNA5} \times G_{LNA6} \times G_{FL5}}{P_{1dB\ FL5}} + \cdots} \cdots\cdots \quad (3.6)$$

The output P_{1dB} of all filters is assumed to be100 dBm. By substituting the values in equation (3.6) and we get output P_{1dB} of 0.308 W in linear and –5.12 dBm in decibel. This output P_{1dB} is just above the transmitted output power of –5.5 dBm.

3.4 Receiver Design

The receiver performance is shown in table 3.2. The left column of the table 2 is descriptions of the block in the receiver chain. Each block has typical value for Insertion Loss (IL) or Gain (G), Noise Figure (NF) and output third order intercept point (OIP3) and Power output.

Table 3.2 Stage Properties of Receiver

	Gain (dB)	N.F (dBm)	OIP3 (dBm)	Power (dBm)
Input From Antenna				-81
FL1 TOKO RF Filter	-2	2	100	-83
SA630	-2	2	33	-85
MAX2630 LNA 1	13.4	3.8	-1	-71.6
MAX2631 LNA 2	13.4	3.8	-1	-58.2
MAX2630 LNA 3	13.4	3.8	-1	-44.8
MAX2650 LNA 4	18.3	3.9	10	-26.5
FL2 Murata RF Filter	-3	2	100	-29.5
MAX2681 MIXER	14.2	3.9	4.9	-15.3
FL3 RC BPF	-3	2	100	-18.3
Total	62.7	7.92	1.8	-18.3

The total gain at the receiving path, $G_{Rx,TOT}$ can be calculated by using equation (3.7). In this equation, all gains are in dB.

$$G_{Rx,TOT}(dB) = G_{ANT\,SW} + G_{FL1} + G_{LNA1} + G_{LNA2} + G_{LNA3} + G_{LNA4} + G_{FL2} + G_{mixer} + G_{FL3} \quad (3.7)$$

$$G_{Rx,TOT}(dB) = -2 - 2 + 13.4 + 13.4 + 13.4 + 18.3 - 3 + 14.2 - 3$$
$$= 62.7\ dB$$

The noise figure of the receiver can be calculated by using the equation (3.8). The noise figure for a passive element is equal to its insertion loss. The gain and noise figure of each of the elements in equation (3.8) are linear.

$$NF = NF_{FL1} + \left(\frac{NF_{ANT\,SW} - 1}{G_{FL1}}\right) + \left(\frac{NF_{LNA1} - 1}{G_{FL1} \times G_{ANT\,SW}}\right) + \left(\frac{NF_{LNA2} - 1}{G_{FL1} \times G_{ANT\,SW} \times G_{LNA1}}\right) + \left(\frac{NF_{LNA3} - 1}{G_{FL1} \times G_{ANT\,SW} \times G_{LNA1} \times G_{LNA2}}\right) + \cdots\cdots \quad (3.8)$$

From equation (3.8) we know that the noise figure of the whole system is dominnated by the first element in the chain. By substituting the values in equation (3.8) and we got the noise figure of 6.19 in linear and 7.92 in dBm.

The third order intercept point is the point at which the fundamental response and the thrid order spurious response curve intersect. To reduce third order intermodulation distortion we need higher third order intercept point.The output third order intercept point (OIP3) can be calculated by using equation (3.9a). The gain and OIP3 of each of the element in equation (3.9a) are linear. The input third order intercept point (IIP3) also calculated by using equation (3.9b).

$$OIP3 = \frac{G_{Rx,TOT}}{\frac{G_{FL1}}{OIP3_{FL1}} + \frac{G_{FL1} \times G_{ANT\,SW}}{OIP3_{ANT\,SW}} + \frac{G_{FL1} \times G_{ANT\,SW} \times G_{LNA1}}{OIP3_{LNA1}} + \cdots\cdots} \quad (3.9a)$$

$$IIP3\ (dBm) = OIP3\ (dBm) - G_{RX,TOT}\ (dB) \quad (3.9b)$$

The OIP3 of all filters are assumed to be 100 dBm. By substituting the values in equation (3.9a) and (3.9b), we got the IIP3 of –60.9 dBm.

3.5 Frequency Synthesizer Design

The frequency synthesizers are based on the phase locked loop (PLL) for their operation. A block diagram of a basic phase locked loop is shown in figure 3.2.

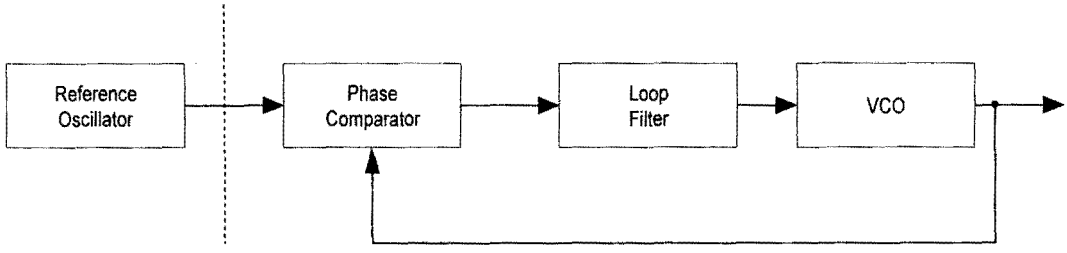

Figure 3.2 Basic Block Diagram for Phase Lock Loop

From the figure 3.2, it can be seen that a basic PLL consists of three main blocks; a voltage controlled oscillator (VCO), loop filter, and a phase comparator. A reference oscillator is also needed, but this is not strictly part of the loop. Within the loop, the key element is the phase comparator. This circuit takes in two signals, compares the phase between them and produces an output voltage proportional to the phase difference between them.

There are two signals entering the phase comparator. One is from the VCO and the other is from the reference. Thus, the output from the phase comparator represents the phase difference between these two signals. This error signal is passed through the loop filter to VCO where it is used to control the VCO frequency. As the voltage is in the correct sense to reduce the phase error between the two signals, it brings the VCO closer in frequency to the reference. When in lock there is a steady state phase error between the two signals. As the phase error is constant, it means that the frequencies of the VCO and reference are exactly the same.

The loop filter fulfils a number of functions. It attenuates the high frequency signals, which would degrade the performance of the loop if they reached the VCO input. The main one is the reference frequency signal. It also controls the stability of the loop. The filter design also affects the phase noise generated by the loop. It also governs the rate at which the loop can change frequency.

In order to be able to use a PLL as a frequency synthesizer a further element is required. If a frequency divider is placed into the loop as shown in figure 3.3, this enables the VCO to run at a different frequency to the phase comparator.

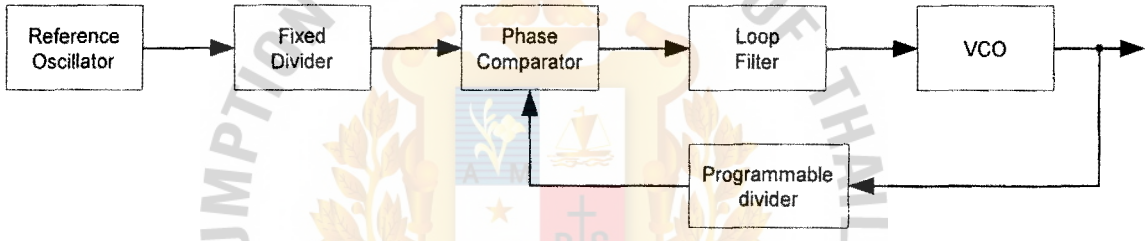

Figure 3.3 Basic Frequency Synthesizer

If the division ratio of the divider is n, then the frequency entering the divider from the VCO will be n times the comparison frequency. The divider in the loop is normally a programmable divider whose ratio can be changed to give the required output frequency. The reference oscillators are normally crystal controlled.

A linear control system model of the phase feedback for a PLL in the locked state is shown in figure 3.4(a). The open loop gain K is the product of the phase detector gain K_{PD}, the VCO gain K_{VCO} /s, and the loop filter gain Z(s). The gain of the feedback is counter of modulus N. The passive loop filter configuration is shown in figured 3.4(b).

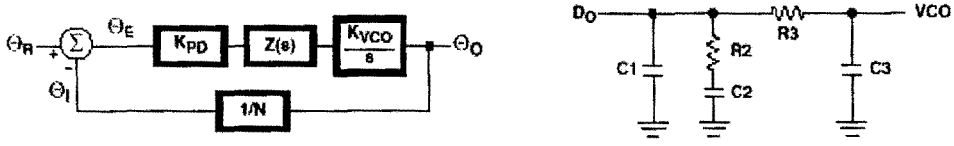

Figure 3.4 (a) PLL Linear Model (b)Passive Loop Filter.

3.5.1 Local Oscillator 1 (RF LO, 995 MHz) Design

The mixers in this design used high side local oscillator injection. For 915 MHz RF and 80 MHz IF, the required local oscillator is 995 MHz. The following steps are shown how to calculate loop filter for 995 MHz local oscillator.

f_{Loop} = The desired loop bandwidth = 5 kHz

f_{ref} = The reference frequency of the loop = 1 MHz

ϕ = The desired phase margin of the PLL = 50°

K_{VCO} = The VCO tuning Voltage constant = 4.7 MHz / V

K_{PD} = The phase detector pump constant = 0.004

N = The divider ratio = 995

$\omega_L = 2\pi f_{Loop} = 6.283*10^4$ rad/s

$\omega_{ref} = 2\pi f_{ref} = 6.283*10^6$ rad/s

$K_{VCO} = 4.7*10^6 * 2\pi = 29.53*10^6$ rad/s – V

$K_{PD} = 0.004 / 2\pi = 6.366*10^{-4}$ rad/s

The time constants T_3, T_1 and T_2 can be calculated by using equation (3.10), (3.11) and (3.13) respectively.

$$T_3 = \frac{1}{10\omega_L} \qquad (3.10)$$

$$T_3 = 3.183*10^{-6}\,s$$

$$T_1 = \frac{\sec(\phi) - \tan(\phi)}{1.414 * \omega_L} \tag{3.11}$$

$$T_1 = 8.136 * 10^{-6} s$$

Gain cross over frequency f_c is approximately equal to the loop bandwidth f_{loop}. Then

$$\omega_c = \omega_L \tag{3.12}$$

$$T_2 = \frac{1}{\omega_C^2 * (T_1 + T_3)} \tag{3.13}$$

$$T_2 = 8.951 * 10^{-5} s$$

C_1 and C_2 can be calculated by using equation (3.14) and (3.15) respectively.

$$C_1 = \left[\frac{T_1 * K_{PD} * K_{VCO}}{N * T_2 * \omega_C^2} \right] * \sqrt{\frac{1 + (\omega_C * T_2)^2}{[(1 + (\omega_C * T_1)^2) * (1 + (\omega_C * T_3)^2)]}} \tag{3.14}$$

$$C_1 = 5.006 * 10^{-9} F$$

$$C_2 = C_1 \left[\left(\frac{T_2}{T_1} \right) - 1 \right] \tag{3.15}$$

$$C_2 = 5.007 * 10^{-8} F$$

R_2 can be calculated by using equation (3.16).

$$T_2 = R_2 \cdot C_2 \tag{3.16}$$

$$R_2 = \frac{T_2}{C_2} = 1.787 * 10^3 \Omega$$

Loop filter components Values are

C_1 = 5600 pF C_2 = 0.056 μF R_2 = 1.8 kΩ

Choose $R_3 < 2*R_2$ then R_3= 3.6 kΩ

$$T_3 = R_3 \cdot C_3 \tag{3.17}$$

$$C_3 = \frac{T_3}{R_3} = 884pF$$

Choose C_3=1000 pF and R_3 = 3.3 kΩ

The transfer function of the loop filter Z(s) is shown in equation (3.18).

$$Z(s) = \frac{(1+sT_2)\times(1+sT_3)}{s\left[C_1T_2T_3s^2 + s\left(C_1T_2 + C_1T_3 + C_2T_3 + C_3T_2\right) + \left(C_1 + C_2 + C_3\right)\right]} \tag{3.18}$$

By substituting the component values and time constants, the transfer function of loop filter Z(s) becomes

$$Z(s) = \frac{(5.368\times10^{17})\times(1+1.008\times10^{-4}s)\times(1+3.3\times10^{-6}s)}{s(s+3.772\times10^{5})\times(s+0.891\times10^{5})}$$

and the open loop gain GH(s) of the PLL can be calculated by using equation (3.19).

$$GH(s) = \frac{K_{PD}\times K_{VCO}\times Z(s)}{s\times N} \tag{3.19}$$

$$GH(s) = \frac{(1.014\times10^{19})\times(1+1.008\times10^{-4}s)\times(1+3.3\times10^{-6}s)}{s^2(s+3.772\times10^{5})\times(s+0.891\times10^{5})}$$

By using MATLAB program we can get the bode plot for the open loop gain of frequency synthesizer. This bode plot is shown in figure 3.5. From this bode plot we can get phase margin of 54.21°and which is satisfied for initial value of 50°. And we can also get the gain cross over frequency of 30352 rad/sec (4.83 kHz) from the graph. This value is equal to the loop bandwidth and which is also close with the design value of 5 kHz.

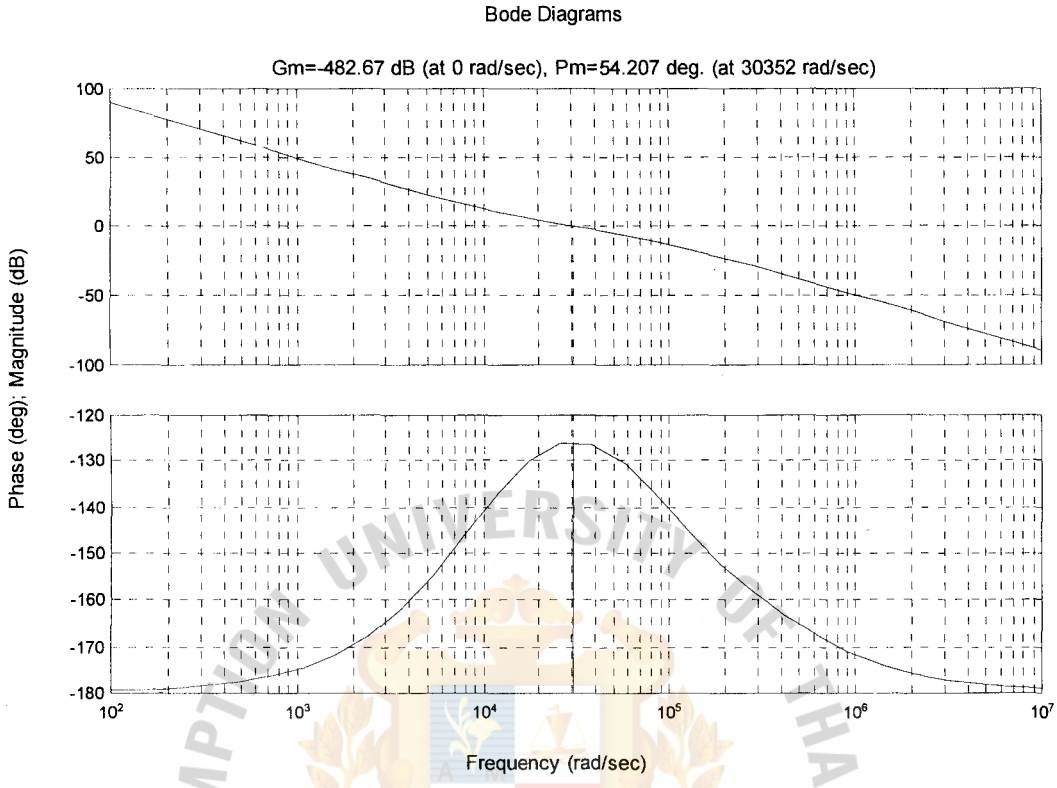

Figure 3.5 Bode Diagram for the RF PLL

3.5.2 Local Oscillator 2 (2 * IF LO, 160 MHz) Design

The two times IF local oscillator is used in basedband modulation to convert from basedband signal to IF signal. The following steps are shown how to calculate loop filter for 160 MHz local oscillator.

f_{Loop} = The desired loop bandwidth =5 kHz

f_{ref} = The reference frequency of the loop = 1 MHz

ϕ = The desired phase margin of the PLL = 50°

K_{VCO} = The VCO tuning Voltage constant = 11 MHz/V

K_{PD} = The phase detector pump constant = 0.004

N = The divider ratio = 160

$\omega_L = 2\pi f_{Loop} = 6.283*10^4$ rad/s

$\omega_{ref} = 2\pi f_{ref} = 6.283*10^6$ rad/s

$K_{VCO} = 11*10^6 * 2\pi = 4.46*10^5$ rad/s – V

$K_{PD} = 0.004 /2\pi = 6.366*10^{-4}$ rad/s

The time constants T_3, T_1 and T_2 can be calculated by using equation (3.10), (3.11) and (3.13) respectively. Euqation (3.12) is also used to apprroximate $\omega_C = \omega_L$.

$$T_3 = \frac{1}{10\omega_l} = 3.183*10^{-6} s$$

$$T_1 = \frac{\sec(\phi) - \tan(\phi)}{1.414 * \omega_L} = 8.136*10^{-6} s$$

$$T_2 = \frac{1}{\omega_C^2 * (T_1 + T_3)} = 8.951*10^{-5} s$$

C_1 and C_2 can be calculated by using equation (3.14) and (3.15) respectively.

$$C_1 = \left[\frac{T_1 * K_{PD} * K_{VCO}}{N * T_2 * \omega_C^2}\right] * \sqrt{\frac{1 + (\omega_C * T_2)^2}{[(1 + (\omega_C * T_1)^2) * (1 + (\omega_C * T_3)^2)]}} = 7.287*10^{-8} F$$

$$C_2 = C_1\left[\left(\frac{T_2}{T_1}\right) - 1\right] = 7.287*10^{-7} F$$

R_2 can be calculated by using equation (3.16).

$$R_2 = \frac{T_2}{C_2} = 122.8\,\Omega$$

Loop filter components Values are

C_1 = 0.068 μF C_2 = 0.68 μF R_2 = 130 Ω

Choose $R_3 < 2*R_2$ then R_3= 260 Ω

C_3 can be calculated by using equation (3.17) as follow

$$C_3 = \frac{T_3}{R_3} = 0.011\mu F$$

Choose R_3 = 270 Ω and C_3 = 0.01 μF

The transfer function of loop filter Z(s) can be calculated by using equation (3.18) and we can get the following

$$Z(s) = \frac{(1.161\times10^{16})\times(1+8.84\times10^{-5}s)\times(1+2.7\times10^{-6}s)}{s(s+4.441\times10^{5})\times(s+1.052\times10^{5})}$$

and the open loop gain GH(s) of the PLL can be calculated by using equation (3.19).

$$GH(s) = \frac{(1.694\times10^{19})\times(1+8.84\times10^{-5}s)\times(1+2.7\times10^{-6}s)}{s^2(s+4.441\times10^{5})\times(s+1.052\times10^{5})}$$

By using MATLAB program we can get the bode plot for the open loop gain of frequency synthesizer. This bode plot is shown in figure 3.6. From this bode plot we can get phase margin of 54.46°and which is satisfied for initial value of 50°. And we can also get the gain cross over frequency of 32485 rad/sec (5.22 kHz) from the graph. This value is equal to the loop bandwidth and which is also close with the design value. of 5 kHz.

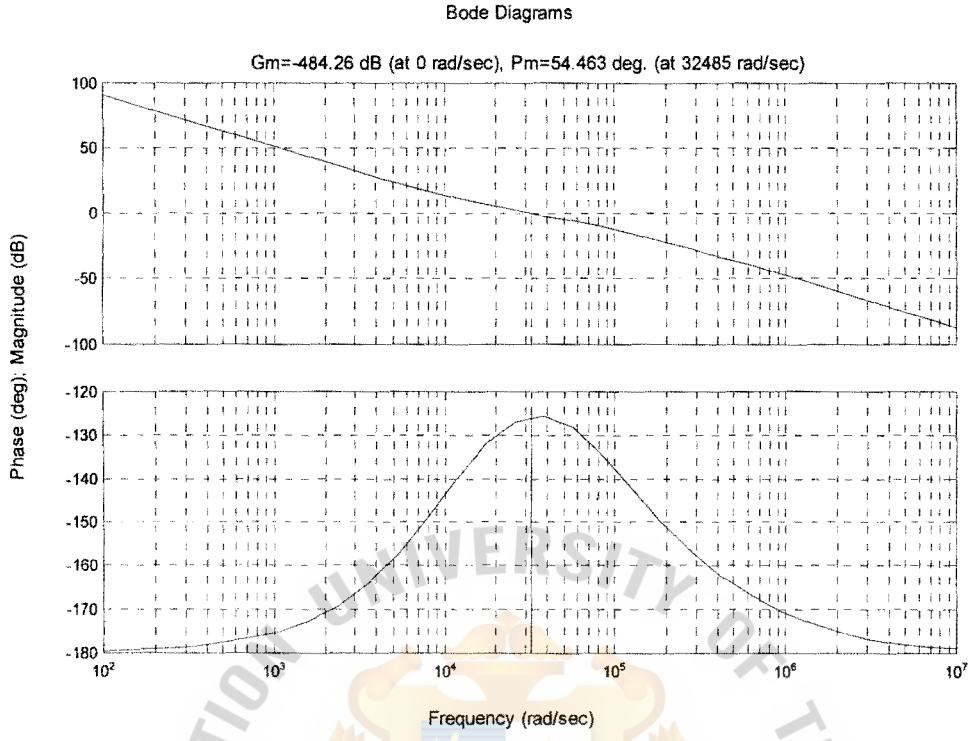

Figure 3.6 Bode Diagram for IF PLL

3.5.3 VCO Tuning Circuit Design for 995 MHz

The 995 MHz VCO tuning circuit diagram is shown in figure 3.7. This tuning circuit is placed between loop filter and VCO.

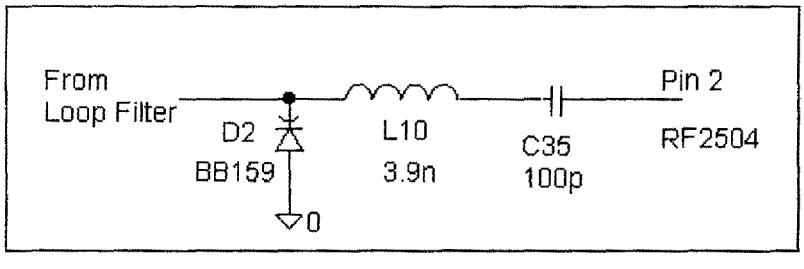

Figure 3.7 VCO Tuning Circuit for 995 MHz

The 995 MHz VCO frequency can be calculated by using the equation (3.20).

$$f_O = \frac{1}{2\pi\sqrt{L_{10}(C_D + C_{IN})}} \tag{3.20}$$

Where

f_0 = Oscillating frequency of VCO

L_{10} = Tunning inductor

C_D = Varactor capacitance

C_{IN} = Input capacitance at pin 2 of VCO

The input capacitance C_{IN} is given by data sheet as 1 pF. The following equation can be used to find the varactor capacitance range.

$$\text{Capacitance ratio } CR = \frac{C_{D(V\,\text{min})}}{C_{D(V\,\text{max})}} = \left(\frac{V_{\text{max}}}{V_{\text{min}}}\right)^{\rho} \tag{3.21}$$

Where

ρ = capacitance exponents

$C_{D\,(Vmax)}$= Capacitance value at maximum varactor voltage

$C_{D(Vmin)}$= Capacitance value at minimum varactor voltage

From the data sheet we can get $C_{D\,(Vmax)}$= 1.9 ~ 2.25 at V_{max}=28 V. By using equation (3.21) we can get capacitace ratio ρ and varactor capacitance value $C_{D(Vmin)}$ at $V_{(min)}$ = 1 V.

ρ = 0.69; $C_{D(Vmin)}$ = 20 pF (@ 1 V)

By substituting maximum and minimum C_D values to the equation (3.20) and we got the VCO tunning range from 1.47 GHz to 556 MHz. The required 995 MHz frequency can be obtained from C_D = 5.6 pF.

3.5.4 VCO Tuning Circuit Design for 160 MHz

The 160 MHz VCO tuning circuit is shown in figure 3.8. This tuning circuit is placed between loop filter and 160 MHz VCO.

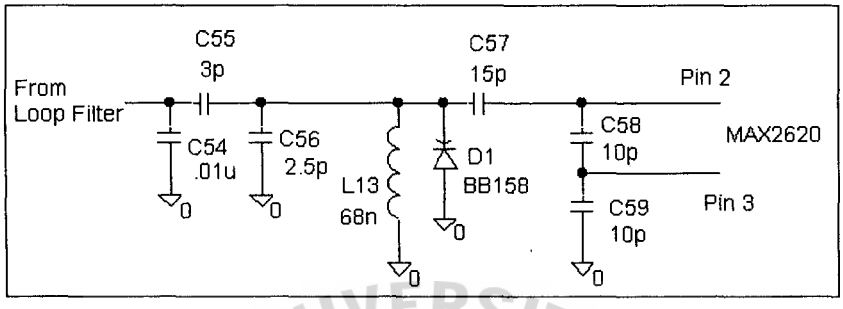

Figure 3.8 VCO Tuning Circuit for 160 MHz

The 160 MHz VCO frequency can be calculated by using the following equation.

$$f_O = \frac{1}{2\pi\sqrt{L_{13}\left[C_{STRAY} + \left(\frac{C_{55} \times C_D}{C_{55} + C_D}\right) + C_{56} + \frac{(C_{58} + C_{03})(C_{59} + C_{04})}{C_{58} + C_{03} + C_{59} + C_{04}}\right]}} \qquad (3.22)$$

Where

f_0 = Oscillating frequency of VCO

C_D = Varactor capaccitance

C_{STRAY} = Approximate stray capacitance of PCB

C_{03} = Input capacitance at the pin 3 of VCO

C_{04} = Input capacitance at the pin 4 of VCO

Other components are refered to figure 3.8. Stray capacitance value is approximated as 3.5 pF. The input capacitance of the MAX2620 (C_{03}, C_{04}) are given as 2.4 pF by data sheet.

From the data sheet we can get $C_{D\,(Vmax)}$= 2.4~2.75 at V_{max}=28 V. By using equation (3.21) we can get capacitace ratio ρ and varactor capacitance value $C_{D(Vmin)}$ at $V_{(min)}$ = 1 V.

ρ = 0.813; $C_{D(Vmin)}$ = 37.5 pF (@ 1 V)

By substituting maximum and minimum C_D values to the equation (3.22) and the tunning range of the VCO can be obtained between 165.9 MHz to 157.7 MHz. The required 160 MHz frequency can be obtained from C_D = 10.9 pF.

3.6 Frequency Synthesizer Simulation Results

The simulation for the frequency synthesizer PLL is done by using symphony Ver 8.0 from Ansoft. The following block diagram is a synthesizer PLL for simulation

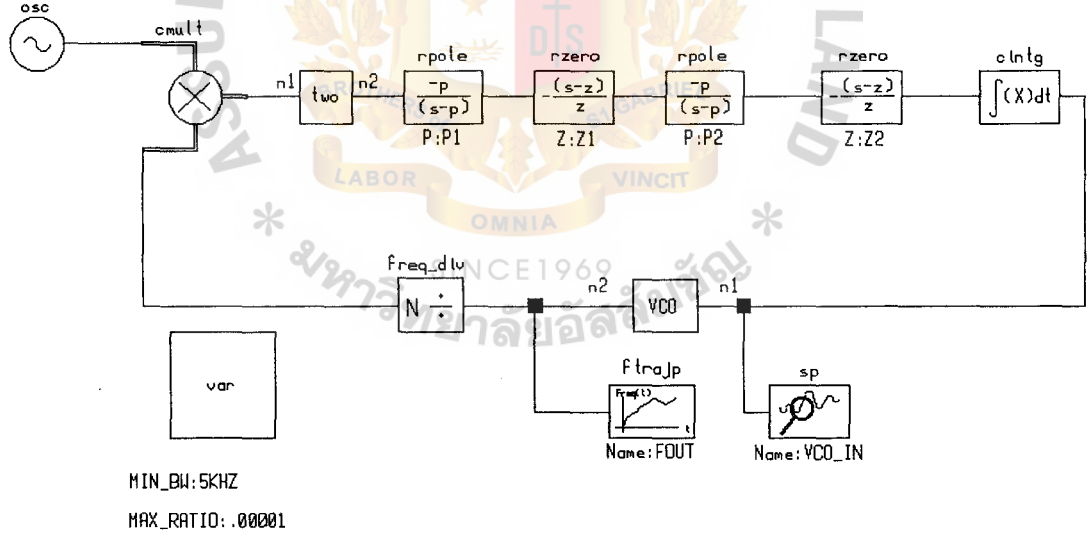

Figure 3.9 Block Diagram of PLL Synthesizer for Simulation

The phase detector is a complex multiplier element (CMULT) in the block diagram. A simple two port black box is placed after the complex multiplier in the

loop. The third order loop low-pass filter in this system is described by the transfer function where 1/s represents the complex integrator element (CINTG), P1 and P2 are the poles, Z1 and Z2 are the zeros of the loop filter.

The frequency divider (feedback transfer function H(s)=1/N) is placed at the output of VCO and the output of divider is fed into the phase detector. There are two probe elements placed in the PLL synthesizer simulation block diagram: (1) Signal Probe for VCO tuning voltage (VCO_IN) placed at the input to the VCO. (2) Frequency Trajectory probe for measuring VCO output frequency (FOUT) versus time.

Figure 3.10 is the blcok diagram of 995 MHz RF PLL for simulation. Pole and zero locations are calculated from equation (3.18). Figure 3.11 and 3.12 show the locking behavior of the VCO tunning voltage and output frequency of RF PLL verses time respectively. PLL locks at 990 MHz with a VCO tunning voltage of 2.78 V. The locking time is approximately 130 μsec and the frequency swing is about 60 MHz.

Figure 3.13 is the block diagram of 160 MHz PLL. From equation (3.8) we can get ploe and zero locations. Figure 3.14 and 3.15 show the locking behavior of the VCO tunning voltage and output frequency of 160 MHz PLL verses time respectively. PLL locks at 160 MHz with a VCO tunning voltage of 0.5 V. The locking time is approximately 100 μsec and the frequency swing is about 20 MHz.

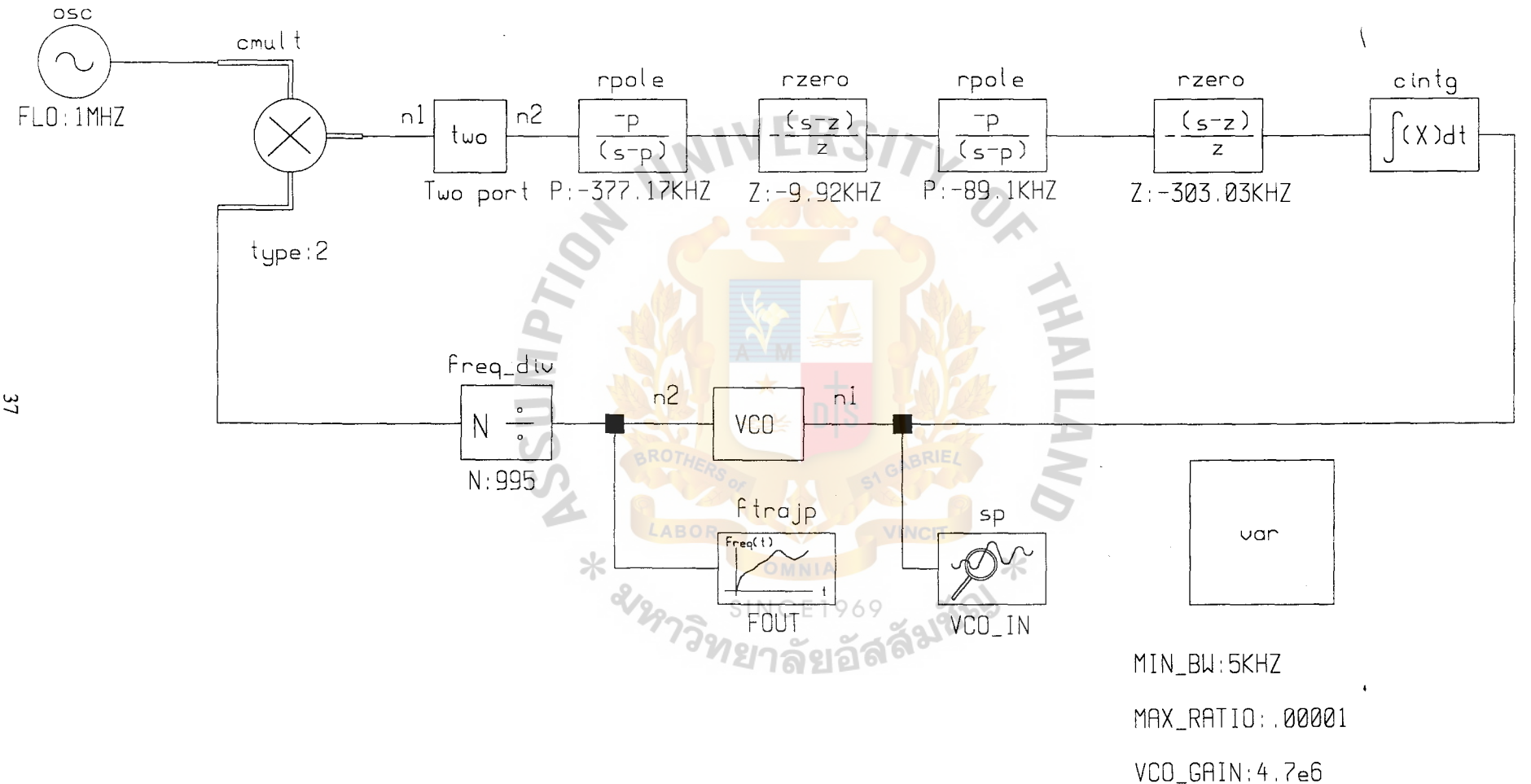

Figure 3.10 Block Diagram for 995 MHz Synthesizer

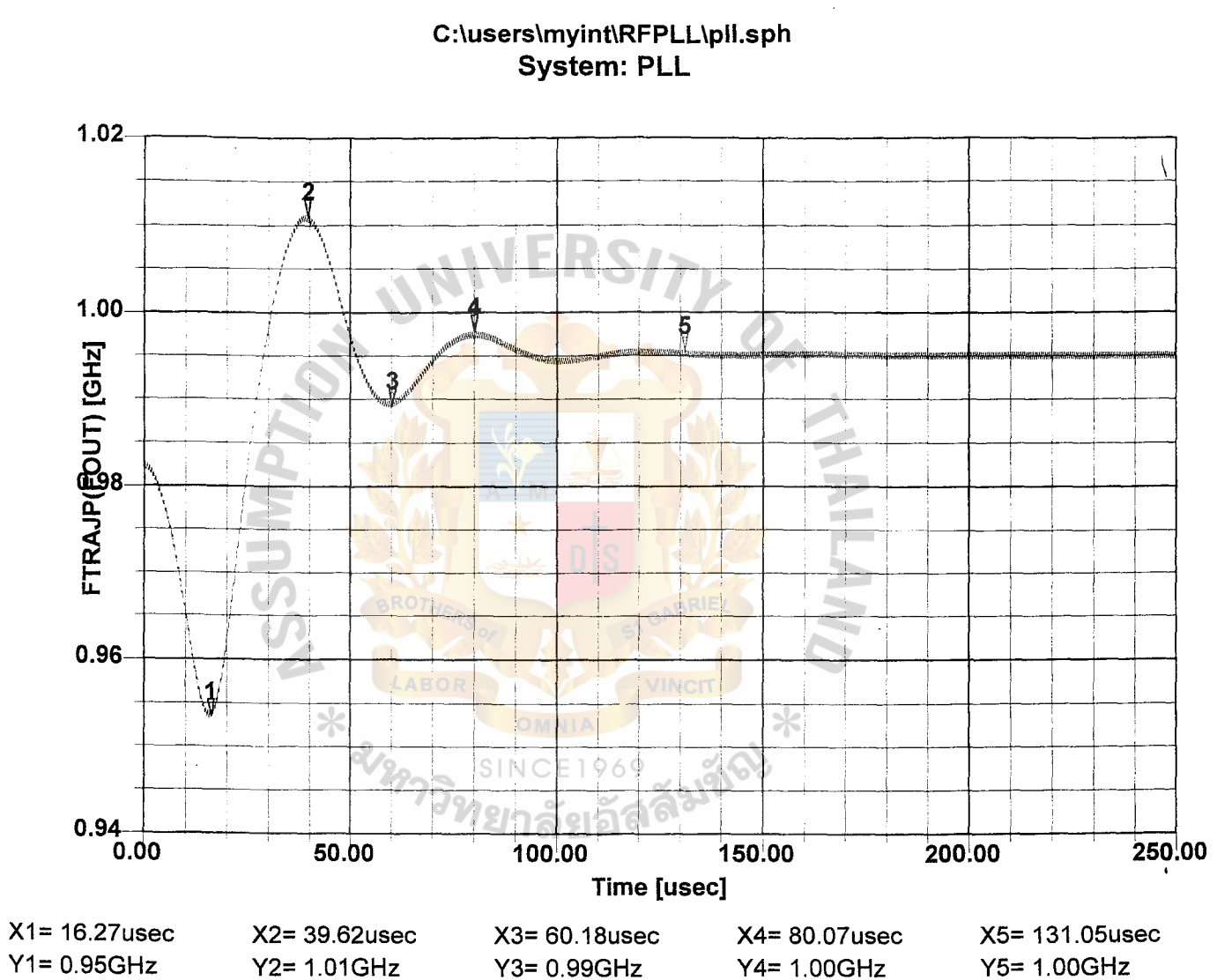

Figure 3.11 The Frequency Output vs. Time for 995 MHz

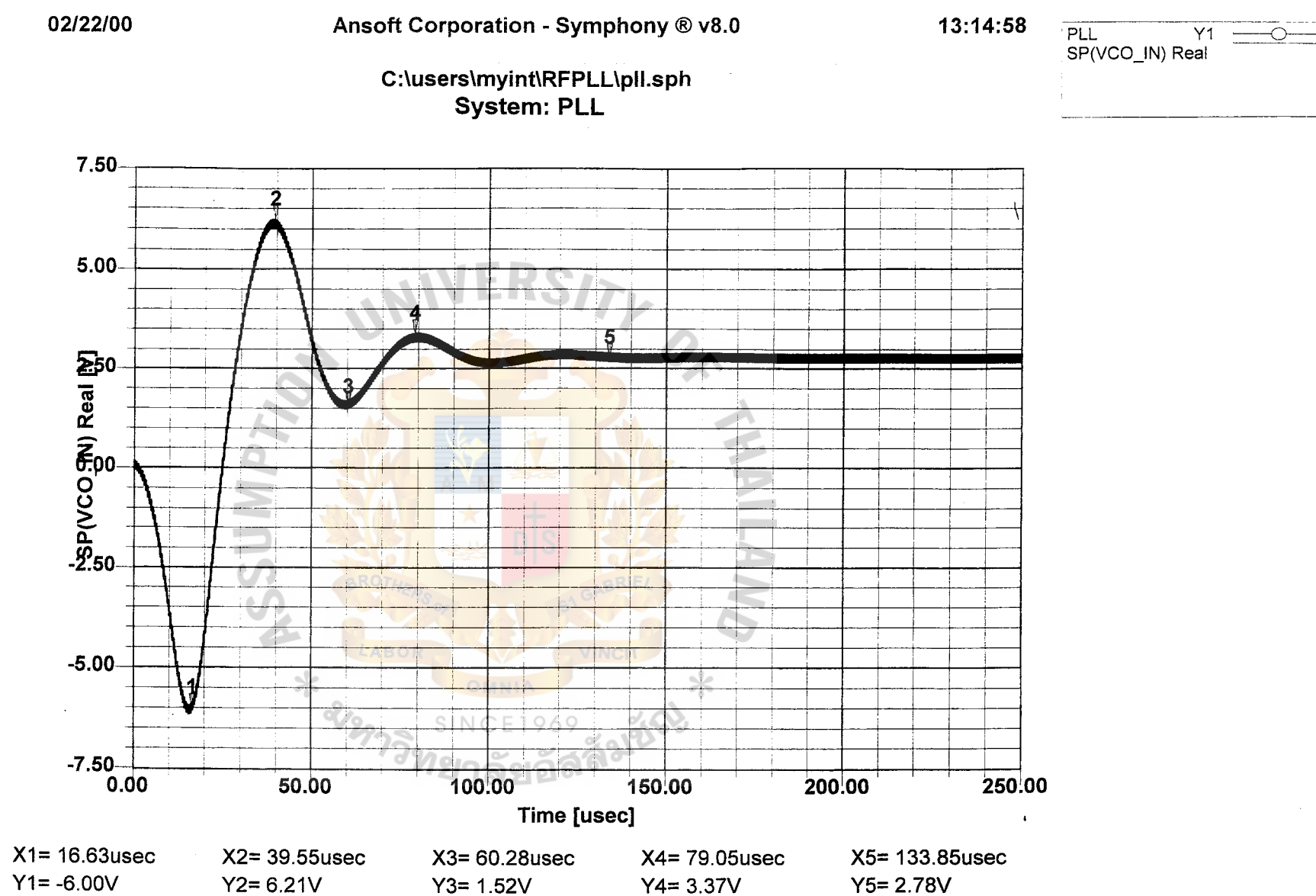

Figure 3.12 The Voltage at VCO Input vs. Time for 995 MHz

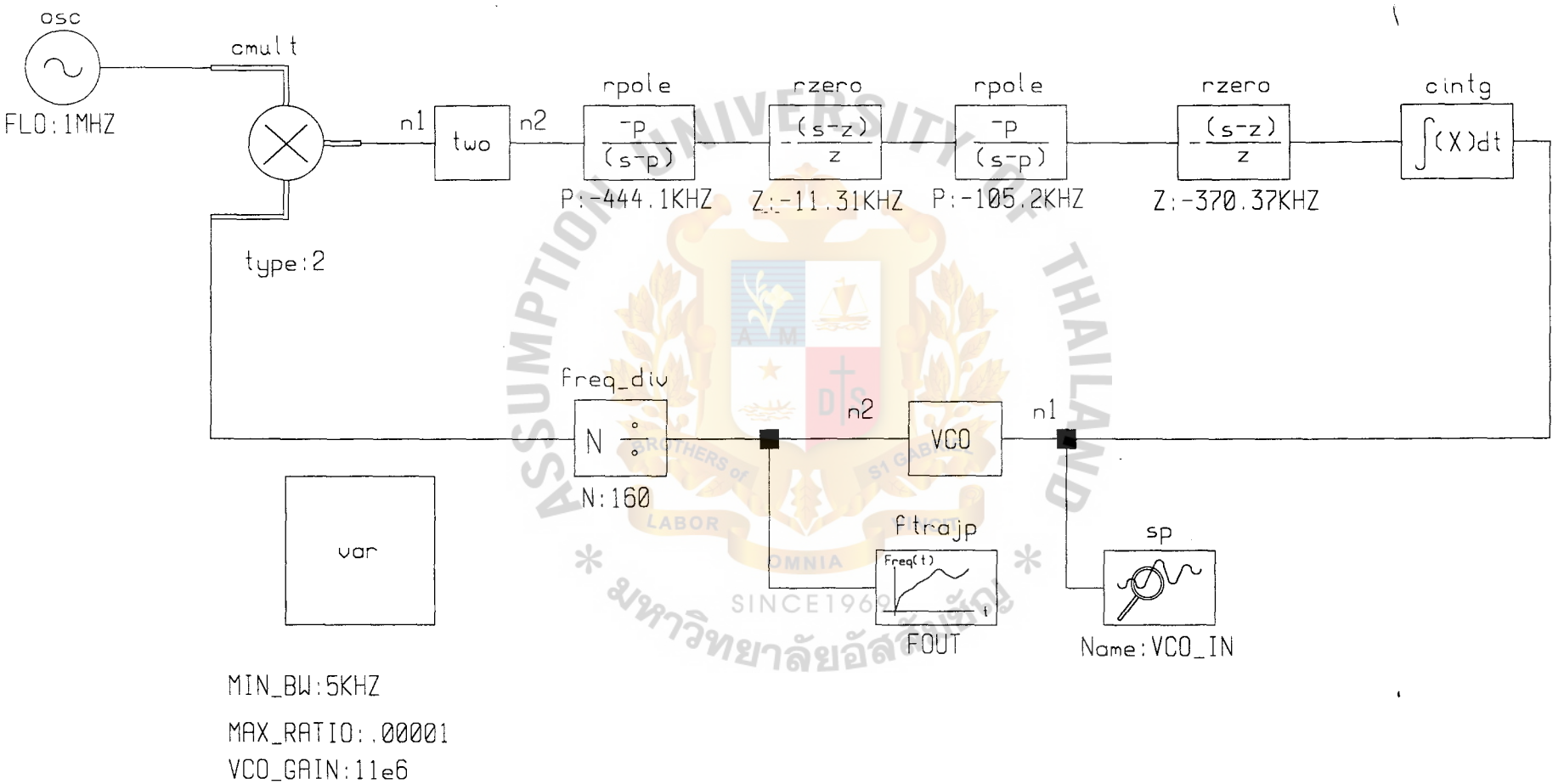

Figure 3.13 Block Diagram for 160 MHz Synthesizer

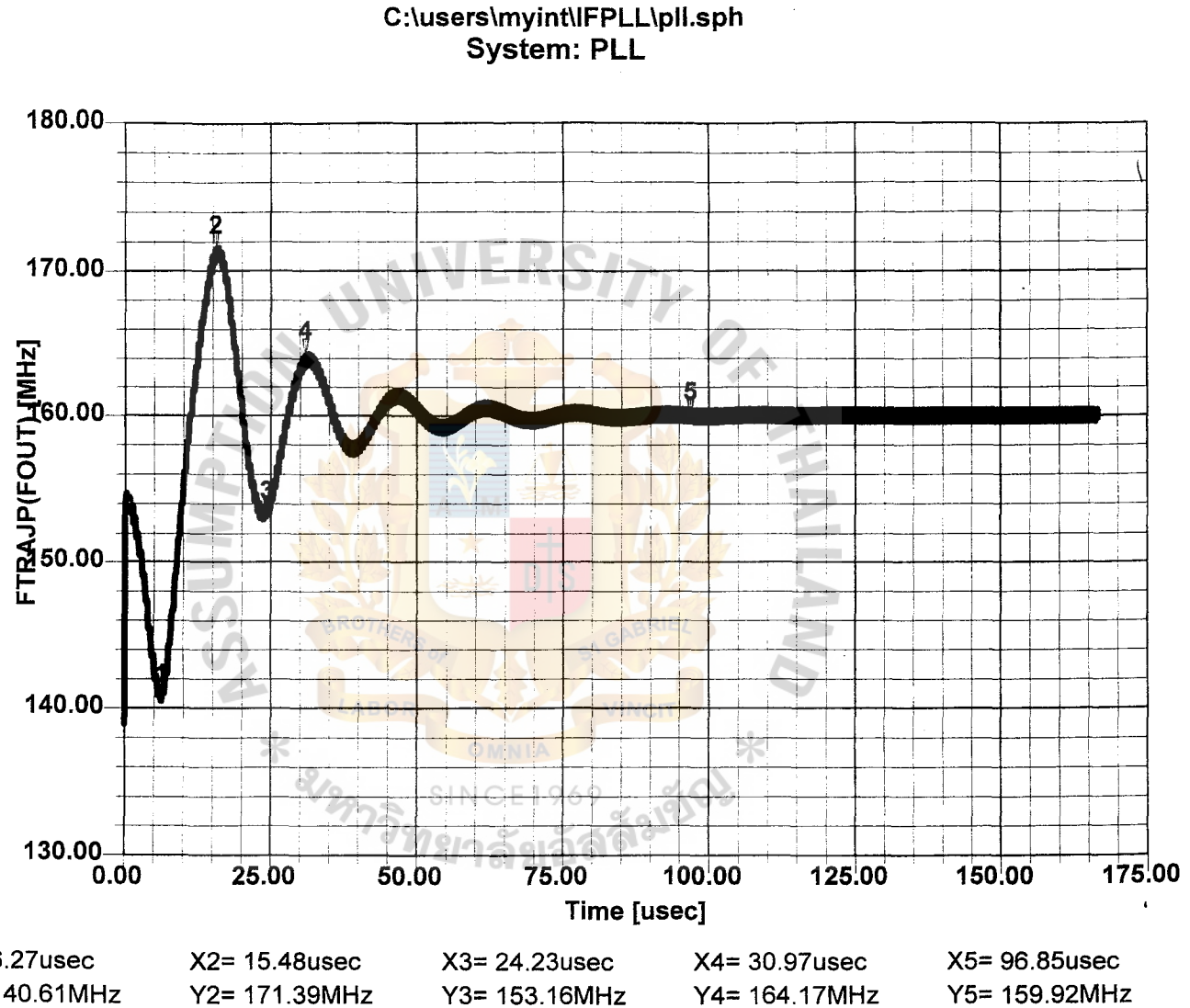

Figure 3.14 The Frequency Output vs. Time for 160 MHz

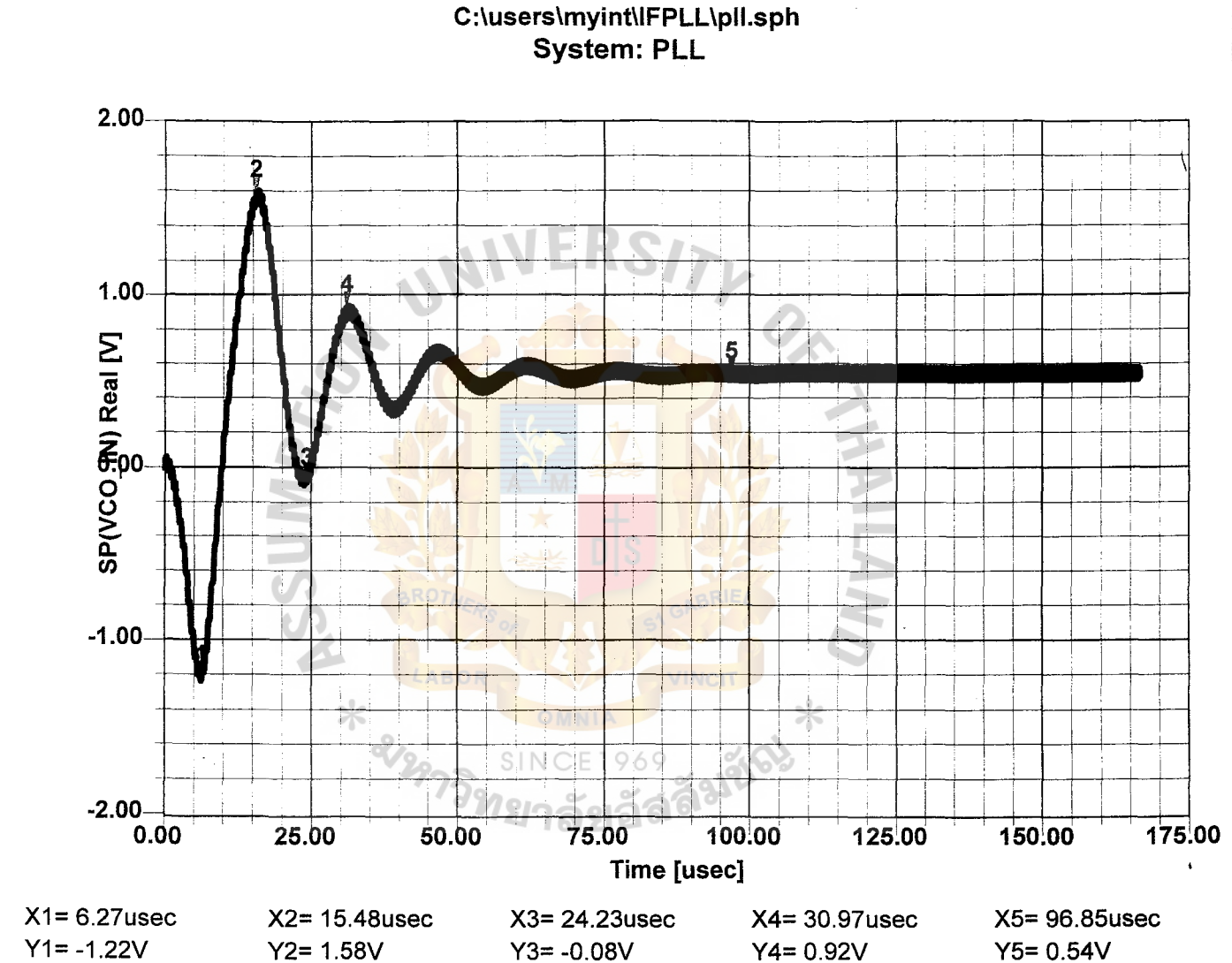

Figure 3.15 The Voltage at VCO Input vs. Time for 160 MHz

3.7 Miscellaneous Components

In this design, all Low Noise Amplifiers need to use DC blocking capacitors at the input and output port. But these capacitors must be large enough to contribute negligible reactance in a 50 Ω system at the minimum operating frequency. The following equation can be used to calculate these capacitors

$$C_{BLOCK} = \frac{53{,}000}{f}\ pF \tag{3.23}$$

Where

f = minimum operating frequency in MHz

Using equation (3.23) we get the DC blocking capacitors of 53.26 pF and used 56pF. For most of the bypass capacitors in this design used 0.1 μF. Use TTL 7404 inverter to control transmit and receive mode. External signal is needed to switch between transmit and received mode.

3.8 Schematic Diagram and PCB Design

The complete schematic diagram for physical layer of wireless LAN at 915 MHz RF part is shown in figure 3.16. The two layers PCB for this schematic is shown in figure 3.17 and 3.18, top layer and bottom layer of PCB respectively.

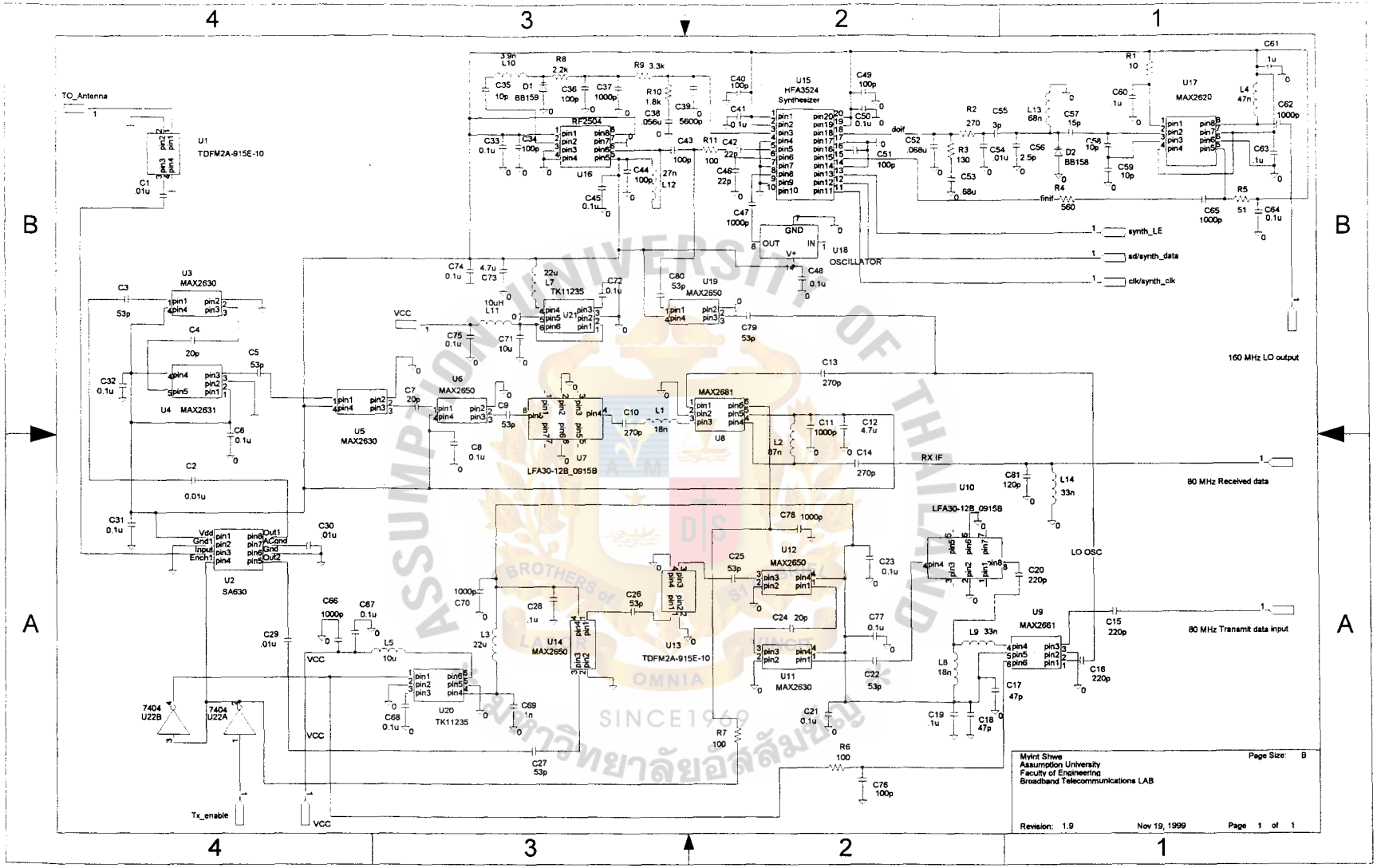

Figure 3.16 Physical Layer of Wireless LAN RF Part Schematic Diagram

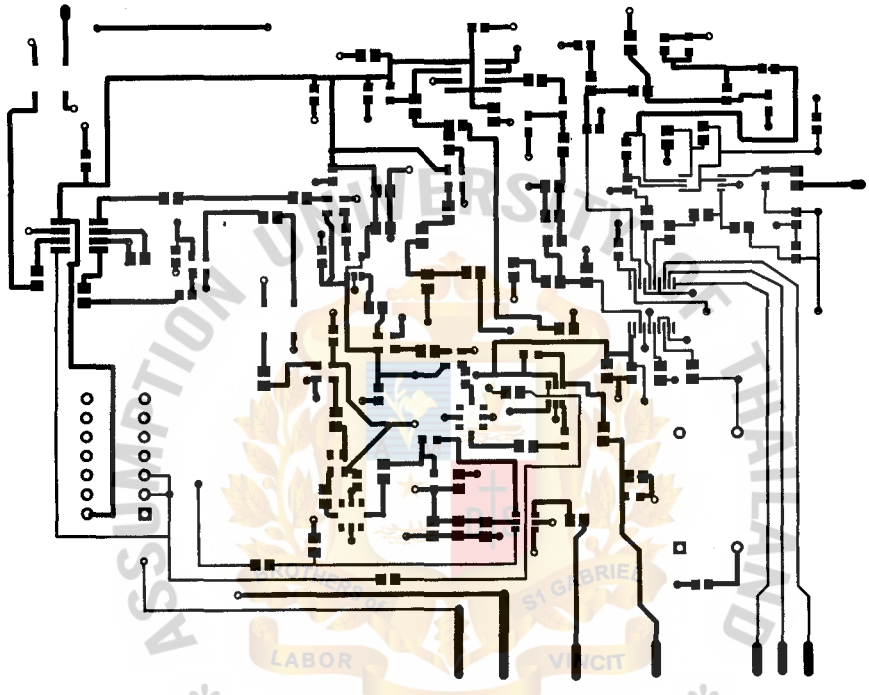

Figure 4.17 Top Layer PCB Layout

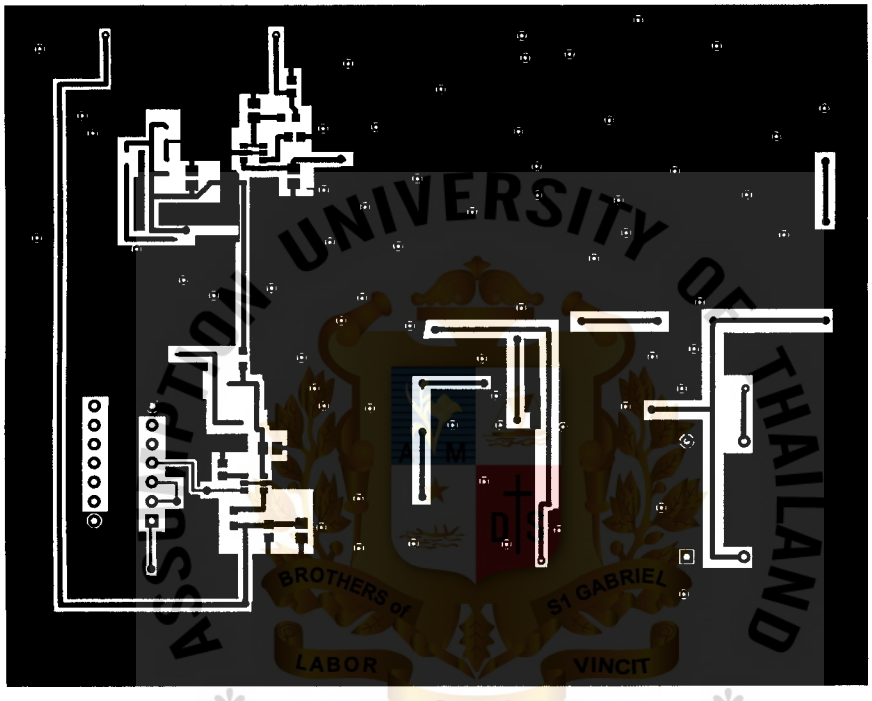

Figure 3.18 Bottom Layer PCB Layout

CHAPTER 4. MEASUREMENTS

There are four different types of signals that can be measured from this design card. These include: two times 80 MHz (160 MHz) IF local oscillator output, 995 MHz RF local oscillator output, 915 MHz transmitted signal at the antenna port and 80 MHz received signal at IF port.

The two times IF local oscillator output power spectrum are shown in figure 4.1 with 3 MHz frequency span, and figure 4.2 with 860 MHz frequency span. That frequency is used in upconverter to get 80 MHz IF signal. From figure 4.1, we can get the local oscillator output power of –13 dBm and it also shows the two reference frequency noises. The reference frequency suppression can get 62 dB. We can also see the harmonic components of 160 MHz frequency in figure 4.2. A third harmonic is the most dominant in the output and has –20 dBm.

The 995 MHz RF local oscillator output power spectrum are shown in figure 4.3 with 20 MHz frequency span and figure 4.4 with 3 GHz frequency span. From figure 4.3, we can get the local oscillator output power of –18 dBm and we can see noise in the output spectrum. Figure 4.4 shows harmonic components and second harmonic is the most dominant and has –39 dBm.

4.1 Measured by using Carrier Input Signal

In this measurement carrier frequency is used to simulate as the input signal for transmit and transmit mode. This carrier frequency is generated by using RF signal generator.

For transmit mode measurements, 80 MHz with power of –20 dBm carrier signal is send to the IF port and measured at the antenna port by using spectrum analyzer. The output spectrum are shown in figure 4.5 with 30 MHz frequency span and figure 4.6 with 200 MHz frequency span. Form figure 4.5 we can get –4 dBm transmitted power. From figure 4.6, we can see the local oscillator leakage noise and some other noises.

Two different types of measurement have done for the receiver mode measurements. For the first method, the RF generator is directly connected to the antenna port and generates 915 MHz carrier frequency with –20 dBm. The 80 MHz frequency is come out from the IF port and this output is measured by spectrum analyzer. The output of 80 MHz IF port is shown in figure 4.7 with 30 MHz frequency span and figure 4.8 with 3.57 GHz frequency span. From these figures, we can see the noise generated by the RF local oscillator 995 MHz.

For the second method, two circuit boards are used one as a transmitter and another as a receiver. The maximum distance that the two system can be away form each other is 1 m only, which is different from the original design. The 80 MHz with –20 dBm of carrier signal is fed to the transmitter card. The output of transmitter card is 915 MHz with –4 dBm. This signal is transmitted by using monopole antenna. This transmitted signal is received by monopole antenna of receiver card. The 80 MHz output of receiver card is measured by using spectrum analyzer and results are shown in figure 4.9 with 24 MHz frequency span and figure 4.10 with 3.55 GHz frequency span.

We can see a lot of noise on the received signal dominated by RF local oscillator frequency of 995 MHz.

4.2 Measured by Using Spread Spectrum Input Signal

In this measurement, 22 MHz spread spectrum signal is used as an input signal. This input spread spectrum signal is shown in figure 4.11.

For transmit mode measurement, -15 dBm spread spectrum signal with 80 MHz center frequency is applied to the antenna port and measurement is done at the antenna port. The measured spectrum is shown in figure 4.12.

In received mode measurement, the above transmitted signal is measured 30 cm away from the transmitter by using monopole antenna. The measured spectrum is shown in figure 4.13. The maximum received signal strength is –40 dBm. This signal is send to the receiver card and measurement is done at the 80 MHz receiver port. The output spectrum is shown in figure 4.14.

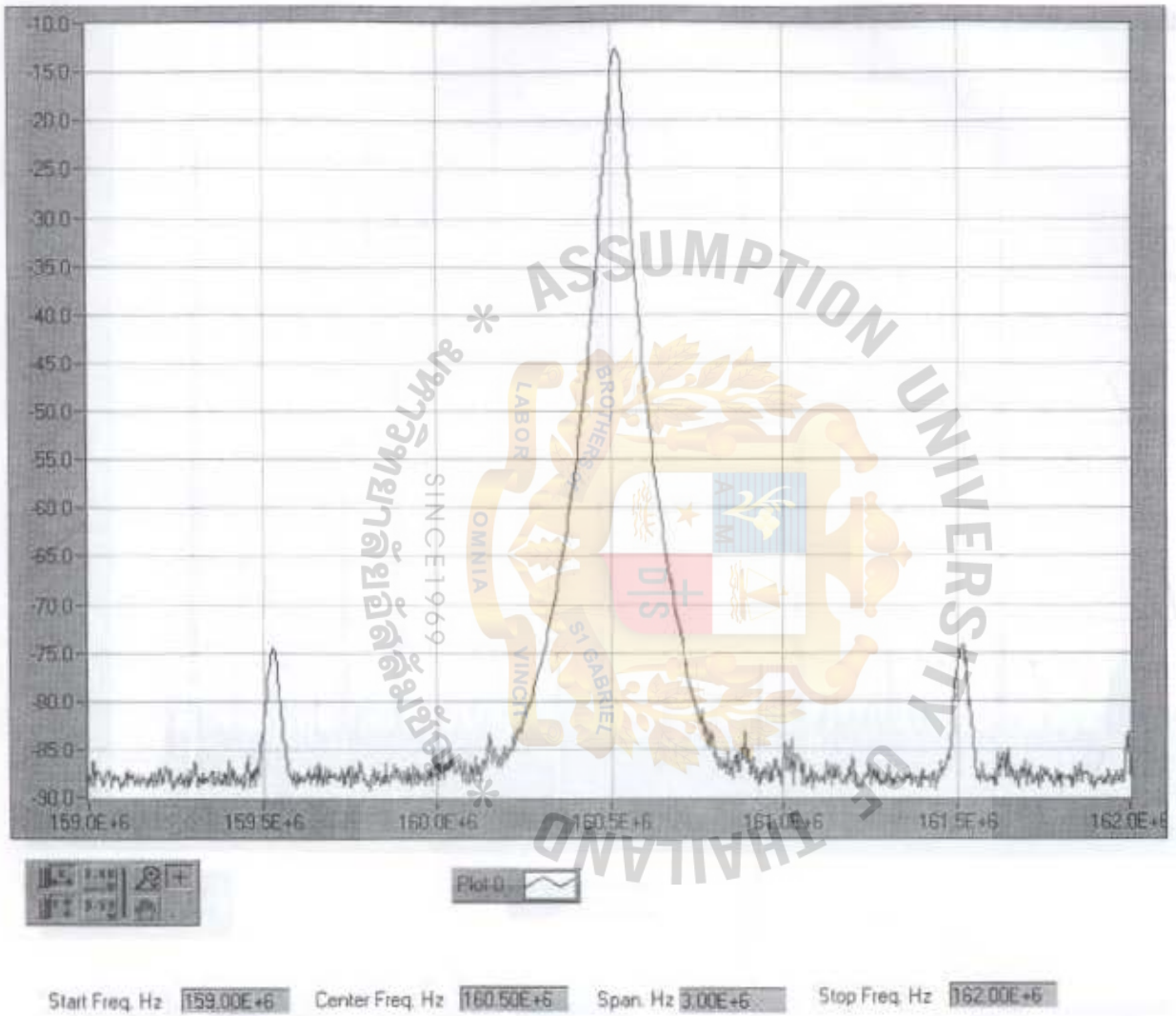

Figure 4.1 2X IF Local Oscillator (160 MHz) Output with 3 MHz Span

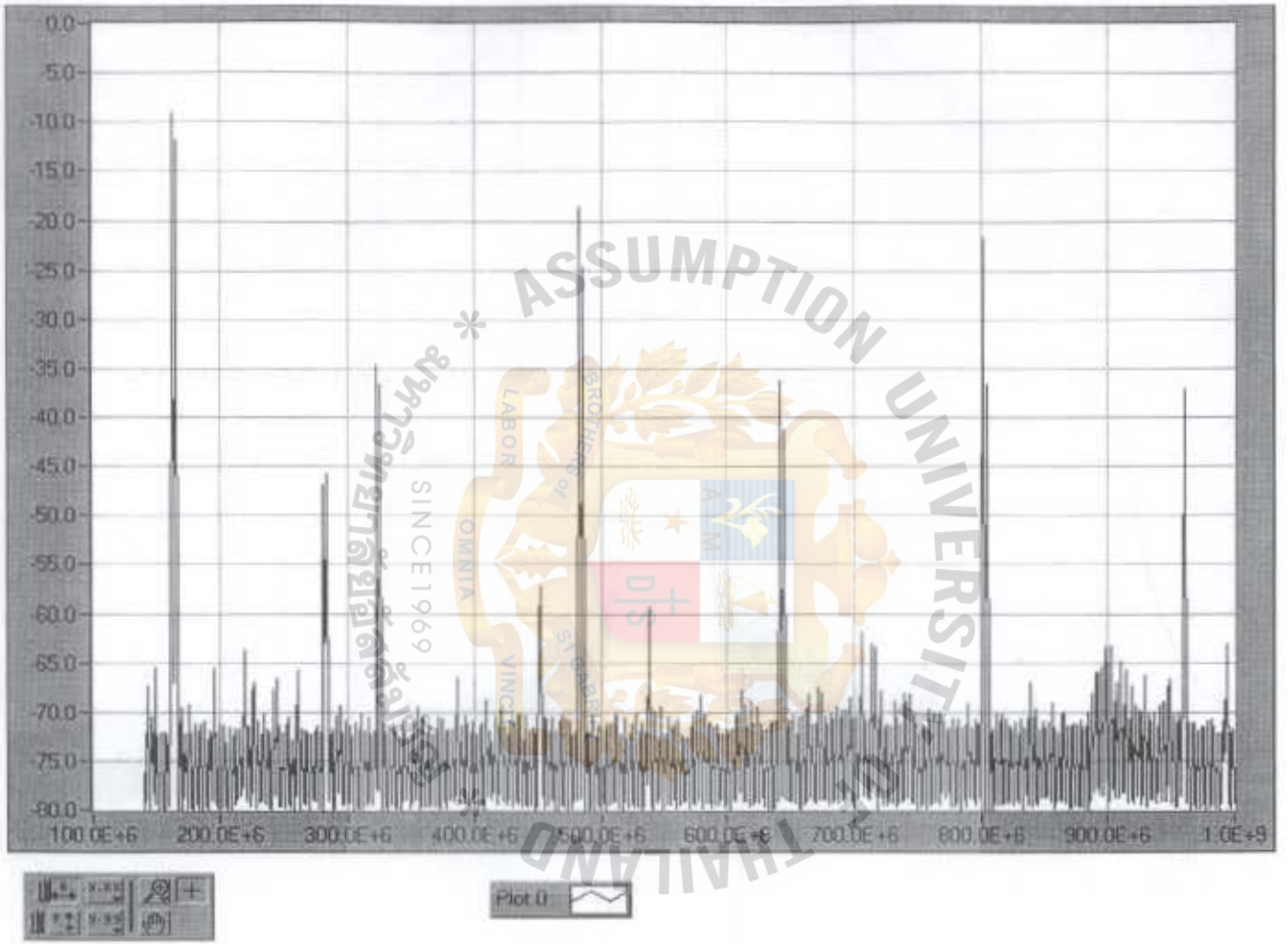

Figure 4.2 2X IF Local Oscillator (160 MHz) Output with 860 MHz Span

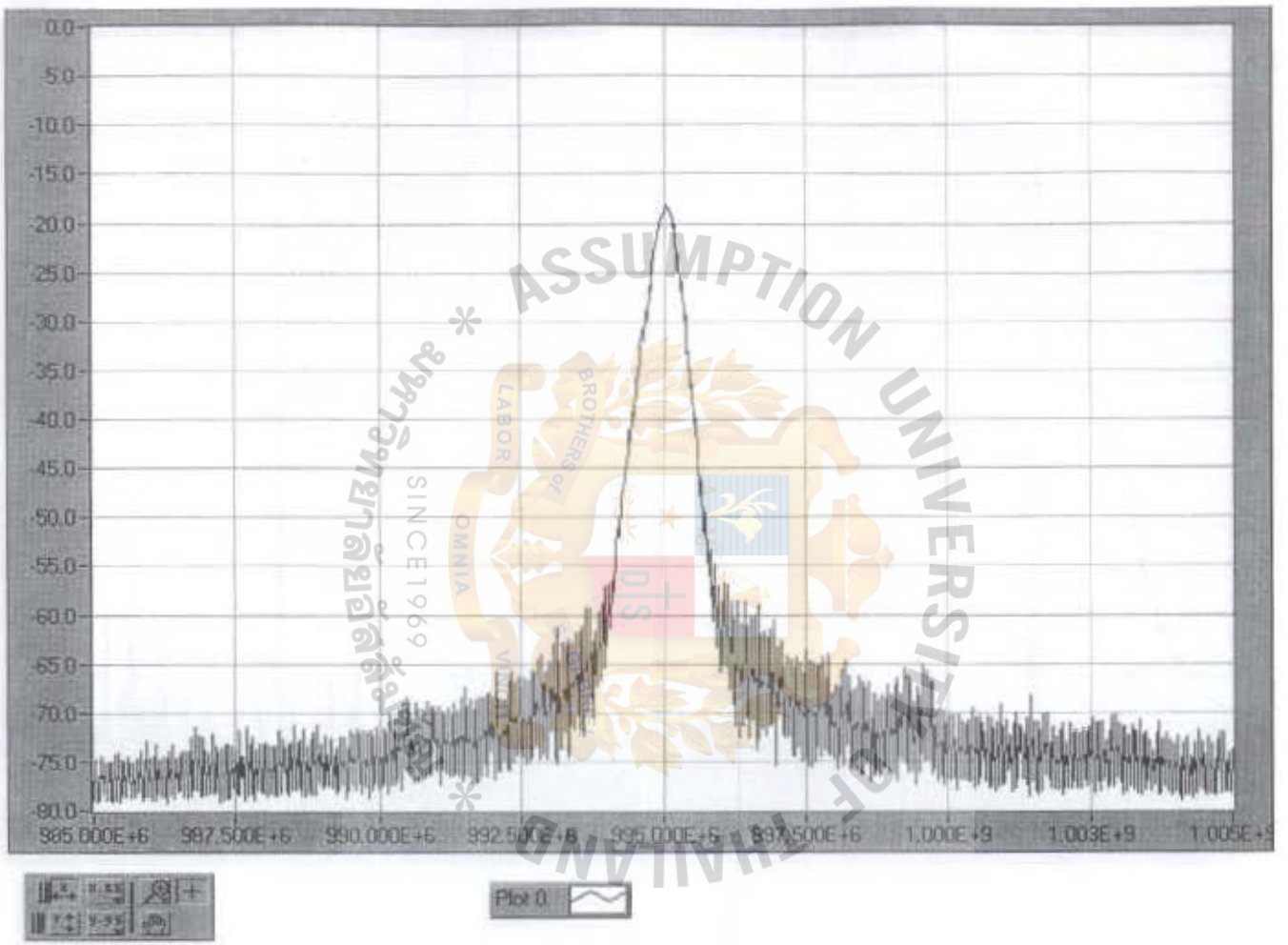

Figure 4.3 995 MHz RF Local Oscillator Output with 20 MHz Span

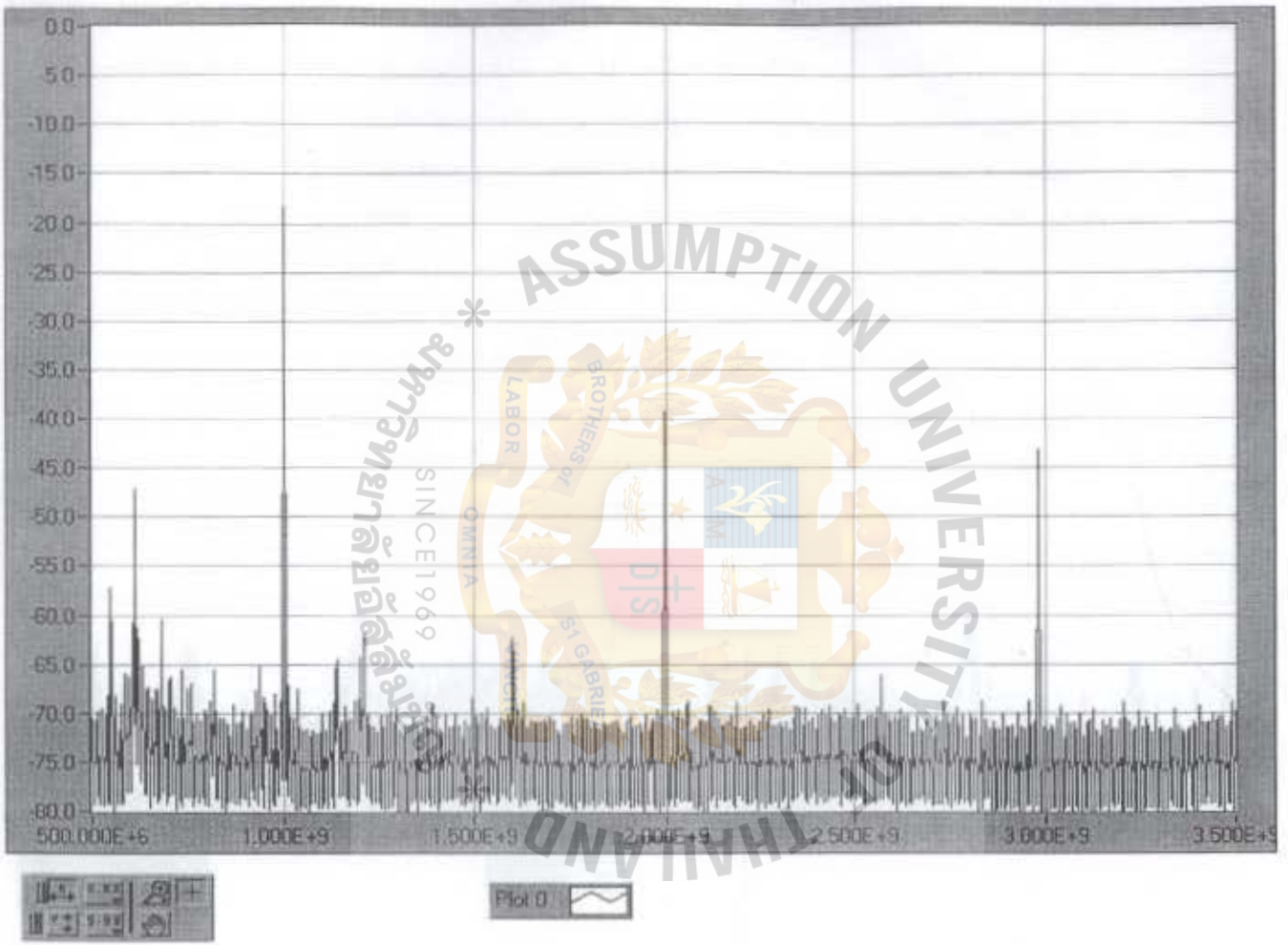

Figure 4.4 995 MHz RF Local Oscillator Output with 3 GHz Span

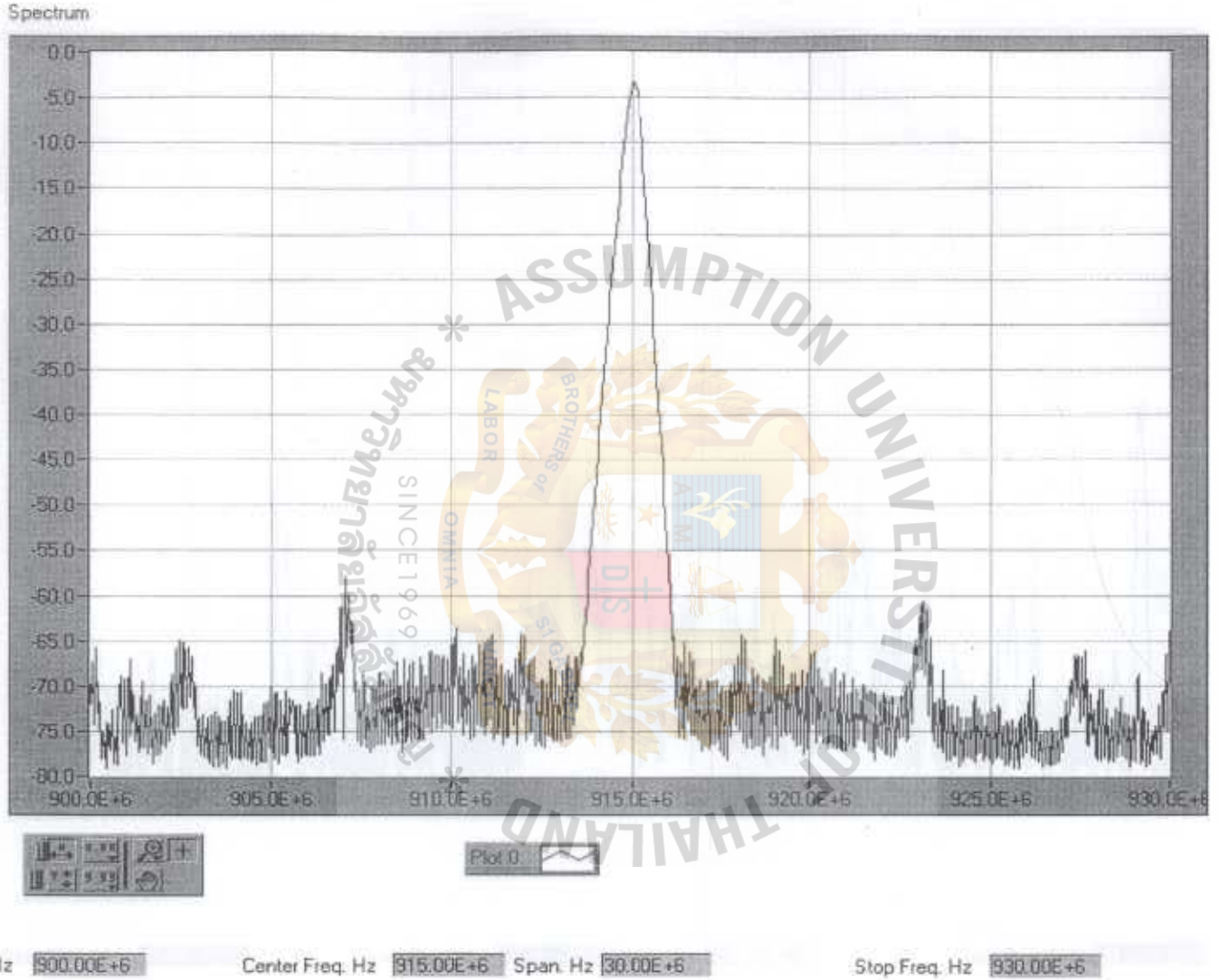

Figure 4.5 Transmitted Output Spectrum with 30 MHz Span

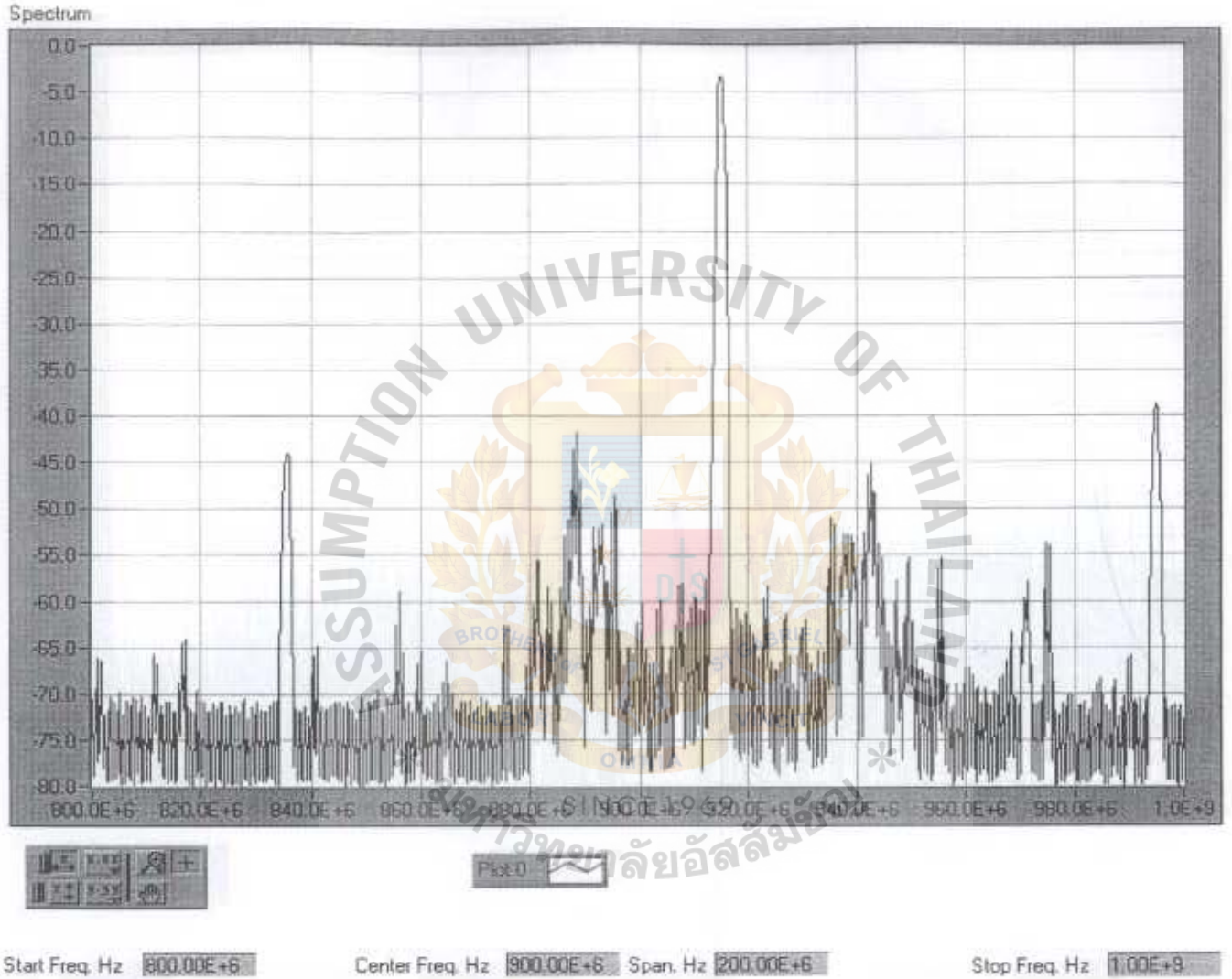

Figure 4.6 Transmitted Output Spectrum with 200 MHz Span

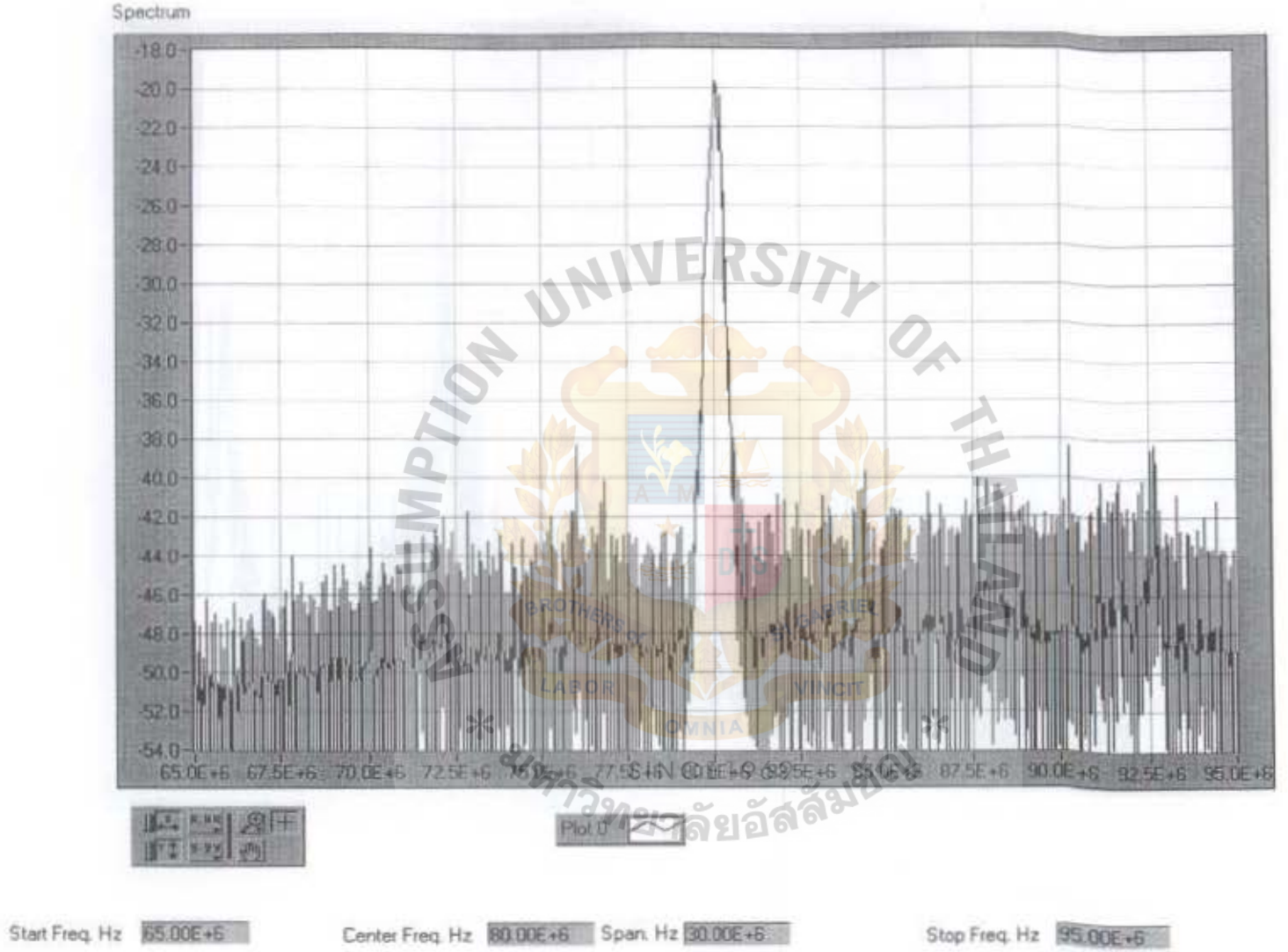

Figure 4.7 Received 80 MHz IF Spectrum with 30 MHz Span (direct input measurement)

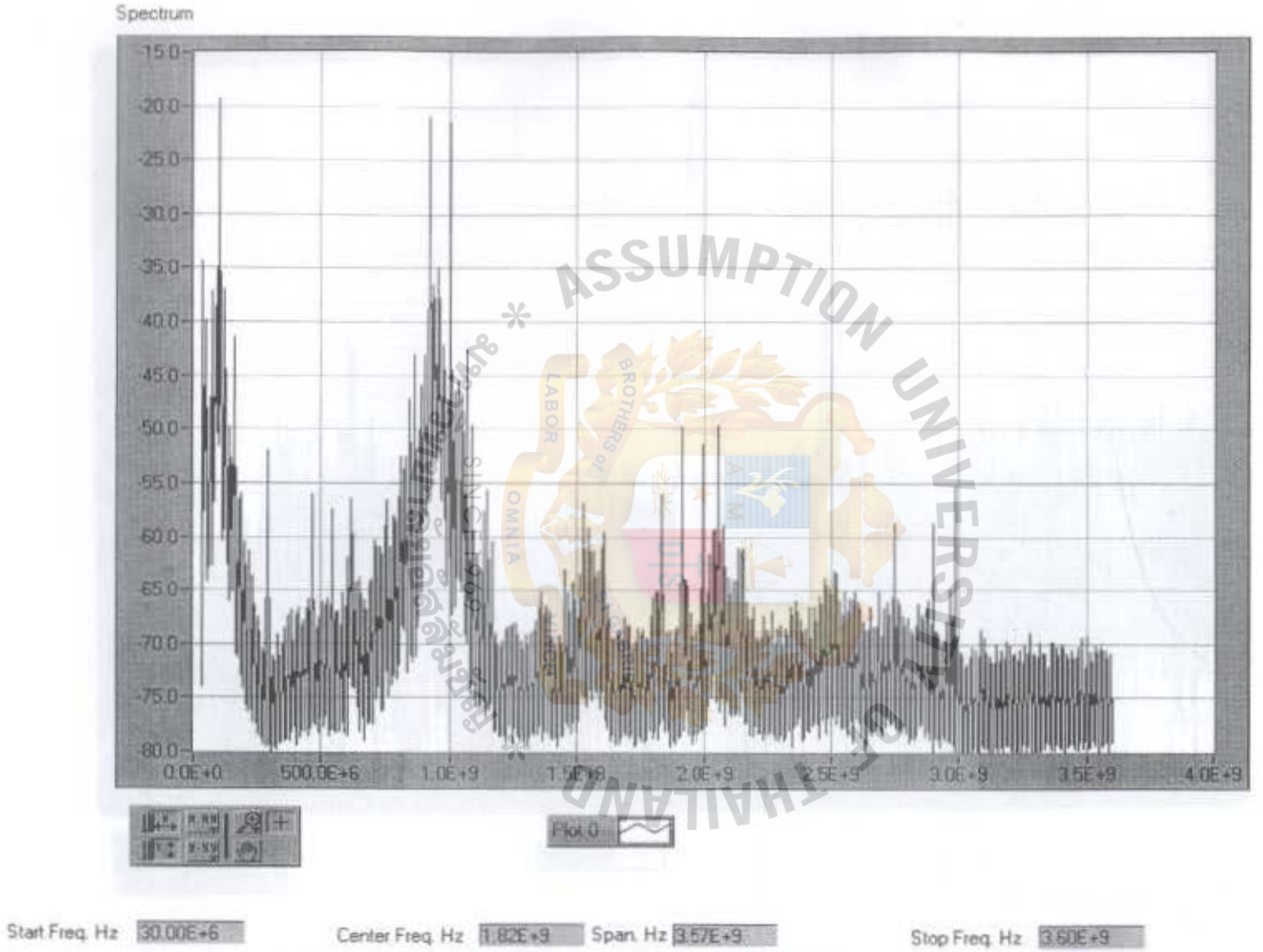

Figure 4.8 Received 80 MHz IF Spectrum with 3.57 GHz Span (direct input measurement)

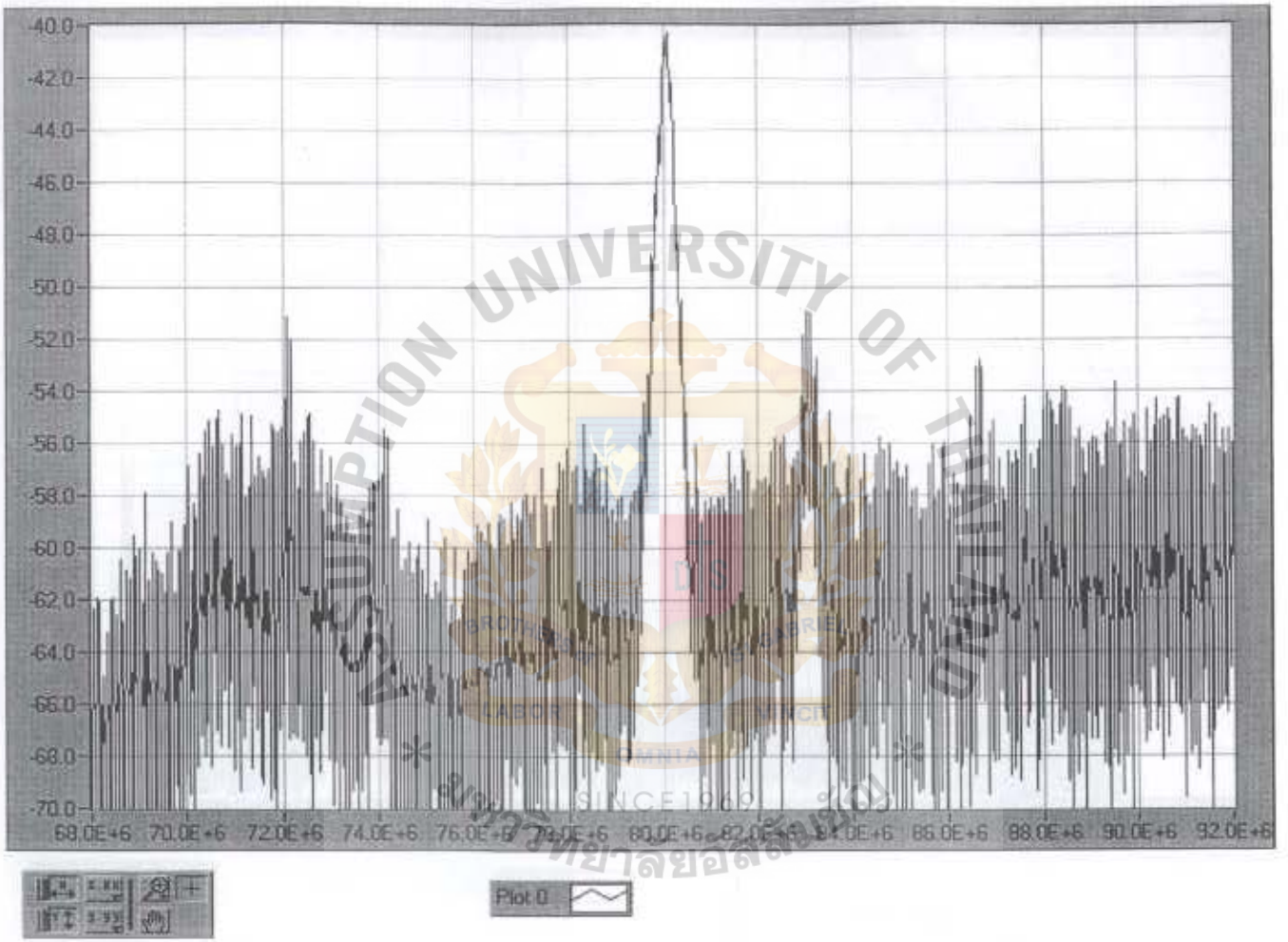

Figure 4.9 Received 80 MHz IF Spectrum with 24 MHz Span (Tx-Rx separation)

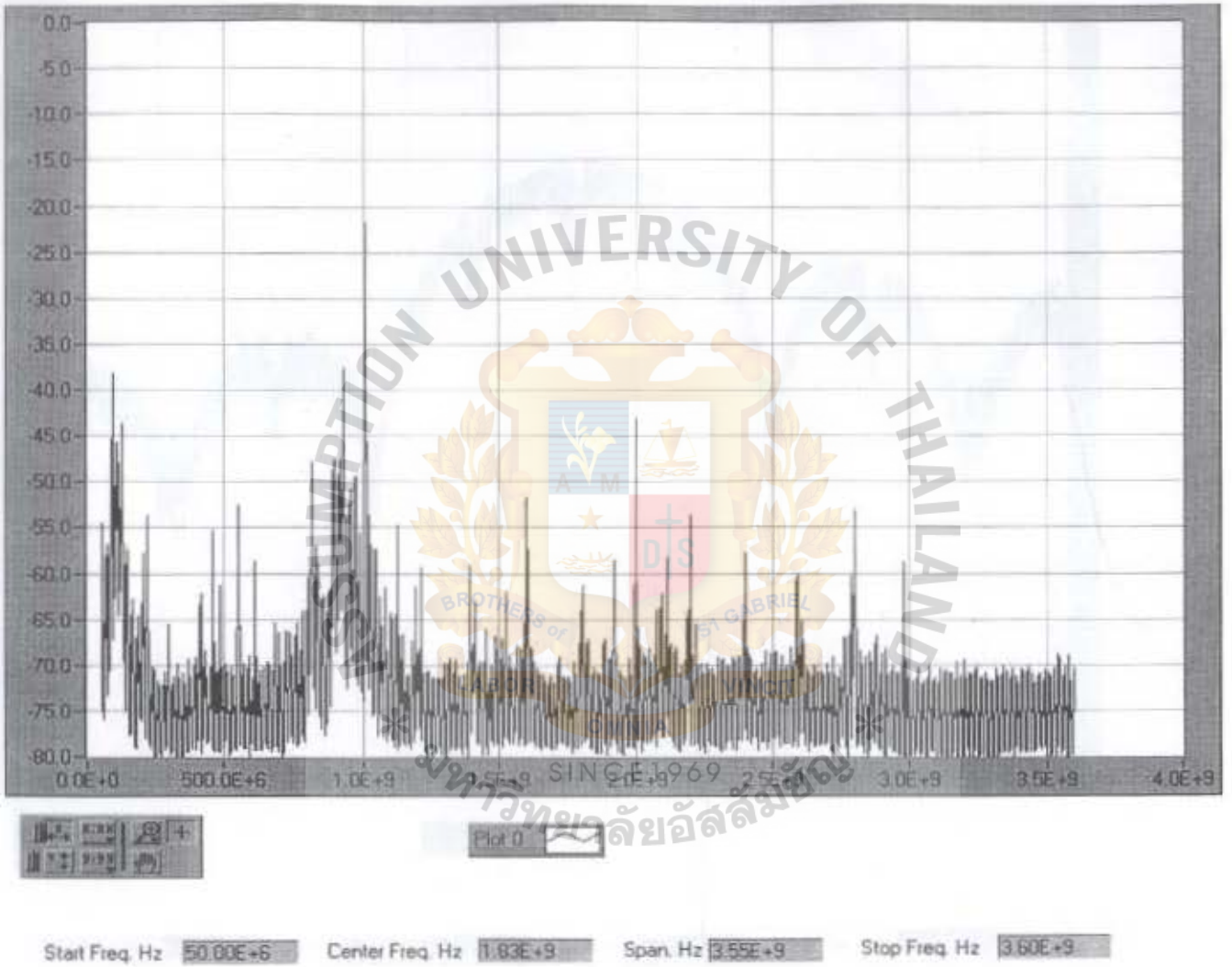

Figure 4.10 Received 80 MHz IF Spectrum with 3.55 GHz Span (Tx-Rx separation)

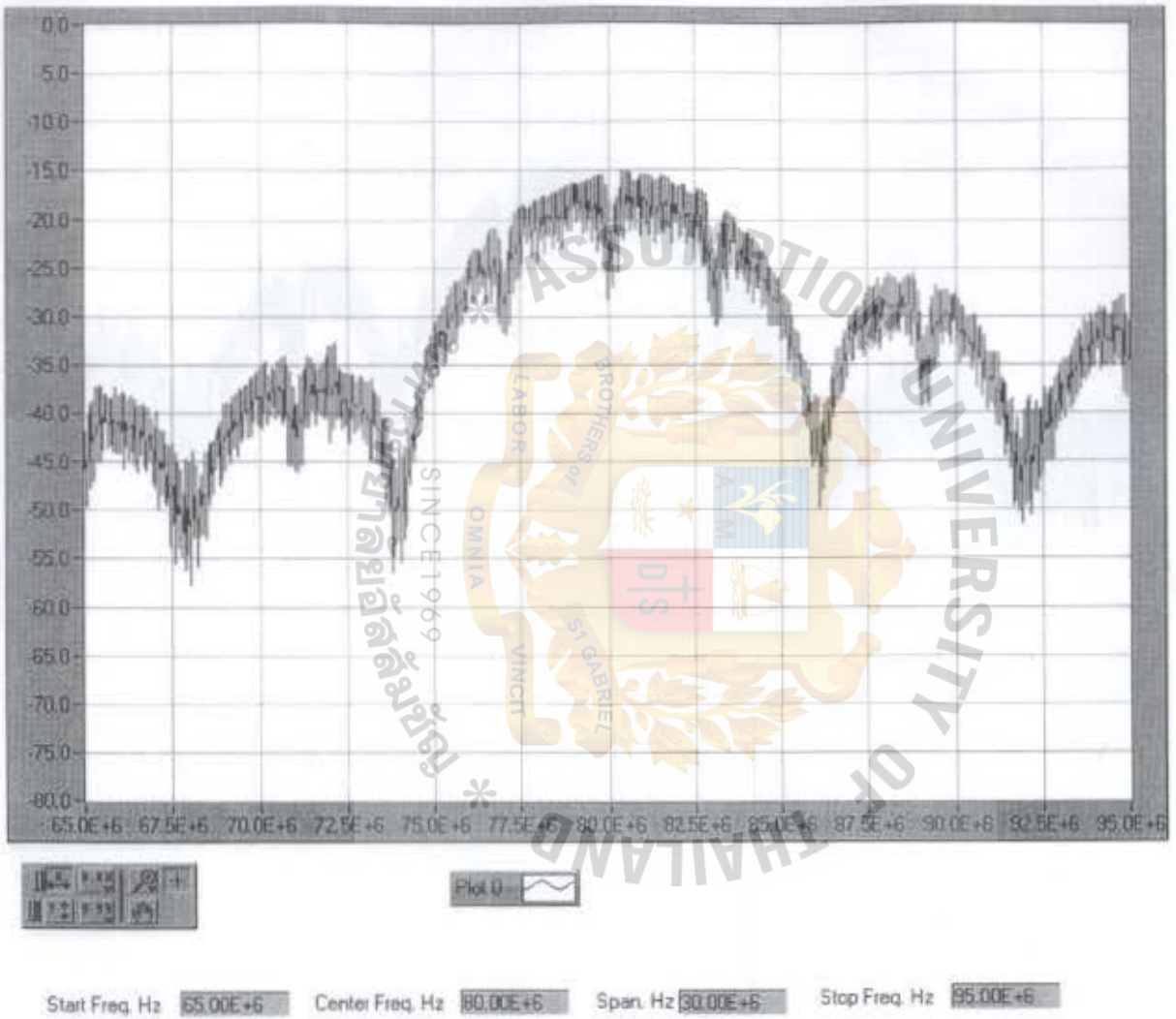

Figure 4.11 Input 80 MHz Spread Spectrum Signal

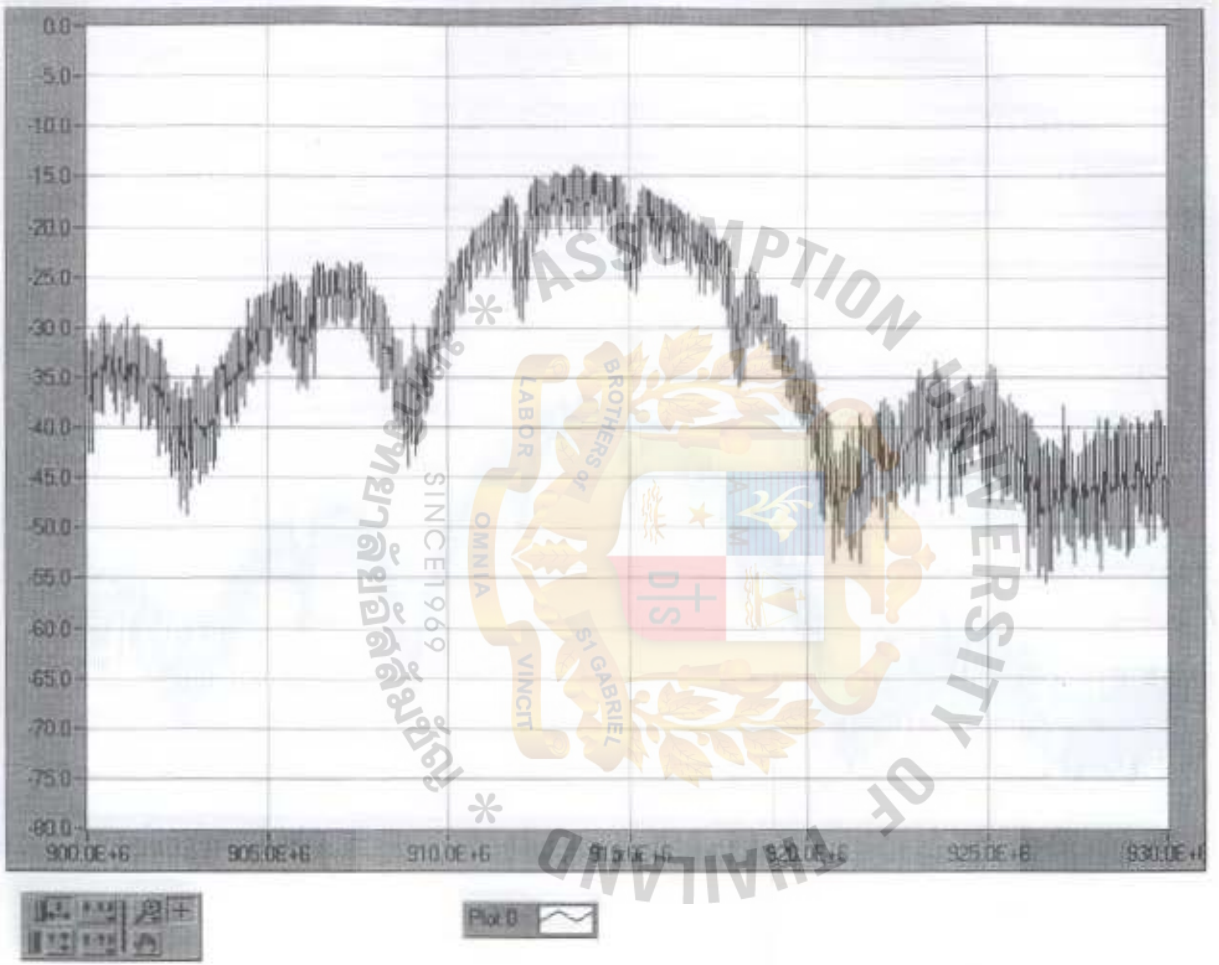

Figure 4.12 Transmitted Spread Spectrum Signal

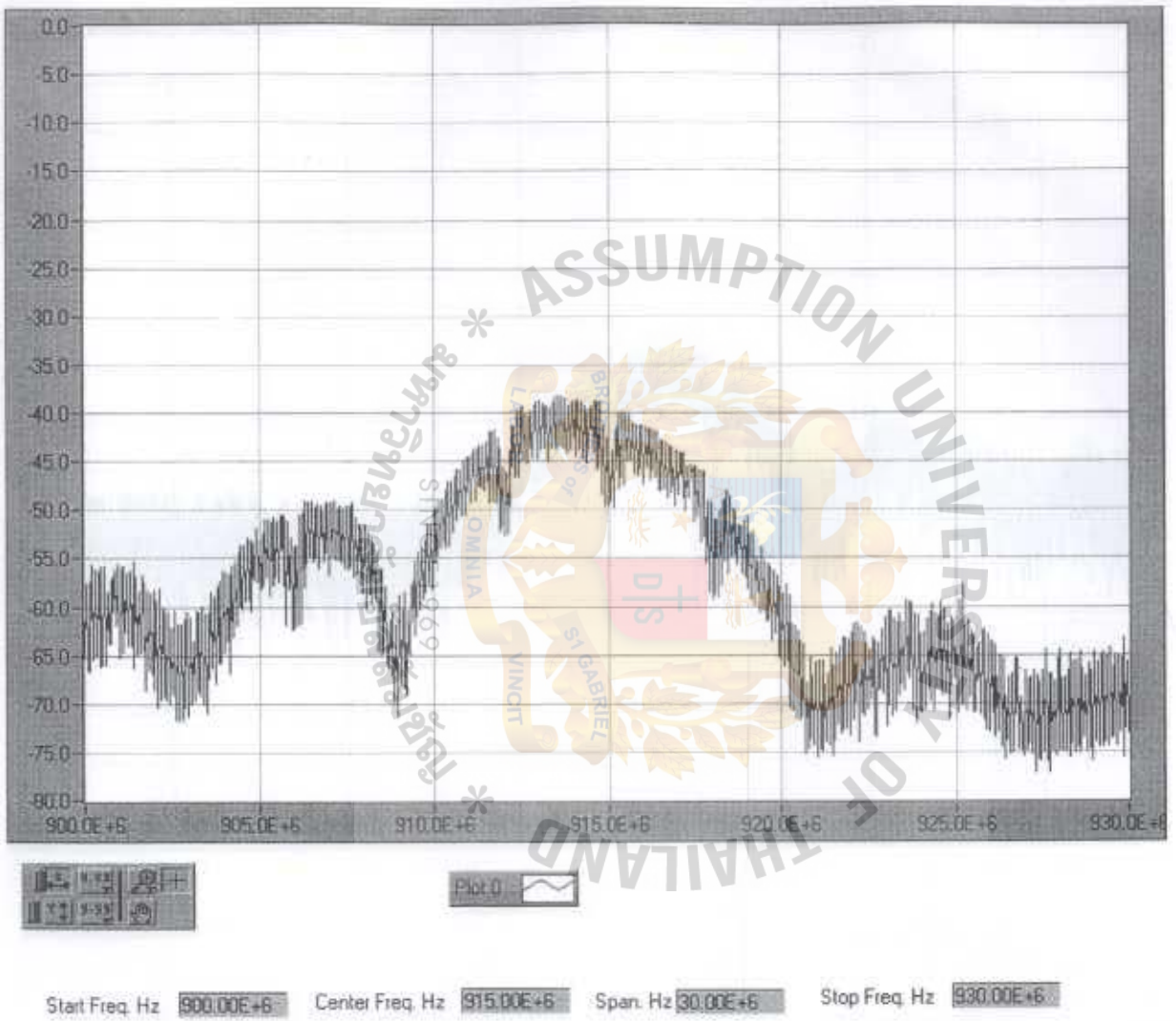

Figure 4.13 Received Spread Spectrum Signal at Antenna Port

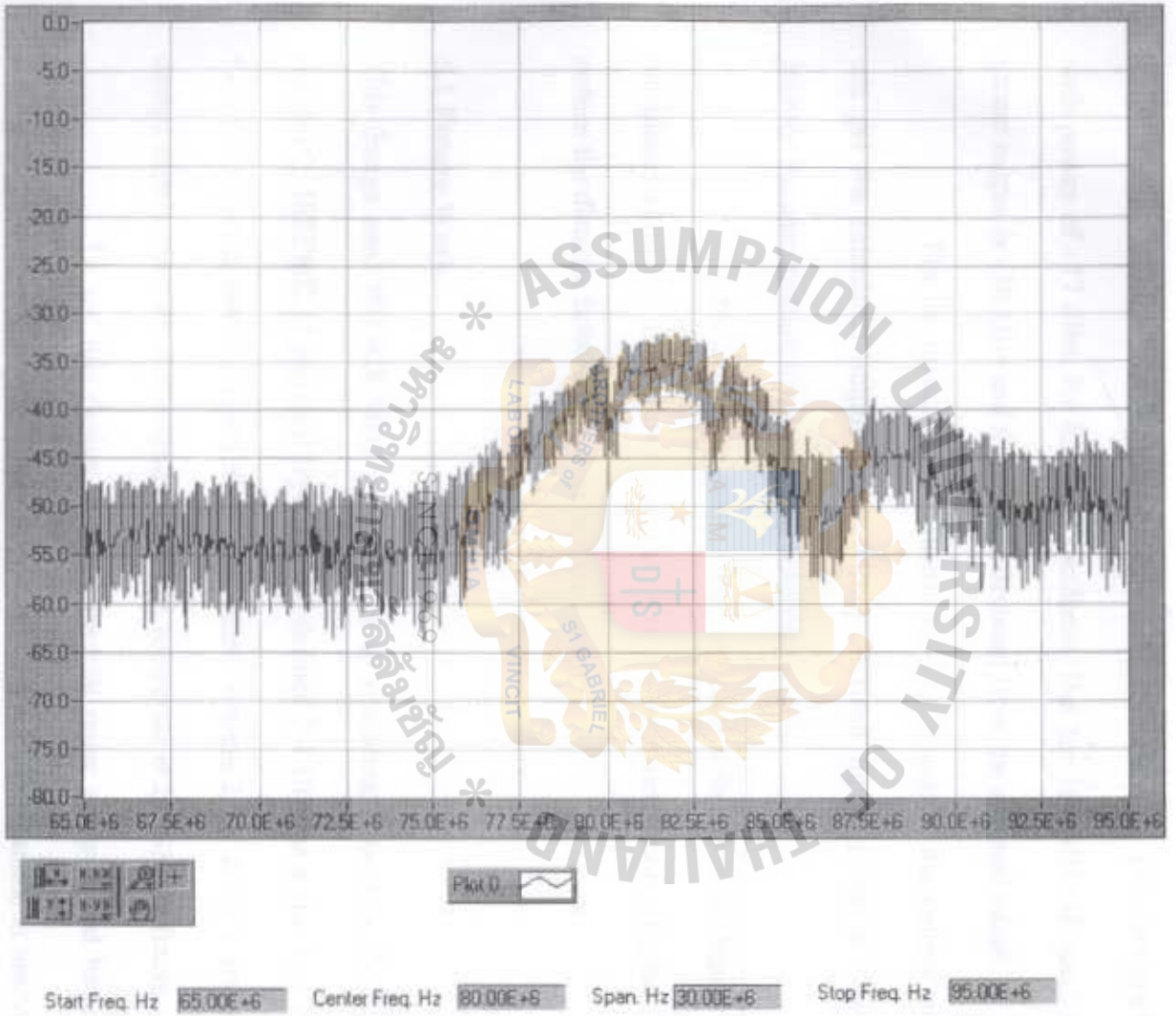

Figure 4.14 Received 80 MHz IF Spread Spectrum Signal

CHAPTER 5. CONCLUSION

From the measurement results as shown in chapter 4, there are some noises in the output spectrums. But we still achieved our goal, to design and build physical layer of 915 MHz wireless LAN RF part, with minimum cost.

For the dual frequency synthesizer, it works very well. We got 995 MHz with power of –17 dBm for RF local oscillator. But for 160 MHz IF local oscillator, power output is –10 dBm and it 0.5 MHz deviated from the required value.

For the transmit mode, there are some losses in the system and we can not get the calculated output power with predefined input IF signal. These losses include the transmission line losses and soldering losses.

For the receiving mode, the measured noise floor is higher than the calculated value. So the receiver sensitivity of the receiver become higher. This will reduce the distance between receiver and transmitter.

5.1 Future Work

This design used 902-928 MHz frequency as an operating frequency. As mention in chapter 2, IEEE802.11 physical layer for RF defined 2.4 GHz as a standard frequency. So this design is not interoperability with other wireless LAN design. Based on this design experiences, we will extend this design to operate at 2.4 GHz in future.

To use this design as a commercial noise analysis and battery power consumption analysis, which is very important in mobile computers, is needed. So we will design minimum possible noises with lowest battery consumption will be done in near future.

5.2 Suggestion

In this design, local oscillators are placed very close to the receiver parts and add more noises to received signal. To avoid this, the two local oscillator parts are needed to shield or place on separate PCB.

In this design, the local oscillator outputs are send to mixers without using filters. These local oscillators output include harmonics frequencies. These frequencies mix with the signal and create more noises. So, filters should use at the local oscillator output, both 995 MHz and 160 MHz, before entering to the mixer.

For the transmitting mode, this design did not use the filter before the signal entering to the upconverter mixer. Filter should be added to avoid noises and harmonics signal entering to the mixer.

APPENDIX A

A.1 Frequency Synthesizer interface

To get the required frequency, the four internal counters (reference dividers) are needed to register in synthesizer. Two counters for RF (RF R and RF N counter) and two for IF (IF R and IF N counters). The serial data format for R counter is shown in figure A.1. The control bits 00 is for IF and 01 is for RF counter.

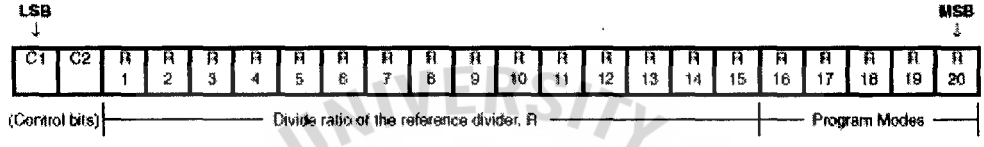

Figure A.1 R Counter for RF and IF

The N counter consists of the 7-bit swallow counter (A counter) and the 11-bit counter (B counter). If the Control bits are 10 the data is for IF and 11 for RF counter. Serial data format for N counter is shown in figure A.2. For the IF N counter bits 5, 6, and 7 are don't care bits.

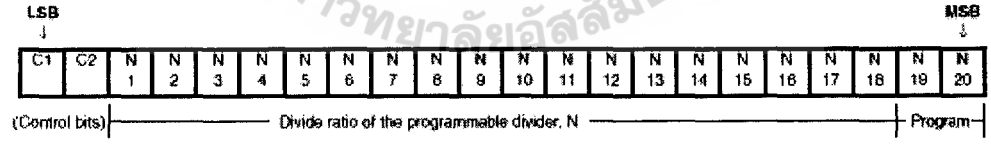

Figure A.2 N Counter for RF and IF

Counters can be calculated by using the following equation (A.1)

$$f_{VCO} = \left[\left(P \times B\right) + A\right] \times \frac{f_{OSC}}{R} \qquad \text{(A.1)}$$

Where

f_{VCO} = output frequency of external VCO

B = binary 11-bit programmable counter (3 to 2047)

A = binary 7-bit swallow counter ($0 \leq A \leq 127$ {RF}, $0 \leq A \leq 15$ {IF}, $A \leq B$)

f_{OSC} = output frequency of the external reference frequency oscillator

R = binary 15-bit programmable reference counter (3 to 32767)

P = dual modulus prescaler (for IF: P = 8 or 16; for RF: P = 32 or 64)

Oscillator frequency in this design uses 24 MHz. Using equation (A.1) the require counters for 160 MHz frequency can be calculated and the results are

f_{OSC}=24 MHz; A=0; P=16; B=10; R=24

Using the above parameters, the serial data for IF 160 MHz is shown in figure A.3.

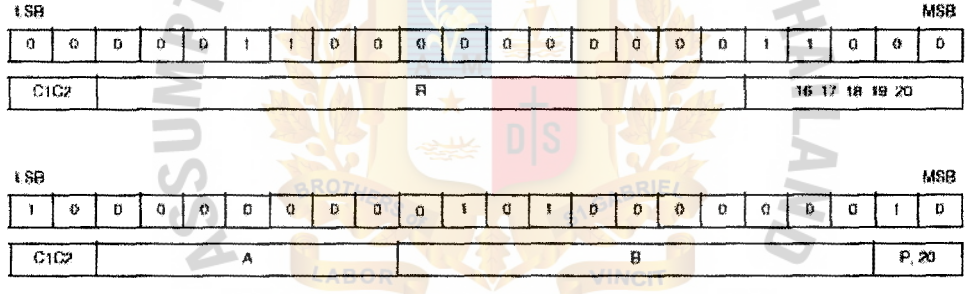

Figure A.3 Serial Data Format for 160 MHz

Using equation (A.1) the require counters for 995 MHz frequency are

f_{OSC}=24 MHz; A=3; P=32; B=31; R=24

and the serial data is shown in figure A.4.

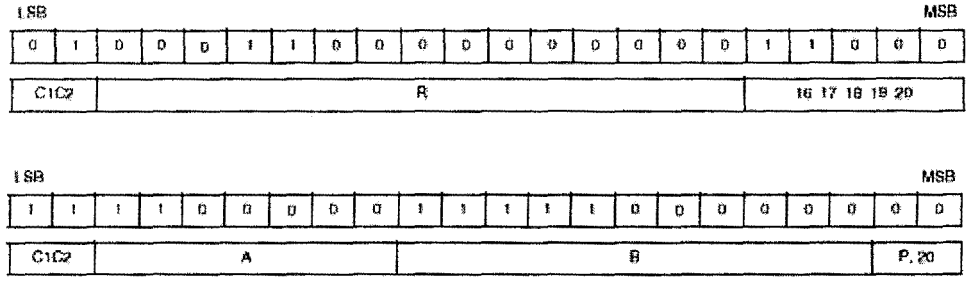

Figure A.4 Serial Data Format for 995 MHz

The initialization is required for synthesizer to configure internal control register at every power up. The following three signals are required for the functions of this interface:

Synth_Data : Serial Synthesizer Data

Synth_Clock : Synthesizer Data Clock

Synth_LE : Synthesizer Load Enable

The above three signals are program in ATMEL 8 bit micro controller AT89c2051. This interface schematic diagram is shown in figure A.5.

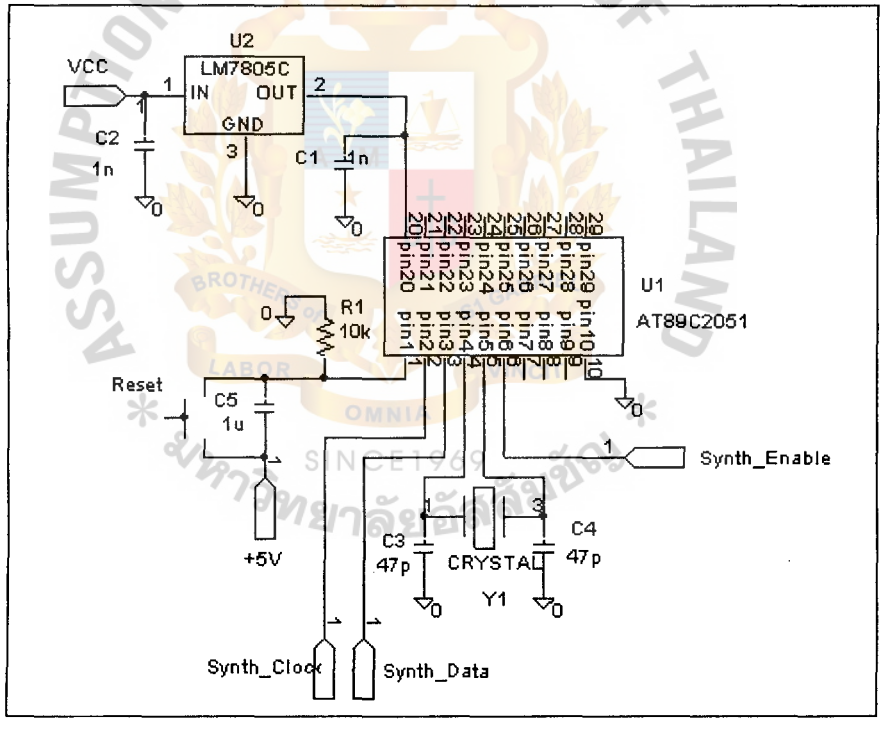

Figure A.5 Synthesizer Interface Schematic Diagram

APPENDIX B

B.1 Components List

The following table shows the components list used in wireless LAN RF part design.

Table B.1 The Components List

Name	Type	Value	Company
C71	Capacitor	10u	MURATA
C12, C73	Capacitor	4.7 u	MURATA
C53	Capacitor	0.68u	MURATA
C6, C8, C19, C21, C23, C28, C31, C32, C33, C41, C45, C48, C50, C60, C61, C63, C64, C67, C68, C72, C74, C75, C77	Capacitor	0.1u	MURATA
C52	Capacitor	0.068u	MURATA
C38	Capacitor	0.056u	MURATA
C1, C2, C29, C30, C54	Capacitor	0.01u	MURATA
C39	Capacitor	5600p	MURATA
C11, C37, C47, , C62, C65, C66, C69, C70, C78	Capacitor	1000p	MURATA
C10, C13, C14	Capacitor	270p	MURATA
C15, C16, C20	Capacitor	220p	MURATA
C81	Capacitor	120p	MURATA
C34, C36, C40, C43, C44, C49, C51, C76	Capacitor	100p	MURATA
C3, C5, C9, C22, C25, C26, C27, C79, C80	Capacitor	53p	MURATA
C17, C18	Capacitor	47p	MURATA
C42, C46	Capacitor	22p	MURATA
C4, C7, C24	Capacitor	20p	MURATA
C57	Capacitor	15p	MURATA
C35, C58, C59	Capacitor	10p	MURATA
C55, C56	Capacitor	3p	MURATA
L3, L7	Inductor	22u	
L5, L11	Inductor	10u	
L2	Inductor	87n	TOKO
L13	Inductor	68n	COIL CRAFT
L4	Inductor	47n	COIL CRAFT
L9, L14	Inductor	33n	TOKO
L1,L8	Inductor	18n	COIL CRAFT
L12	Inductor	27n	TOKO
L10	Inductor	3.9n	COIL CRAFT
R9	Resistor	3.3K	ROHM
R8	Resistor	2.2K	ROHM
R10	Resistor	1.8K	ROHM
R4	Resistor	560	ROHM
R2	Resistor	270	ROHM
R3	Resistor	130	ROHM
R6, R7, R11	Resistor	100	ROHM
R5	Resistor	51	ROHM
R1	Resistor	10	ROHM
U1, U13	RF Filter	TDFM2A-915E-10	TOKO

Name	Type	Value	Company
U7, U10	RF BPF	LFA30-12B-0915B	MURATA
U2	Antenna Switch	SA630	PHILIP
U15	Synthesizer	HFA3524	HARRIS
U16	VCO	RF2504	RF MD
U17	VCO	MAX2620	MAXIM
U3, U5, U11,	LNA	MAX 2630	MAXIM
U4	LNA	MAX2631	MAXIM
U6, U12, U14, U19,	LNA	MAX2650	MAXIM
U8	Down Converter	MAX2681	MAXIM
U9	Up Converter	MAX2661	MAXIM
U18	Oscillator	24 MHz	
U22	Inverter	7404	MOTOROLA
U20, U21	5V Regulator	TK11235	TOKO

BIBLIOGRAPHY

[1] Theodore S. Rappaport, "Wireless Communications: Principle and Practice," Prentice Hall PTR, Upper Saddle Rivers, New Jersey, 1996.

[2] Jim Zyren, Al Petric, "Tutorial on Basic Link Budget Analysis," HARRIS Semiconductor Application Note, June 1998.

[3] Robert Rood, Doug Schultz, "2.4 GHz Direct Sequence Wireless LAN Cascade Analysis," HARRIS Semiconductor Application Note, September 1998.

[4] Carl Andren, Mike Paljug, and Doug Schultz, "PRISM1KIT-EVAL DSSS PC Card Wireless LAN Description," HARRIS Semiconductor Application Note, November 1998.

[5] Theodore S. Rappaport, Keith Blankenship, Hao Xu, " Tutorial on Propagation and Radio system Design Issues in Mobile Radio Systems for the GloMo Project," Virginia Polytechnic Institute and State University, January 31, 1997.

[6] Jim Geier, "Wireless Networking Handbook," New Riders Publishing, 201 West 103rd Street, Indianapolis, 1996.

[7] Ulrich L. Rohde, "Microwave and Wireless Synthesizers Theory and Design," A Wiley-Interscience publication, New York, 1997.

[8] Floyd M. Gardner, "Phase Lock Techniques," 2nd ed., John Wiley & Sons, Inc., New York, 1979.

[9] Howard M. Berlin, "Design of Phase Lock Loop Circuits with Experiments," 1st ed., Howard W. Sams & Co., Indiana, 1978.

[10] Peter Vizmuller, "RF Design Guide: Systems, Circuits and Equations," 1st ed., Artech House, Inc, 1995.

[11] www.wlana.com/intro/index.html

[12] www.g4dvj.demon.co.uk/synth.htm

[13] www.intersil.com/prism/prism.asp

[14] www.proxim.com/wireless/standards/80211wp.shtml