An 80 MHz Wireless LAN
(Physical Layer)

by

Sumet   Assawapongkasem

Faculty of Engineering
July 2000

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A thesis

submitted to the Faculty of Engineering

by

Sumet Assawapongkasem

in partial fulfillment of the requirements

for the degree of

Master of Engineering in Broadband Telecommunications

Advisor: Dr. Thiraphong Charoenkhunwiwat

Assumption University

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ABSTRACT

A wireless LAN system is proposed to provide mobility for existing data communication services. This thesis presents a design of the wireless LAN card to transmit data at frequency of 80 MHz and receive data from MAC layer. Direct sequence spread spectrum and quadrature phase shift keying (QPSK) modulation technique are used in design. Filter and amplifier are used to increase the performance of the signal and reduce the noise, and this system supports a data rate up to 2 Mbps. The spread spectrum system design along with detailed description of hardware and software simulation is presented.

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CHAPTER 1. INTRODUCTION

In this chapter, we introduce to wireless system. Objective of this thesis and several information of wireless network are discussed. History of wireless network, wireless network architecture, radio-based wireless LAN, benefits of wireless networks, and the future of wireless network are discussed.

1.1 Objective

Today, communication has increasing influence on our daily life. Wireless data communication services are widely used and allow people to access the data network without a physical connection. In this thesis, we want to design and build a real wireless LAN system operating at radio frequency of 80 MHz. The physical layer of this network has been designed to perform direct sequence spread spectrum processing and use technique of QPSK modulation to have a transmission rate up to 2 Mbps.

1.2 History of Wireless Networks

The first indication of wireless networking dates back to the 1800s and earlier. Indians, for example, sent information to each other via smoke signals from a burning fire. Prior to the nineteenth century, scientists thought light was the only wavelength component of the electromagnetic spectrum. During the nineteenth and twentieth centuries, researchers learned that the spectrum actually consists of longer wavelengths (lower frequencies) as well. Experiments showed that lower frequencies, such as radio waves and infrared light, could be sent through the air with moderate amounts of transmit power and easy-to-manufacture antennas. As a result, companies began building radio

transmitters and receivers, making public and private radio communications, television, and wireless networking possible.

Network technologies and radio communications were brought together for the first time in 1971 at the University of Hawaii as a research project called ALOHANET. The ALOHANET system enabled computer sites at seven campuses spread out over four islands to communicate with the central computer on Oahu without using existing, unreliable, expensive phone lines. ALOHANET offered bi-directional communications, in a star topology, between the central computer and each of the remote stations. The remote stations had to communicate with each other via the centralized computer. ALOHANET became popular among network researchers because of the unique combination of packet switching and broadcast radio.

In 1985, the Federal Communications Commission (FCC) made the commercial development of radio-based LAN components possible by authorizing the public use of the Industrial, Scientific, and Medical (ISM) bands. This band of frequencies resides between 902 MHz and 5.85 GHz, just above the cellular phone operating frequencies. The ISM band is very attractive to wireless network vendors because it provides a part of the spectrum upon which to base their products, and end users do not have to obtain FCC licenses to operate the products. The ISM band allocation has had a dramatic effect on the wireless industry, prompting the development of wireless LAN components.

During the late eighties, the decreasing size of computers from desktop machines to laptops allowed employees to take their computers with them around the office and on business trips. Computer companies then scrambled to develop products that would support wireless connectivity methods. The current depressed state of the wireless LAN market should change as standards mature. The Institute of Electrical and Electronic Engineers (IEEE) 802 Working Group, responsible for the development of

LAN standards such as ethernet and token ring, initiated the 802.11 Working Group to develop a standard for wireless LANs.

1.3 Wireless Network Architecture

In general, networks perform many functions to transfer information from source to destination.

- The medium provides a bit pipes (path for data to flow) for the transmission of data.

- Medium access techniques facilitate the sharing of a common medium.

- Synchronization and error control mechanisms ensure that each link transfers the data intact.

- Routing mechanisms move the data from the originating source to the intended destination.

A good way to depict these functions is to specify the network's architecture. This architecture describes the protocols, major hardware, and software elements that constitute the network. A network architecture, whether wireless or wired, may be viewed in two ways, logically and physically.

1.3.1 Logical Architecture of a Wireless Network

A logical architecture defines the network's protocols—rules by which two entities communicate.

One popular standard logical architecture is the 7-layer Open System Interconnection (OSI) Reference Model, developed by the International Standards Organization (ISO). OSI specifies a complete set of network functions, grouped into layers. Figure 1.1 illustrates the OSI Reference Model.
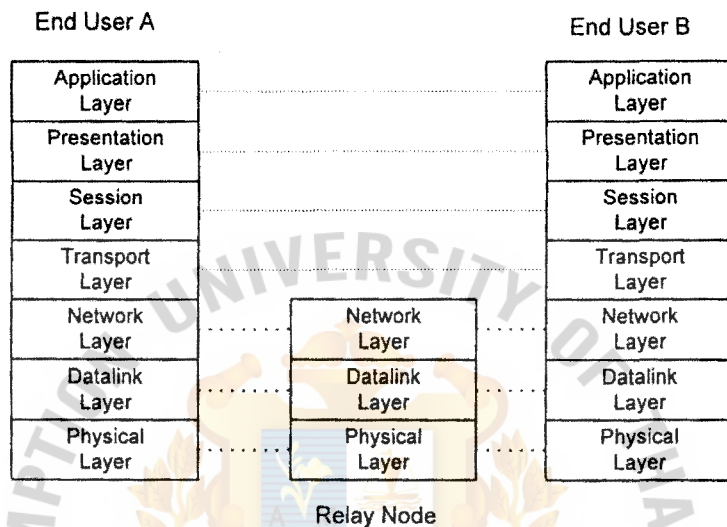
Figure 1.1 The Open System Interconnection Reference Model

The OSI layers provide the following network functionality:

- Layer 7—Application layer. Establishes communications with other users and provides services such as file transfer and e-mail to the end users of the network.

- Layer 6—Presentation layer. Negotiates data transfer syntax for the application layer and performs translations between different data types, if necessary.

- Layer 5—Session layer. Establishes, manages, and terminates sessions between applications.

- Layer 4—Transport layer. Provides mechanisms for the establishment, maintenance, and orderly termination of virtual circuits, while shielding the higher layers from the network implementation details.

- Layer 3—Network layer. Provides the routing of packets from source to destination.

- Layer 2—Data Link layer. Ensures synchronization and error control between two entities.

- Layer 1—Physical layer. Provides the transmission of bits through a communication channel by defining electrical, mechanical, and procedural specifications.

Wireless network logical architecture as shown in figure 1.2, wireless LANs and MANs function only within the Physical and Data Link layers, which provide the medium, link synchronization, and error control mechanisms. Wireless WANs provide these first two layers, as well as Network Layer routing.
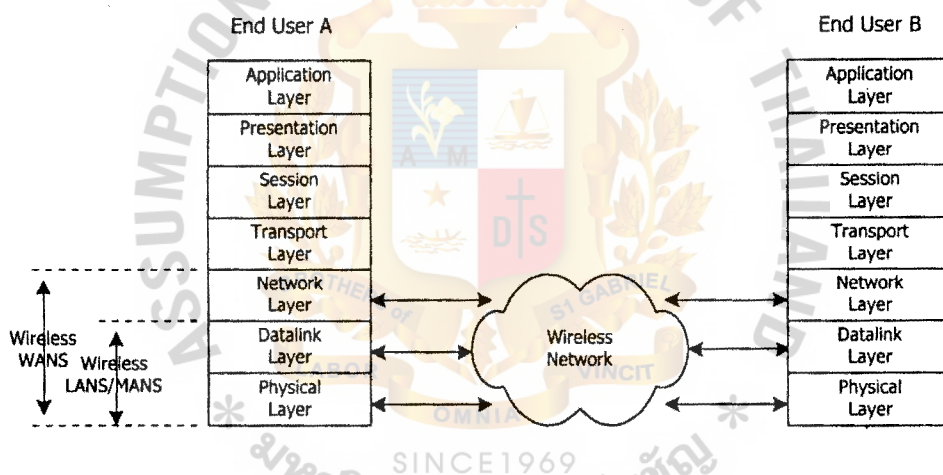
Figure 1.2 The wireless network logical architecture

1.3.2 Physical Architecture of a Wireless Network

The physical components of a wireless network implement the Physical, Data Link, and Network Layer functions (see figure 1.3). The Network Operating System (NOS) of a network, such as Novell NetWare, supports the shared use of applications, printers, and disk space. The NOS, located on client and server machines, communicates with the wireless Network Interface Card (NIC) via driver software, enabling applications to utilize the wireless network for data transport. The NIC prepares data signals for

5

propagation from the antenna through the air to the destination comprised of the same set of components.
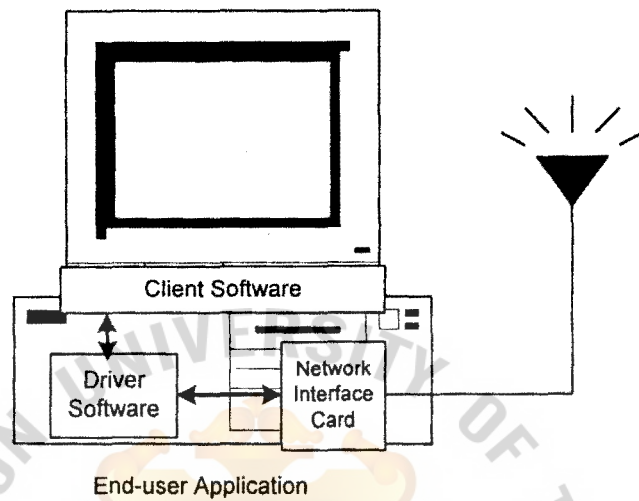
Figure 1.3 The physical components of a wireless network

1.3.2.1 End-User Appliances

As with any system, there must be a way for users to interface with applications and services. Whether the network is wireless or wired, an end-user appliance is a visual interface between the user and the network.

Following are the classes of user appliances:

- Desktop workstations

- Laptops

- Palmtops

- Pen-based computers

- Personal Digital Assistants (PDA)

- Pagers

1.3.2.2 Network Software

A wireless network supports the NOS and its applications, such as word processing, databases, and e-mail, enabling the flow of data between all components. NOSs provide file and print services, acting as a platform for user applications. Many NOSs are server-oriented, as shown in figure 1.4, where the core software resides on a high-performance PC. A client, located on the end user's appliance, includes server software that directs the user's command to the local computer resources, or puts it out onto the network to another computer. Some wireless networks may also contain middleware that interfaces mobile applications to the wireless network hardware.
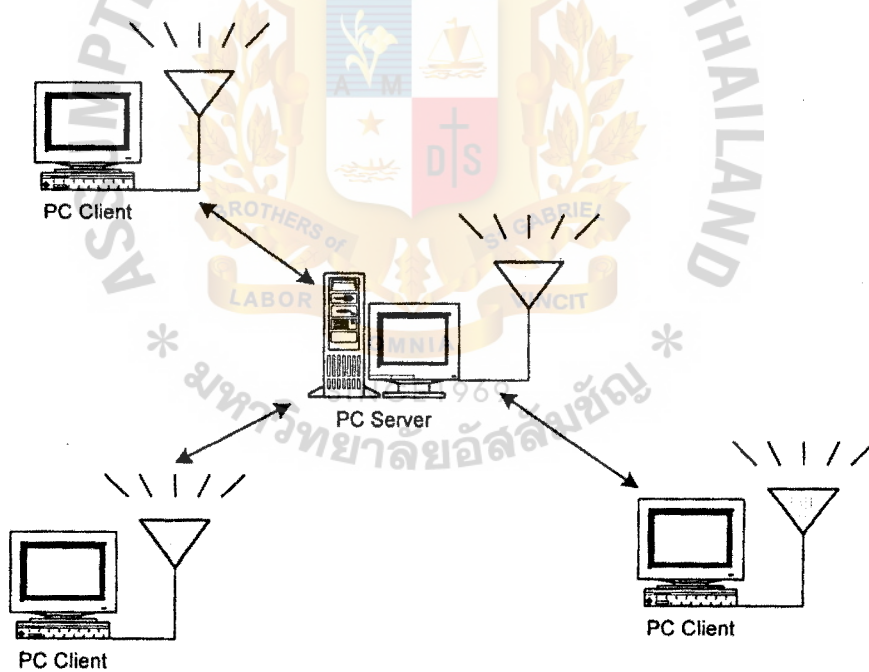
Figure 1.4 The server-based network operating system

1.3.2.3 Wireless Network Interface

Computers process information in digital form, with low direct current (DC) voltages representing data ones and zeros. These signals are optimum for transmission within the computer, not for transporting data through wired or wireless media. A wireless network interface couples the digital signal from the end-user appliance to the wireless medium, which is air, to enable an efficient transfer of data between sender and receiver. This process includes the modulation and amplification of the digital signal to a form acceptable for propagation to the receiving location. *Modulation* is the process of translating the baseband digital signal to a suitable analog form. The wireless modulator translates the digital signal to a frequency that propagates well through the atmosphere. Wireless networks employ modulation by using radio waves and infrared light. *Amplification* raises the amplitude of the signal so it will propagate a greater distance.

The wireless network interface also manages the use of the air through the operation of a communications protocol. For synchronization, wireless networks employ a carrier sense protocol similar to the common ethernet standard. This protocol enables a group of wireless computers to share the same frequency and space. As an analogy, consider a room of people engaged in a single conversation in which each person can hear if someone speaks. This represents a fully connected bus topology (where everyone communicates using the same frequency and space) that ethernet and wireless networks, especially wireless LANs, utilize. To avoid having two people speak at the same time, you should wait until the other person has finished talking. Also, no one should speak unless the room is silent. This simple protocol ensures only one person speaks at a time, offering a shared use of the communications medium. Wireless networks use carrier sense protocols and operate in a similar fashion, except the

communications are by way of radio signals or infrared light. Figure 1.5 illustrates the generic carrier sense protocol.
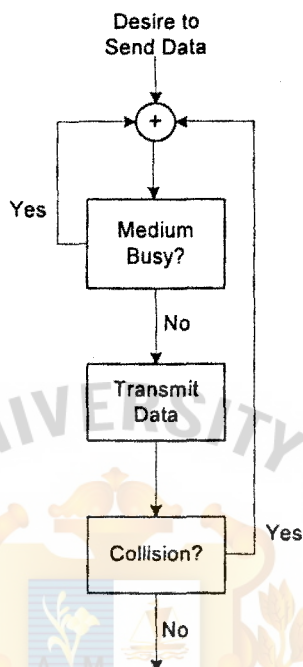
Figure 1.5 The operation of the carrier sense protocol

Wireless networks handle error control by having each station check incoming data for altered bits. If the destination station does not detect errors, it sends an acknowledgment back to the source station. If the station detects errors, the data link protocol ensures that the source station resends the packet.

1.3.2.4 Antenna

The antenna radiates the modulated signal through the air so that the destination can receive it. Antennas come in many shapes and sizes and have the following specific electrical characteristics:

• Propagation pattern

- Radiation power

- Gain

- Bandwidth

The propagation pattern of an antenna defines its coverage. A truly omnidirectional antenna transmits its power in all directions, whereas a directional antenna concentrates most of its power in one direction. Figure 1.6 illustrates the differences. Radiation power is the output of the radio transmitter. Most wireless network devices operate at less than 5 watts of power.

Omnidirectional Radio Propagation

Directional Radio Propagation
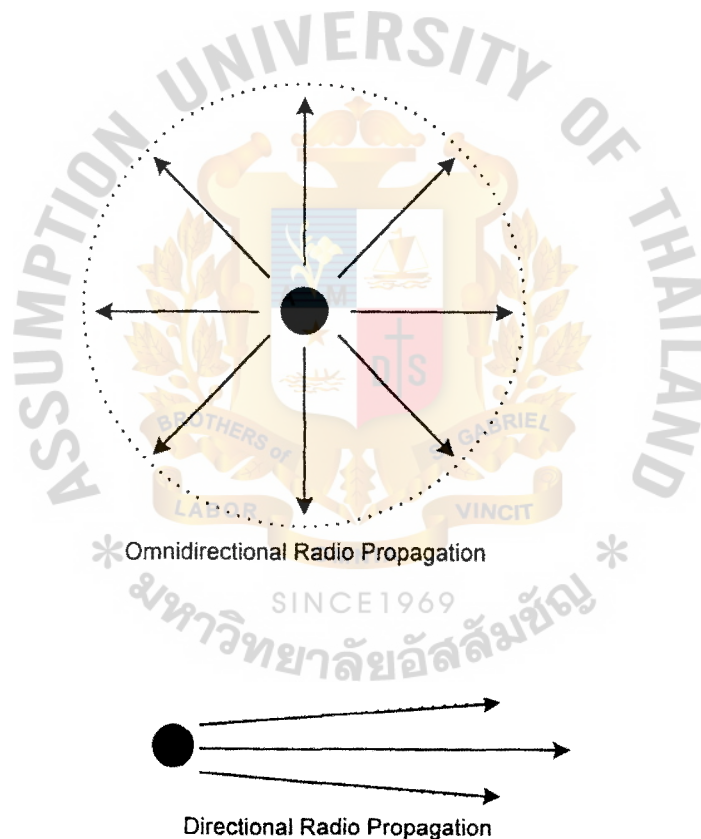
Figure 1.6 The omnidirectional versus directional antennas

A directional antenna has more gain (degree of amplification) than the omnidirectional type and is capable of propagating the modulated signal farther because it focuses the power in a single direction. The amount of gain depends on the directivity

of the antenna. An omnidirectional antenna has a gain equal to one; that is, it doesn't focus the power in any particular direction. A directional antenna, however, is considered to add gain (amplification) to the signal in certain directions.

1.3.2.5 The Communications Channel

All information systems employ a communications channel along which information flows from source to destination. Ethernet networks may utilize twisted-pair or coaxial cable. Wireless networks use air as the medium. At the earth's surface, where most wireless networks operate, pure air contains gases such as nitrogen and oxygen. This atmosphere provides an effective medium for the propagation of radio waves and infrared light. Rain, fog, and snow, however, can increase the amount of water molecules in the air and can cause significant attenuation to the propagation of modulated wireless signals. Smog clutters the air, adding attenuation to the communications channel as well. *Attenuation* is the decrease in the amplitude of the signal, and it limits the operating range of the system. The ways to combat attenuation are to either increase the transmit power of the wireless devices, which in most cases is limited by the FCC, or to incorporate special amplifiers called repeaters that receive attenuated signals, amplify them, and transmit downline to the end station or next repeater.

1.4 Radio-based Wireless LANs

The most widely sold wireless LAN products use radio waves as a medium between computers and peripherals. An advantage of radio waves over other forms of wireless connectivity is that they propagate through walls and other obstructions with fairly little attenuation. Even though several walls might separate the user from the server or

wireless bridge, users can maintain connections to the network—supporting true mobility. With radio-LAN products, a user with a portable computer can move freely through the facility while accessing data from a server or running an application.

A disadvantage of using radio waves, however, is that an organization must manage the radio waves along with other electromagnetic propagation. Medical equipment and industrial components utilize the same radio frequencies as wireless LANs, which could cause interference. An organization must determine whether potential interference is present before installing a radio-based LAN. Because radio waves penetrate walls, security may also be a problem. Unauthorized people from outside the controlled areas could receive sensitive information. However vendors often scramble the data signal to protect the information from being understood by inappropriate people.

This section discusses the following radio-based wireless LAN topics:

- ISM bands

- ISM Band Availability

- Narrow band wireless LANs

- Spread spectrum wireless LANs

- Radio signal interference

1.4.1 ISM Bands

In 1985, as an attempt to stimulate the production and use of wireless network products, the FCC modified Part 15 of the radio spectrum regulation, which governs unlicensed devices. The modification authorized wireless network products to operate in the Industrial, Scientific, and Medical (ISM) bands. The ISM frequencies are shown in figure 1.7. The FCC allows users to operate wireless products without obtaining FCC licenses if the products meet certain requirements, such as operation under 1 watt

transmitter output power. This deregulation of the frequency spectrum eliminates the need for user organizations to perform costly and time-consuming frequency planning to coordinate radio installations that will avoid interference with existing radio systems. As you can see, more bandwidth is available within the higher frequency bands, which will support higher data rates.
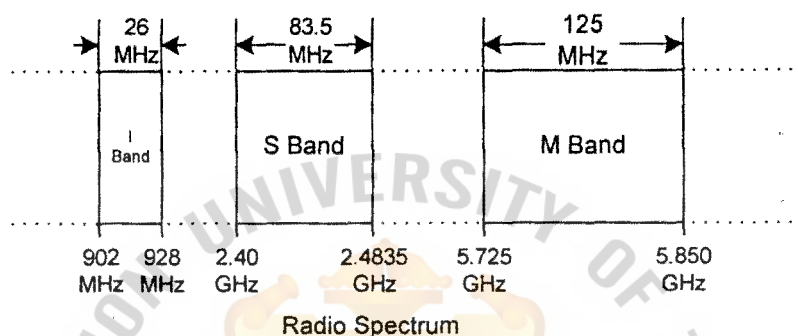
Figure 1.7 The Industrial, Scientific, and Medical (ISM) frequency bands

1.4.2 ISM Band Availability

The ISM band frequencies are not available in all parts of the world, limiting the capability to operate wireless products sold in the United States. Figure 1.8 identifies those countries that allow wireless LAN operation in the 902 MHz and 2.4 GHz ISM bands. The 2.4 GHz is the only unlicensed band available worldwide. This band was approved in North and South America in the mid-1980s and was accepted in Europe and Asia in 1995. Companies first began developing products in the 902 MHz band because manufacturing costs in this band were cheaper. The lack of availability of this band in some areas and the need for greater bandwidth, however, drove these companies to migrate many of their products to the 2.4 GHz band.

902 MHz
2.4 GHz
5.7 GHz

2.4 GHz
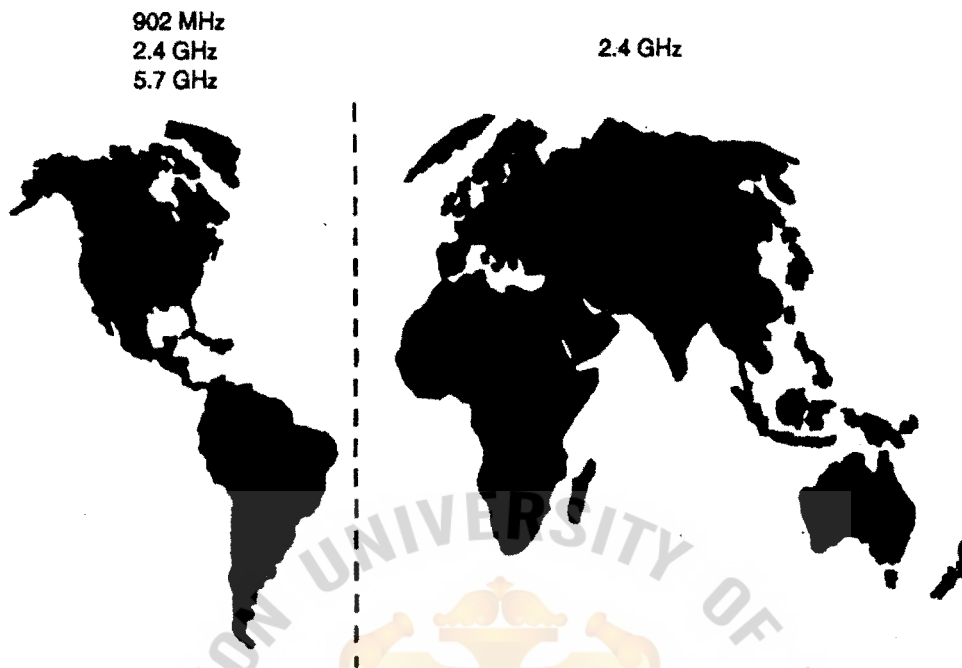
Figure 1.8 ISM spectrum availability

1.4.3 Narrow Band Modulation

Conventional radio systems, such as television and AM/FM radio, utilize narrow band modulation. These systems concentrate all their transmit power within a narrow range of frequencies, making efficient use of the radio spectrum in terms of frequency space. The idea behind most communications design is to conserve as much bandwidth as possible; therefore, most transmitted signals utilize a relatively narrow slice of the radio frequency spectrum. Other systems using the same transmit frequency, however, will cause a great deal of interference because the noise source will corrupt most of the signal. To avoid interference, the FCC requires users of narrow band systems to obtain FCC licenses to properly coordinate the operation of radios. Narrow band products thus have a strong advantage because you can be fairly assured of operating without

interference. If interference does occur, the FCC will resolve the matter. This makes narrow band modulation good for longer links covering the geographical size of a metropolitan area.

1.4.4 Spread Spectrum Modulation

Products that operate according to Part 15.247 of the FCC's Rules and Regulations must utilize spread spectrum modulation. What is spread spectrum? Spread spectrum modulation "spreads" a signal's power over a wider band of frequencies (see figure 1.9). This contradicts the desire to conserve frequency bandwidth, but the spreading process makes the data signal much less susceptible to electrical noise than conventional radio modulation techniques. Other transmission and electrical noise, typically narrow in bandwidth, will only interfere with a small portion of the spread spectrum signal, resulting in much less interference and less errors when the receiver demodulates the signal.
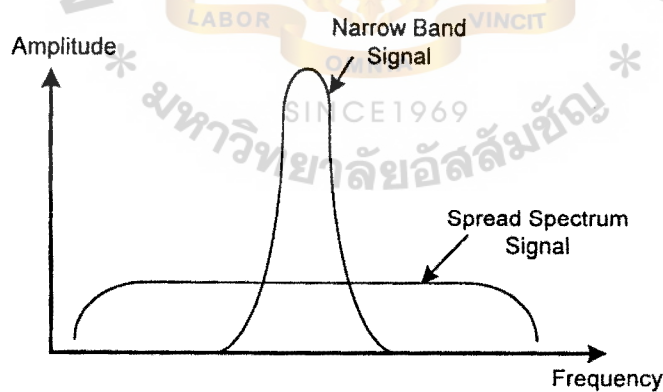
Figure 1.9 Narrow band versus spread spectrum modulation

Spread spectrum modulators use one of two methods to spread the signal over a wider area: direct sequence or frequency hopping.

1.4.5 Radio Signal Interference

The purpose of radio-based networks is to transmit and receive signals efficiently over airwaves. This process, though, makes these systems vulnerable to atmospheric noise and transmissions from other systems. In addition, these wireless networks could interfere with other radio wave equipment. As shown in figure 1.10, interference may be inward or outward.
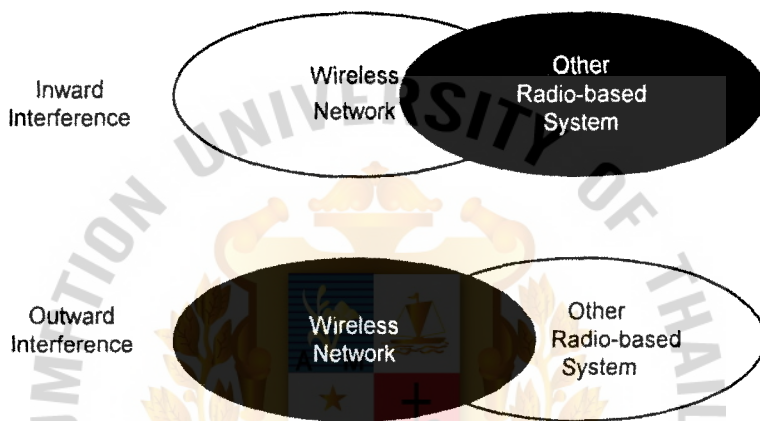
Figure 1.10 Inward and outward interference

1.4.5.1 Inward Interference

Most of us have experienced radio signal interference while talking on a wireless telephone, watching television, or listening to a radio. Someone close by might be communicating with another person via a short-wave radio system, causing harmonic frequencies that you can hear while listening to your favorite radio station. Or, a remote control car can cause static on a wireless phone while you are attempting to have a conversation. These types of interference might also disturb radio-based wireless networks in the form of inward interference.

Interference with radio-based networks is not as bad as it might seem. The products using the ISM bands incorporate spread spectrum modulation that limits the amount of damage an interfering signal causes. The spread spectrum signal covers a wide amount of bandwidth, and a typical narrow bandwidth interference only affects a small part of the information signal, resulting in few or no errors. Thus, spread spectrum-type products are highly resistant to interference. Narrowband interference with signal-to-interference ratios of less than 10 dB does not usually affect a spread spectrum transmission. Wideband interference, however, can have damaging effects on any type of radio transmission. The primary source of wideband interference is domestic microwave ovens that operate in the 2.4 GHz band.

1.4.5.2 Outward Interference

Inward interference is only half of the problem. The other half of the issue, outward interference, occurs when a wireless network's signal disrupts other systems, such as adjacent wireless LANs, navigation equipment on aircraft, and so on. This disruption results in the loss of some or all of the system's functionality. Interference is uncommon with ISM band products because they operate on such little power. The transmitting components must be very close and operating in the same bandwidth for either one to experience inward or outward interference.

1.4.5.3 Techniques for Reducing Interference

When dealing with interference, you will want to coordinate the operation of radio-based wireless network products with your company's frequency management organization, if one exists. This will avoid potential interference problems.

Another tip, especially if no frequency management organization exists within your company, is to run some tests to determine the propagation patterns within your building. These tests let you know if existing systems may interfere with, and thus block and cause delay to, your network. You will also discover whether your signal will disturb other systems.

1.5 Benefits of Wireless Networks

Companies can realize the following benefits by implementing wireless networks:

- Mobility

- Ease of installation in difficult-to-wire areas

- Reduced installation time

- Increased reliability

- Long-term cost savings

1.5.1 Mobility

User mobility indicates constant physical movement of the person and their network appliance. Many jobs require workers to be mobile, such as inventory clerks, healthcare workers, policemen, emergency care specialists, and so on. Wireline networks require a physical tether between the user's workstation and the network's resources, which makes access to these resources impossible while roaming about the building or elsewhere. As an analogy, consider talking on a wired phone having a cord connecting the handset to the telephone base station. You can utilize the phone only within the length of its cord. With a wireless cellular phone, however, you can walk freely within your office, home, or even talk to someone while driving a car. Wireless networking offers mobility to its

users much like the wireless phone, providing a constant connection to information on the network.

1.5.2 Installation in Difficult-to-Wire Areas

The implementation of wireless networks offers many tangible cost savings when performing installations in difficult-to-wire areas. If rivers, freeways, or other obstacles separate buildings you want to connect (see figure 1.11).
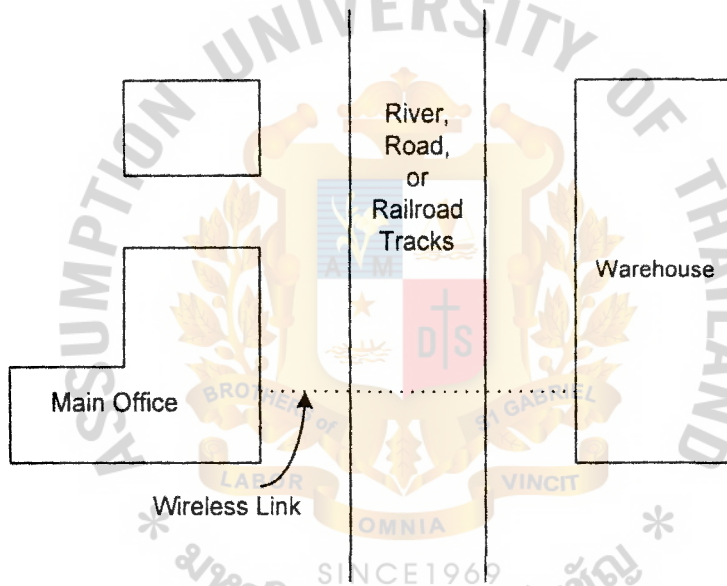
Figure 1.11 A difficult-to-wire situation

In some cases, it might be impossible to install cabling. Some municipalities, for example, may restrict you from permanently modifying older facilities with historical value. This could limit the drilling of holes in walls during the installation of LAN cabling and network outlets. In this situation, a wireless LAN might be the only solution. Right-of-way restrictions within cities and counties may also block the digging of trenches in the ground to lay optical fiber for the interconnection of networked sites.

1.5.3 Reduced Installation Time

The installation of cabling is often a time-consuming activity. For LANs, installers must pull twisted-pair wires above the ceiling and drop cables through walls to network outlets that they must affix to the wall. These tasks can take days or weeks, depending on the size of the installation. The installation of optical fiber between buildings within the same geographical area consists of digging trenches to lay the fiber or pulling the fiber through an existing conduit. You might need weeks or possibly months to receive right-of-way approvals and dig through ground and asphalt. The deployment of wireless LANs, MANs, or WANs greatly reduces the need for cable installation, making the network available for use much sooner. Thus, many countries lacking a network infrastructure have turned to wireless networking as a method of providing connectivity among computers without the expense and time associated with installing physical media.

1.5.4 Increased Reliability

A problem inherent to wired networks is the downtime due to cable faults. Moisture erodes metallic conductors. These imperfect cable splices can cause signal reflections that result in unexplainable errors. The accidental cutting of cables can also bring a network down quickly. Water intrusion can also damage communications lines during storms. These problems interfere with the users' ability to utilize network resources, causing havoc for network managers. The advantage of wireless networking, then, is experiencing fewer problems because less cable is used.

1.5.5 Long-term Cost Savings

Companies reorganize, resulting in the movement of people, new floor plans, office partitions, and other renovations. These changes often require re-cabling the network, incurring both labor and material costs. In some cases, the re-cabling costs of organizational changes are substantial, especially with large enterprise networks. The advantage of wireless networking is again based on the lack of cable—you can move the network connection by simply relocating an employee's PC.

1.6 The Future of Wireless Networks

Where is wireless networking going? What will the future bring predicting what the state of this technology and its products will be five years from now, or even a year from now. The outlook for wireless networks, however, is very good. As figure 1.12 illustrates, the maturation of standards should motivate vendors to produce new wireless products and drive the prices down to levels that are much easier to justify. The presence of standards will motivate smaller companies to manufacture wireless components because they will not need to invest large sums of money in the research and development phases of the product. These investments will have already been made and embodied within the standards, which will be available to anyone interested in building wireless network components.
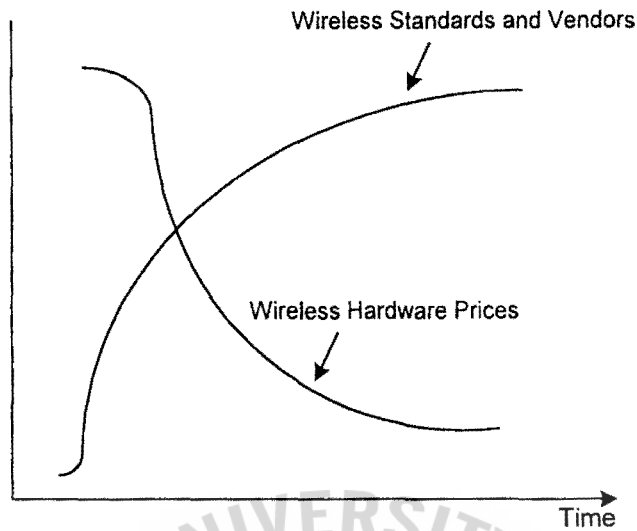
Figure 1.12 The future of wireless networking

In the next chapter, we introduce the concepts of the direct sequence spread spectrum and QPSK modulation technique that we use in our design. Chapter 3 presents the hardware design. A transmitter has been designed and built to perform QPSK modulation, direct sequence spread spectrum, and moved the baseband spread spectrum to IF frequency at 80 MHz. Chapter 4 is simulation and measurement. We design a simulation circuit and compare with the measurement result.

CHAPTER 2. THEORY OF DSSS AND QPSK

2.1 Spread Spectrum

Over the last six or seven years a new commercial marketplace has been emerging. Called spread spectrum, this field covers the art of secure digital communications that is now being exploited for commercial and industrial purposes. In the next five years hardly anyone will escape being involved, in some way, with spread spectrum communications. Applications for commercial spread spectrum range from "wireless" LAN's (computer to computer local area networks), to integrated bar code scanner/palmtop computer/radio modem devices for warehousing, to digital dispatch, to digital cellular telephone communications, to "information society" city/area/state or country wide networks for passing faxes, computer data, email, or multimedia data.

2.1.1 How Spread Spectrum Works

Spread Spectrum uses wide band, noise-like signals. Because Spread Spectrum signals are noise-like, they are hard to detect. Spread Spectrum signals are also hard to intercept or demodulate. Further, Spread Spectrum signals are harder to jam (interfere with) than narrowband signals. These low probability of intercept and anti-jam features are why the military has used Spread Spectrum for so many years. Spread signals are intentionally made to be much wider band than the information they are carrying to make them more noise-like. Spread Spectrum signals use fast codes that run many times the information bandwidth or data rate. These special "Spreading" codes are called "Pseudo Random" or "Pseudo Noise" codes.

Spread Spectrum transmitters use similar transmit power levels to narrow band transmitters. Because Spread Spectrum signals are so wide, they transmit at a much

lower spectral power density, measured in Watts per Hertz, than narrowband transmitters. This lower transmitted power density characteristic gives spread signals a big plus. Spread and narrow band signals can occupy the same band, with little or no interference. This capability is the main reason for all the interest in Spread Spectrum today.

2.1.2 More Details on Spread Spectrum

Spread spectrum communication is a means of transmitting a signal over a much wider frequency bandwidth than the minimum bandwidth required to transmit the information. If radio signals could be seen as light, a spread spectrum signal would look like a floodlight whereas a narrow-band signal would look like a spotlight of equal intensity. Unlike a narrow-band signal where the majority of the energy transmitted is concentrated at its center frequency, a spread spectrum signal uses an equal amount of energy but spreads this energy over a wider frequency band around its center frequency. This spreading process makes the signal virtually undetectable by normal receiving techniques. A spread spectrum receiver performs the opposite function, "de-spreading" the signal. Spreading a signal reduces interference because when the spread spectrum signal is compressed to its original bandwidth, the interfering noise remains spread over a large bandwidth.

A true spread spectrum system must meet two criterias:

- The transmitted bandwidth must be at least ten times the information bandwidth being sent.

- A function other than the information being sent is used to retrieve the resulting modulated RF bandwidth.

Many modulation schemes are used to generate a spread spectrum signal. The most common types are Direct Sequence, Frequency Hopping, Pulsed FM, and Time Hopping modulation. All spread spectrum modulation types use a pseudo-random binary word known as a "code sequence" to modulate the signal carrier frequency. A spread signal not possessing the exact code sequence will appear as wideband noise. This effect is the basis for what is known as "Code Division Multiple Access" or CDMA, which allows multiple code sequences or "channels" to be used simultaneously, each operating in the same frequency band. Spread spectrum signals can share frequency bands without dividing the signals into individual frequency channels as in narrowband signals.

The ability of a receiver to compress a spread signal to its original form is known as the "Process Gain." This parameter is defined as the difference between the signal-to-noise (in dB) of the transmitted bandwidth to the signal-to-noise (in dB) of the information bandwidth. Process gain can also be thought of as an improvement or "gain" realized when the spread signal is despread back into the original signal, and can be estimated by the ratio of spread signal bandwidth to the despread signal bandwidth.

$$G_P = \frac{BW_{RF}}{BW_{Info}}$$

In addition, the process gain provides "noise rejection" because all signals that do not match up with the receiver code sequence do not get increased by this gain. In fact, an interfering signal will actually be reduced. The amount of interference a system is able to withstand while producing the required output signal-to-noise ratio is known as the "jamming margin". This jamming margin is the difference between the system process gain and the sum of all system implementation losses with the output signal-to-noise ratio. The system is not expected to operate with interference greater than this

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jamming margin. However, in a supervised security system, if a loss of signal did occur it would not cause a false alarm. Instead, a trouble signal would be generated.

One way to look at spread spectrum is that it trades a wider signal bandwidth for better signal to noise ratio. Frequency hop and direct sequence are well-known techniques today. The following paragraphs will describe each of these common techniques in a little more detail and show that pseudo noise code techniques provide the common thread through all spread spectrum types.

2.1.3 Direst Sequence Spread Spectrum

Direct sequence spread spectrum combines a data signal at the sending station with a higher data rate bit sequence, which many refer to as a chipping code (also known as processing gain). A high processing gain increases the signal's resistance to interference. The minimum linear processing gain that the FCC allows is 10, and most products operate under 20. The IEEE 802.11 Working Group has set their minimum processing gain requirements at 11.

Figure 2.1 shows an example of the operation of direct sequence spread spectrum. A chipping code is assigned to represent logic "one" and "zero" data bits. As the data stream is transmitted, the corresponding code is sent. For example, the transmission of a data bit equal to "one" would result in sequence 00010011100 being sent.

```
┌─────────────────────────────────────────────────────┐
│                                                       │
│  Chipping Code:  0 = 11101100011                      │
│                  1 = 00010011100                      │
│                                                       │
│  Data Stream: 101                                     │
│                                                       │
│  Transmitted Sequence:                                │
│                                                       │
│   ┊ 00010011100 ┊ 11101100011 ┊ 00010011100 ┊        │
│   ┊             ┊             ┊             ┊        │
│   ┊      1      ┊      0      ┊      1      ┊        │
│                                                       │
└─────────────────────────────────────────────────────┘
```
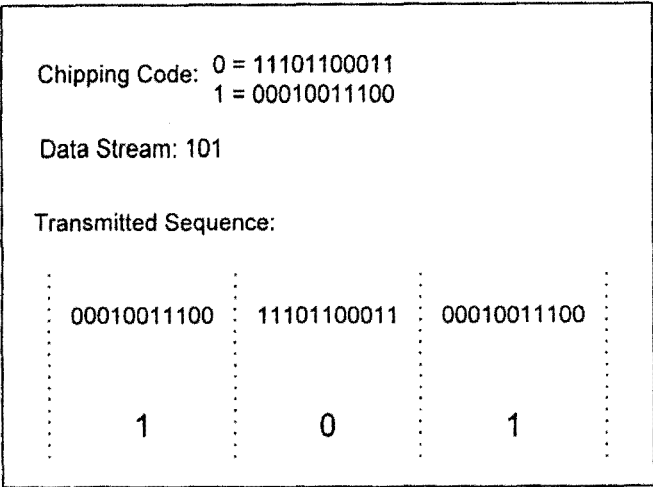
Figure 2.1 The operation of direct sequence spread spectrum.

Many direct sequence products on the market utilize more than one channel in the same area; the number of channels available, however, is limited. With direct sequence, many products operate on separate channels by slicing the frequency band into non-overlapping frequency channels. This results in the potential for several separate networks to operate without interfering with each other. To leave enough bandwidth for moderate to high data rates, however, there can only be a few channels. Proxim's ProxLink and RangeLAN product families, for example, use direct sequence technology in the 902-928 MHz frequency band. ProxLink incorporates seven different channels, and RangeLAN uses three channels.

Terms direct sequence and pseudonoise are used interchangeably here and no distinction is made between them. A typical direct-sequence transmitter is illustrated in figure 2.2. Note that it contains a PN code generator that generates the pseudonoise sequence. The binary output of this code generator is added, modulo 2, to the binary message, and sum is then used to modulate a carrier.

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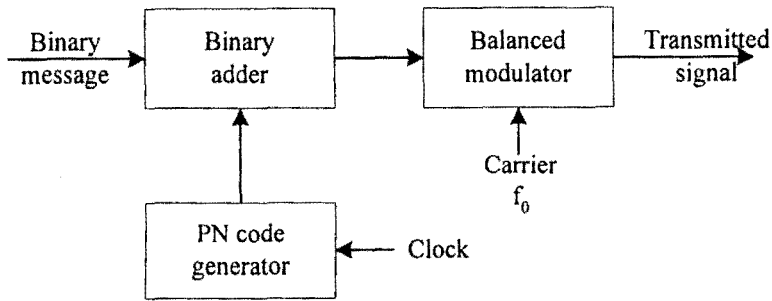
Figure 2.2 Direct-sequence transmitter.

An important parameter that is sometimes useful in specifying the performance of a spread-spectrum signal in the presence of interference is known as the processing gain. This processing gain, PG, is the frequently defined as the ratio of the signal bandwidth to the message bandwidth.

$$PG = \frac{B_s}{B_m} = \frac{2t_m}{t_1}$$

The signal bandwidth is $2/t_1$ and the bandwidth of the message B_m is simply $1/t_m$ because it is customary to use only the positive frequency portion of the spectrum in defining bandwidth.
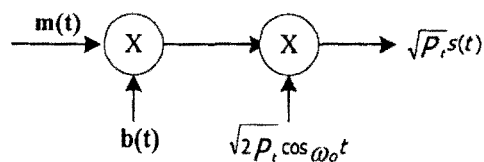
Figure 2.3 Generation of PN signals.

In figure 2.3 indicates the operations that must be performed in generating a PN signal. The quantities in this figure are defined as; m(t)=binary message, b(t)=PN code, s(t)=normalized signal.

$$s(t) = \sqrt{2}m(t)b(t)\cos \omega_o t$$

Note that the binary signals m(t) and b(t) are simply multiplied to create a new binary signal that phase-modulates the carrier. This is done by multiplying the new binary signal with a steady-state sinusoid to produce the output signal s(t). The spectral density of s(t) was obtained by assuming m(t) and b(t) to be random quantities and taking the Fourier transform of the auto-correlation function. The result is

$$S_s(f) = \frac{t_1}{2}\left\{\left[\frac{\sin \pi(f - f_0)t_1}{\pi(f - f_0)t_1}\right]^2 + \left[\frac{\sin \pi(f + f_0)t_1}{\pi(f + f_0)t_1}\right]^2\right\}$$

2.1.4 Frequency Hopping Spread Spectrum

Frequency hopping works very much like its name implies. It takes the data signal and modulates it with a carrier signal that hops from frequency-to-frequency as a function of time over a wide band of frequencies (see figure 16). A frequency hopping radio, for example, will hop the carrier frequency over the 2.4 GHz frequency band between 2.4 GHz and 2.483 GHz. A hopping code determines the frequencies the radio will transmit and in which order. To properly receive the signal, the receiver must be set to the same hopping code and "listen" to the incoming signal at the right time and correct frequency. FCC regulations require manufacturers to use 75 or more frequencies per transmission channel with a maximum dwell time (time at a particular frequency) of 400 ms. If the radio encounters interference on one frequency, then the radio will retransmit the signal on a subsequent hop on another frequency.
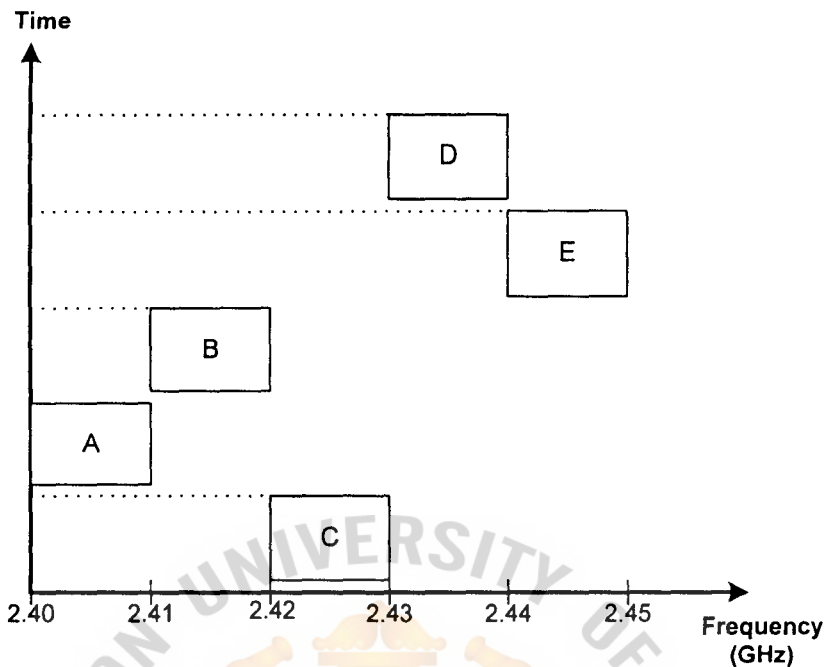
Figure 2.4 A frequency hopping spread spectrum.

The frequency hopping technique reduces interference because the propagation from narrow band systems will only affect the spread spectrum signal when it is using the frequency of the narrow band signal. Thus, the aggregate interference will be very low, resulting in little or no bit errors. Operating radios can use spread spectrum within the same frequency band and not interfere, assuming they each use a different hopping pattern. While one radio is transmitting at one particular frequency, the other radio uses a different frequency. A set of hopping codes that never use the same frequencies at the same time is considered orthogonal. Some vendors allow the user to choose the channel (a particular hopping code) through software that the radio will operate on, all users within the same local network, however, have to use the same code. This does give you the ability, though, to have wireless LANs within close proximity to each other operate within the same band and not interfere with each other, as long as you assign them

orthogonal hopping codes. The FCC's requirement for the number of different transmission frequencies allows frequency-hopping radios to have many non-interfering channels.

2.1.5 Direct Sequence vs. Frequency Hopping

The direct sequence and frequency hopping are the most commonly used methods for the spread spectrum technology. Although the basic idea is the same, these two methods have many distinctive characteristics that result in complete different radio performances. The user should, based on his need and application, determine which method is best for him.

2.1.5.1 The Basics

The carrier of the direct sequence radio stays at a fixed frequency. The narrow band informations are spread out into a much larger (at least 10 times) bandwidth by using a pseudo-random chip sequence. The generation of the direct sequence spread spectrum signal (spreading) can be shown as follows,
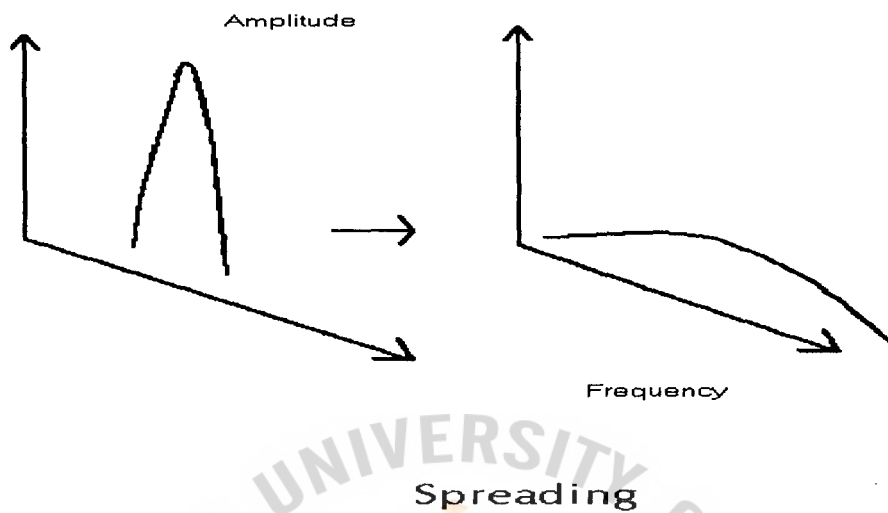
Figure 2.5 Spreading of direct sequence signal

Please note that in the above figure, the narrowband signal and the spread spectrum signal both use the same amount of transmit power and carry the same information. However, the power density of the spread spectrum signal is much lower than the narrowband signal. As a result, it is more difficult to detect the presence of the spread spectrum signal. The power density is the amount of power over a certain frequency. In this case, the narrowband signal's power density is 10 times higher than the spread spectrum signal, assuming the spread ratio is 10.

At the receiving end, the spread spectrum signal is despread to generate the original narrowband signal as shown in the following figure,
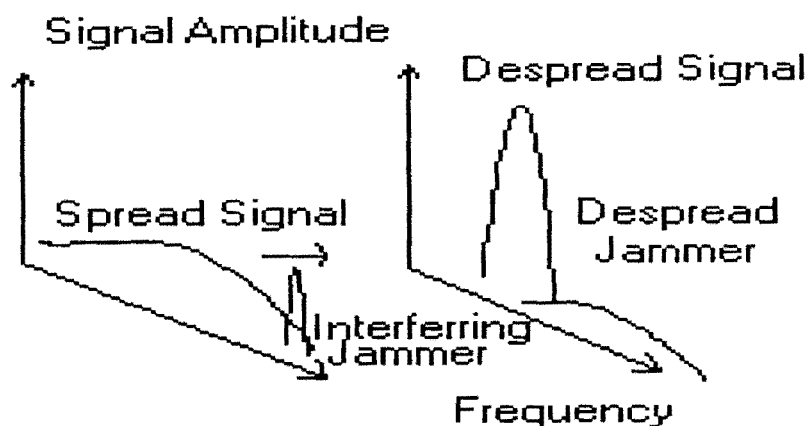
Figure 2.6 Despreading of direct sequence signal

If there is an interference jammer in the same band, it will spread out during the despreading. As a result, its impact is greatly reduced. This is the way that the direct sequence spread spectrum radio fights the interference. It spreads out the offending jammer by the spreading factor, which are at least 10. In other words, the offending jammer's amplitude is greatly reduced by at least 90%.

The frequencies hopping achieve the same result by using different carrier frequency at different time. Its carrier will hop around within the band so that hopefully it will avoid the jammer at some frequencies. The frequency hopper is more popular and is the only way to survive in the 2.45 GHz band because of the leakages from the microwave oven (from 2.4 to 2.5 GHz) sometimes exceeds 10W! The need for frequency hopper in 915 MHz band is not there because there is no legal big jammer in this frequency. The frequency hopping can be shown as the following figure,
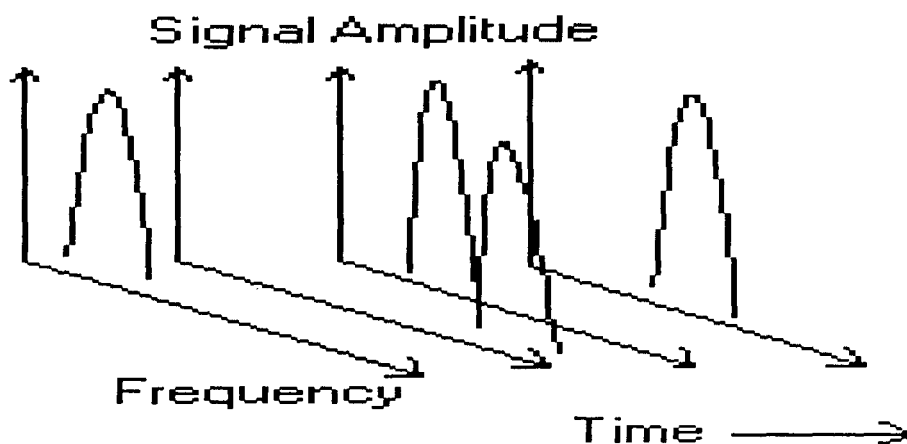
Figure 2.7 Frequency hopping signal

2.1.5.2 Comparisons

- The frequency hopping technique does not spread the signal, as a result, there is no processing gain. The processing gain is the increase in power density when the signal is despread and it will improve the received signal's S/N ratio. In other words, the frequency hopper needs to put out more power in order to have the same S/N as a direct sequence radio.

- The frequency hopper is also more difficult to synchronize the receiver to the transmitter because both the time and frequency need to be in tune. While in a direct sequence radio, only the timing of the chips needs to be synchronized. The frequency hopper will need to spend more time to search the signal and lock to it. As a result, the latency time is usually longer. While a direct sequence radio can lock in the chip sequence in just a few bits.

- Usually, to make the initial synchronization possible, the frequency hopper will park at a fixed frequency before hopping or communications begin. If the jammer happens to locate at the same frequency as the parking frequency, the hopper will not be able to hop at all! And once it hops, it will be very difficult, if not impossible to re-synchronize if the receiver ever lost the sync.

- The hopper is usually cost more and more complicated than the direct sequence radio because it needs extra hopping and synchronizing circuits to implement the synchronization algorithm.

- The frequency hopper, however, is better than the direct sequence radio when dealing with multipath. This is because that the hopper does not stay at the same frequency and a null at one frequency is usually not a null at another frequency if it is not too close to the original frequency. So a hopper can usually survive the multipath better than direct sequence radio.

- The frequency hopper can usually carry more data than the direct sequence radio because the signal is narrowband.

- In the 915 MHz band, the hopper does not have any edge over the direct sequence in dealing the interference because it has the same effect on both systems. One reduces its impact by avoiding the jammer and the other by spreading or diluting offending jammer. The net effect is the same.

- When two signals collide, the stronger one may survive regardless of the kind of signal. In this band, all radio must not exceed the same power density limit set by the FCC. In other words, all radios are equal when interfereing with one another. The best strategy to prevent interference is to make the important radios close to each other (strengthen the link) and prevent using frequency hopper because they are guaranteed to interfere with other radios!

- The hopper itself will also suffer when it interferes with other radio. Which system can survive better depends upon which can suffer more data loss. In general, a voice system can survive an error rate as high as 10^{-2} while a data system must have an error rate better than 10^{-4}. Voice system can tolerate more data loss because human brain can "guess" between the words while a dumb microprocessor can't! As a result, the frequency hopper is more popular for voice than data communications.

2.1.5.3 Summary

The strength and weakness of the direct sequence and the frequency hopper at 915 MHz band can be listed as follows.

Direct Sequence	Frequency Hopper
Easy and Simple	Complicated
Use lower power	Use higher power
Short Latency Time	Long Latency Time
Quick Lock In	Slow Lock In
Short Indoor Range	Long Indoor Range
Low Data Rate	High Data Rate

Table 2.1 Comparison of DSSS & FHSS

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2.2 Modulation

Modulation is the process of encoding information from a message source in a manner suitable for transmission. It generally involves translating a baseband message signal (called the source) to a bandpass signal at frequencies that are very high when compared to the baseband frequency. The bandpass signal is called the modulated signal and the baseband message signal is called the modulating signal. Modulation may be done by varying the amplitude, phase, or frequency of a high frequency carrier in accordance with the amplitude of the message signal. Demodulation is the process of extracting the baseband message from the carrier so that it may be processed and interpreted by the intended by the intended receiver (also called the sink).

2.2.1 Type of modulation

Digital modulation transforms input digital signals into wave forms that are compatible with the nature of the communications channel. RF communications channels use bandpass modulation where the characteristics of a carrier wave are modified to carry the desired information. There are two major categories of digital modulation. One category uses a constant amplitude carrier and carries the information in phase or frequency variations, known as phase shift keying (PSK) or frequency shift keying (FSK). The vast majority of frequency hopping Wireless LAN and spread spectrum-based systems today employ simple FSK modulation schemes. The other category conveys the information in carrier amplitude variations and is known as amplitude shift keying (ASK). More advanced modulation techniques convey multiple bits of information simultaneously by providing multiple states in each symbol of transmitted information. Quadrature phase shift keying (QPSK) conveys 2 bits per symbol and is prevalent in satellite communication.

2.2.2 QPSK Modulation

In Quadrature Phase Shift Keying (QPSK) modulation, a cosine carrier is varied in phase while keeping a constant amplitude and frequency. The term "quadrature" implies that there are four possible phases (4-PSK) which the carrier can have at a given time, as shown at right on the characteristic *constellation* for this modulation type. The four phases are labeled {A,B,C,D} corresponding to one of {0,90,180,270} degrees.
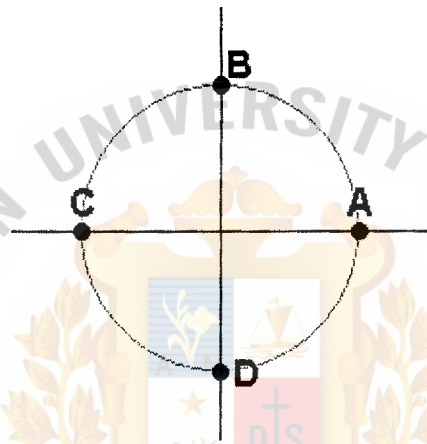
Figure 2.8 Four phases of QPSK modulation

In QPSK, information is conveyed through phase variations. In each time period, the phase can change once. Since there are four possible phases, there are 2 bits of information conveyed within each time slot. The rate of change (baud) in this signal determines the signal bandwidth, but the throughput or bit rate for QPSK is twice the baud rate.

2.2.3 Transmitting Data Using QPSK

Each of the four possible phase changes is assigned a specific two-bit value, or dibit. For example, the relationship between phase changes and dibits is given by:

PHASE CHANGE (Degrees)	Example state change	Dibit
0	A-to-A	01
90	A-to-B	00
180	B-to-D	10
270	D-to-C	11

Table 2.2 Relationship between phase changes and dibits

In the figure below, a carrier is shifted through the phases **ADABAADCCA**.
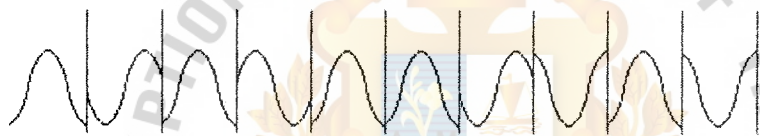
Figure 2.9 Example of QPSK modulation

Two bits of information are conveyed in the transition between time slots.

The signal has undergone the following phase transitions:

PHASE	A	D	A	B	A	A	D	C	C	A	...
Change	-	A-to-D	D-to-A	A-to-B	B-to-A	A-to-A	A-to-D	D-to-C	C-to-C	C-to-A	...
Degrees	-	270	90	90	270	0	270	270	0	180	
Dibit	-	11	00	00	11	01	11	11	01	10	

Table 2.3 Phase transition to dibit

The corresponding information transmitted is therefore: **110000110111110110**

2.3 The IEEE 802.11 Wireless Standard

The IEEE 802.11 specification is a wireless LAN standard developed by the IEEE (Institute of Electrical and Electronic Engineering) committee in order to specify an "over the air" interface between a wireless client and a base station or Access Point, as well as among wireless clients.

2.3.1 IEEE 802.11 Physical Layer

The physical Layer in any network defines the modulation and signaling characteristics for the transmission of data. At the physical layer, two RF transmission methods and one infrared are defined. The RF transmission standards in the standard are Frequency Hopping Spread Spectrum (FHSS) and Direct Sequence Spread Spectrum (DSSS). Both architectures are defined to operation in the 2.4 GHz frequency band typically occupying the 83 MHz of bandwidth from 2.400 GHz to 2.483 GHz. The radiated power is limited to 1W for the United States, 10mW per 1MHz in Europe and 10mW for Japan. The physical layer data rate for FHSS system is 1 Mbps. For DSSS both 1 Mbps and 2 Mbps data rates are supported.

2.3.2 Direct Sequence Spread Spectrum (DSSS) Physical Layer

The DSSS physical layer uses an 11-bit Barker Sequence to spread the data before it is transmitted. Each bit transmitted is modulated by the 11-bit sequence. This process spreads the RF energy across a wider bandwidth than would be required to transmit the raw data. The processing gain of the system is defined as 10x the log of the ratio of spreading rate (also know as the chip rate) to the data. The receiver despreads the RF input to recover the original data. The advantage of this technique is that it reduces the effect of narrowband sources of interference. This sequence provides 10.4dB of

processing gain which meets the minimum requirements for the rules set by the FCC. Direct Sequence Spread Spectrum uses technique of differential BPSK (DBPSK) and DQPSK for modulation.

2.3.3 IEEE 802.11 MAC Layer

The MAC layer specification for 802.11 has similarities to the 802.3 Ethernet wired line standard. The protocol for 802.11 uses a protocol scheme know as carrier-sense, multiple access, collision avoidance (CSMA/CA). This protocol avoids collisions instead of detecting a collision like the algorithm used in 802.3. It is difficult to detect collisions in an RF transmission network and it is for this reason that collision avoidance is used. The MAC layer operates together with the physical layer by sampling the energy over the medium transmitting data. The physical layer uses a clear channel assessment (CCA) algorithm to determine if the channel is clear. This is accomplished by measuring the RF energy at the antenna and determining the strength of the received signal. This measured signal is commonly known as RSSI. If the received signal strength is below a specified threshold the channel is declared clear and the MAC layer is given the clear channel status for data transmission. If the RF energy is above the threshold, data transmissions are deferred in accordance with the protocol rules. The CSMA/CA protocol allows for options that can minimize collisions by using request to send (RTS), clear-to-send (CTS), data and acknowledge (ACK) transmission frames, in a sequential fashion.

CHAPTER 3. CIRCUIT DIAGRAM AND DESCRIPTION

3.1 Overview

We design physical layer WLAN card in baseband part. In this card, we design to operate transmit and receive signal at the IF frequency of 80 MHz by receiving data from PC medium access control (MAC) layer. In this design we use HFA3824 Direct Sequence Spread Spectrum (DSSS) Baseband Processor and HFA3724 400 MHz Quadrature IF Modulator/Demodulator. We use technique of DSSS and QPSK modulation technique.

3.2 General Specification

- Data Rate ....2 Mbps DQPSK

- IF frequency ....80 MHz

- IF Bandwidth ....17 MHz

- RX/TX Switching Speed ....2 μs

- Operating Voltage .... 4.5 VDC – 5.5 VDC
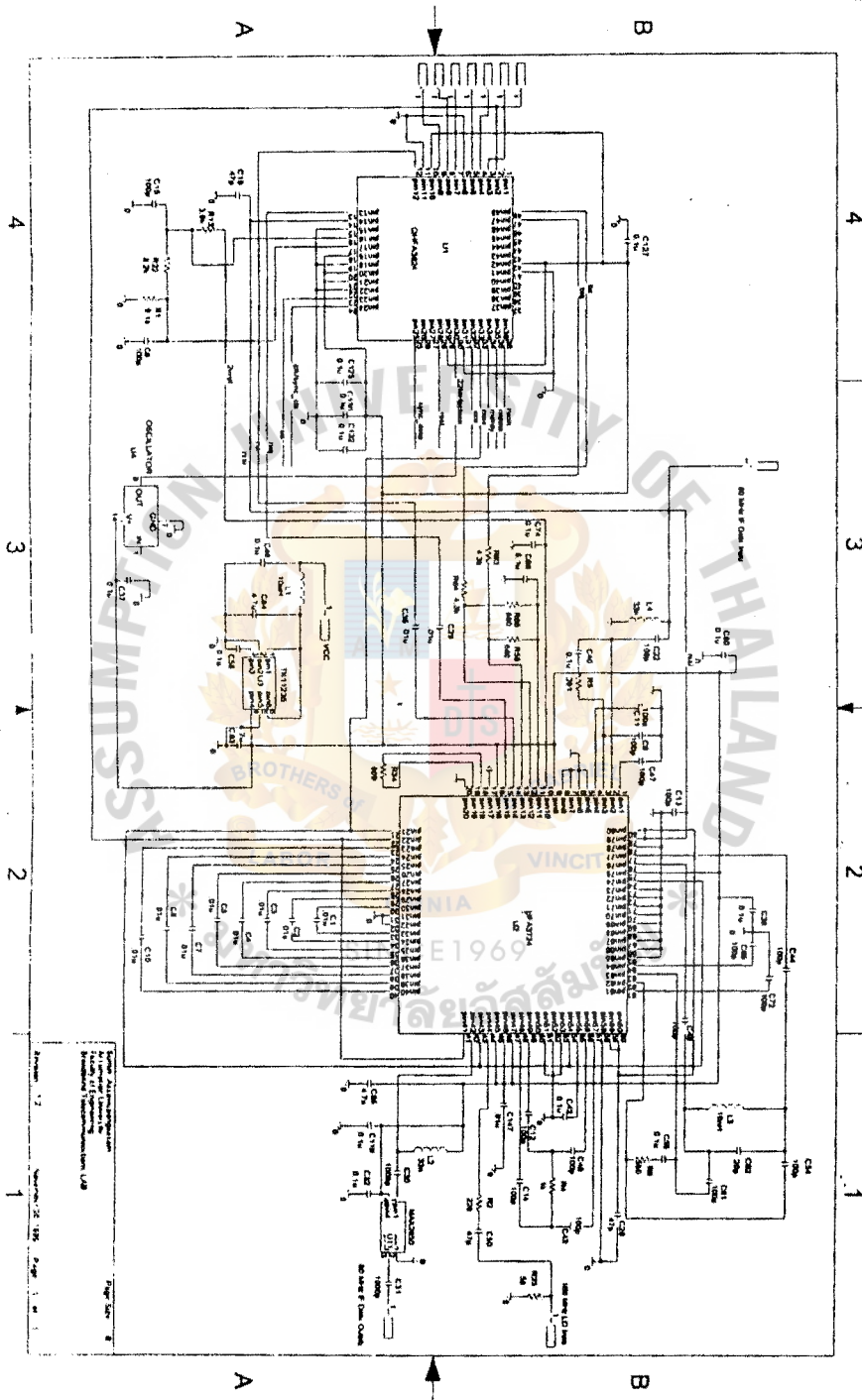
3.3 Circuit Diagram & PCB Layout

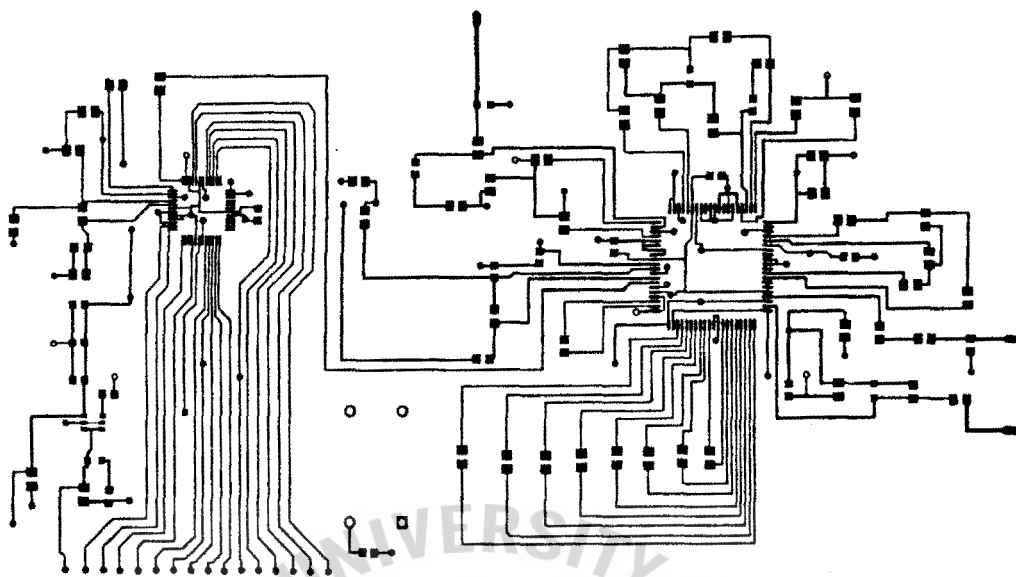Figure 3.1 Circuit Design Diagram

Figure 3.2 PCB Design (Front Side)
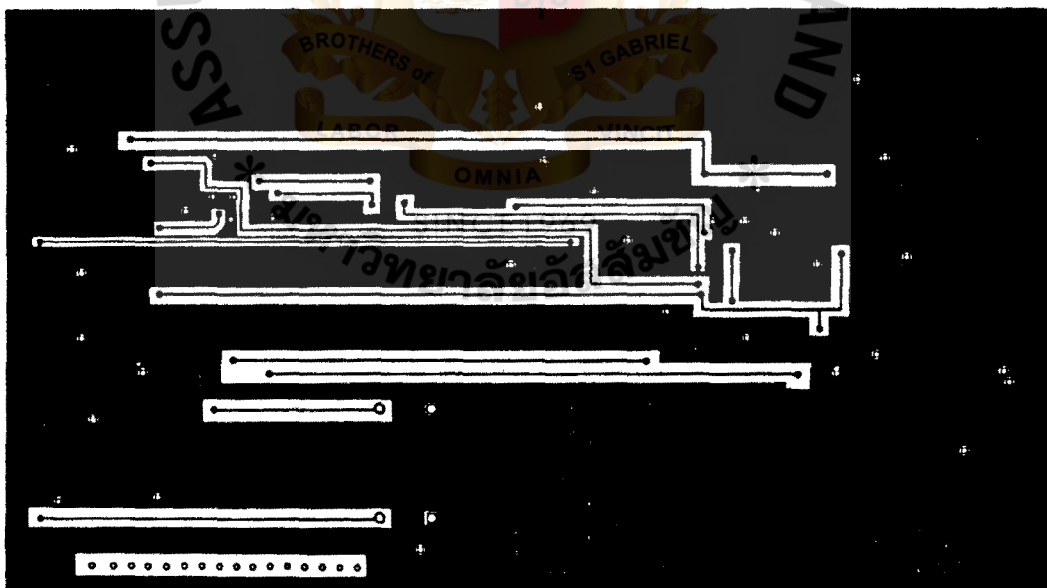
Figure 3.3 PCB Design (Back Side)

3.3.1 Transmit Processing

Data from the host computer is sent to the MAC via the PC card interface. Prior to any communications, however, the MAC sends a Request to Sent (RTS) packet to the other end of the link and receives a Clear to Send (CTS) packet. The MAC then formats the payload data packet and sends it on to the HFA3824 Baseband Processor which clocks it in. The HFA3824 Baseband Processor adds preamble and header, scrambles the packet and differentially encodes it before applying the spread spectrum modulation. We use technique of cyclic redundancy check for data error detection. The data use DQPSK modulated at 1 Msps and is a baseband quadrature signal with I and Q components. The QPSK spreading is an 11 chip Barker sequence that is clocked at around 11 MHz and is modulated with the I and Q data components. These are then output to the HFA3724 as CMOS logic signals.

Transmit quadrature single-bit digital inputs are applied to the HFA3724 Quadrature IF Modulator/Demodulator from the HFA3824 Baseband Processor. These inputs are attenuated and DC coupled to the fifth order Butterworth low pass filters, which are used to provide shaping of the phase shift keyed (PSK) signal. The low pass filters provide initial shaping of the PSK waveform. Final shaping is provided by a transmit IF filter. The low pass filter outputs are off-chip AC coupled to the quadrature up-converter in the HFA3724. The twice IF frequency LO is used in this up-conversion. The IF output of the HFA3724 is reactively matched with a 50 Ω resistive load presented to the HFA3724. A shunt inductor, in parallel with a resistor, is used to provide this match, negate the effects of board and component capacitance, and provide a DC return to VCC to prevent saturation in the IF output stage of the HFA3724.

3.3.2 Receive Processing

In receive mode, the HFA3724 Quadrature IF Modulator/Demodulator provides two limiting amplifiers, a quadrature baseband demodulator, and two baseband low pass filters.

At the output of the limiters, a 200mVp-p differential signal level is maintained under all input conditions. This limited signal is then mixed in quadrature to baseband in the HFA3724 Quadrature IF Modulator/Demodulator. The LO needed for the quadrature mixing is applied at twice the IF frequency, or 160 MHz. A divide by two circuit then provides an accurate quadrature LO for the mixers. The baseband outputs of the quadrature mixers are AC coupled off-chip to the integrated fifth order Butterworth filters. The output levels of the low pass filters are norminally 500 mVp-p, and are intended to be AC coupled to the HFA3824 Baseband Processor.

At the input to the HFA3824 Baseband Processor, the quadrature signals are analog to digital converted in wideband 3 bit converters. A 24 MHz crystal oscillator is used to provide the main clock for the HFA3824. The signals are spread spectrum with no DC term, so it is feasible to AC couple the signals to the ADCs and avoid DC bias offsets. The signal at this point has been limited to a constant IF amplitude and then passed through two separate mixer and low pass filter paths. The component variations in these two paths can introduce offsets in amplitude and phase. The maximum amplitude variation is 2dB and the maximum phase balance variation is 4 degrees. Since the signal is limited, the IF signals will have low peak to average ratios even with noise as an input. The I and Q signals will have sinusoidal properties with PSK modulation imposed. It is their combined vector magnitude that is limited, not their individual amplitudes. To optimize the demodulator's performance, the ADCs are operated at the point where they are at full scale on either I or Q one third of the time.

To maintain this operating point in the face of component variations, there is an optional active adjustment of the ADC reference voltage by feedback. This avoids the necessity of allowing extra headroom for the variation. The adjustment circuit is very slow and averages the energy from the two channels over both packet and noise conditions.

The HFA3824A Baseband Processor correlates the PN spreading to remove it and to uncover the differential QPSK data. The processor initially uses differential detection to identify and lock onto the signal. It then makes measurements of the carrier and symbol timing phase and frequency and uses these to initialize tracking loops for fast acquisition. Once demodulating and tracking, the processor uses coherent demodulation for best performance.

The HFA3824A Baseband Processor provides differential decoding and descrambling of the data to prepare it for the Media Access Controller (MAC). All packet signals have a preamble followed by a header containing a start frame delimiter (SFD), other signal related data and a cyclic redundancy check (CRC). The MAC processes the header data to locate the SFD, determine the mode and length of the incoming message and to check the CRC. The MAC then processes the packet data and sends it on through the PC card interface to the host computer. The MAC checks the packet data CRC to determine the data purity. If corrupted data is received, a retransmission is requested by the MAC which handles the physical layer link protocols.

3.4 HFA3824 Direct Sequence Spread Spectrum Baseband Processor

3.4.1 Features

- Complete DSSS Baseband Processor

- High Data Rate ……………………………………… up to 2 Mbps

- Processing Gain …………………………………up to 12 dB

- Programmable PN Code ……………………….. up to 16 Bits

- Modulation Method ……………………………. DBPSK or DQPSK

- Supports Full or Half Duplex Operations
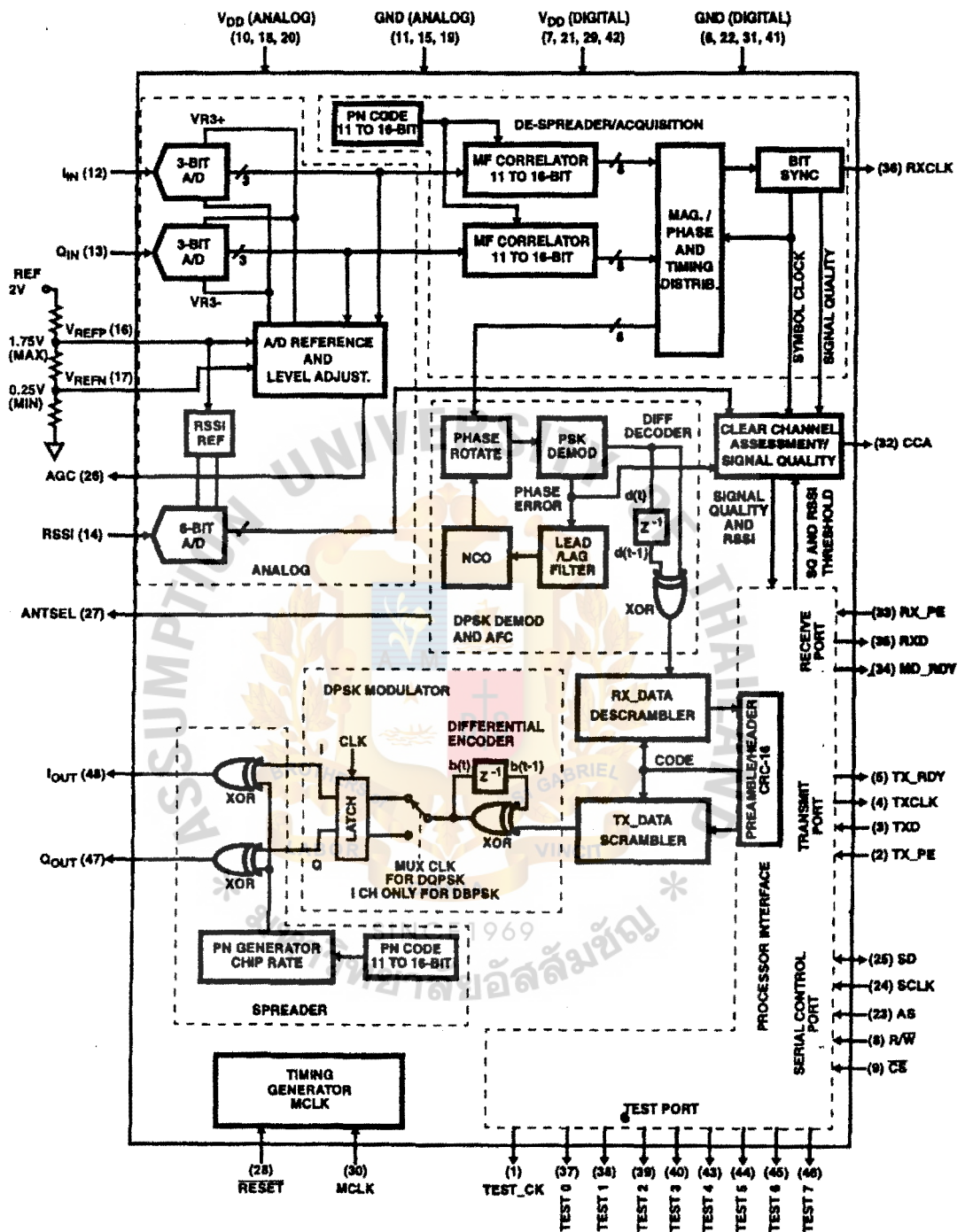
Figure 3.4 Circuit diagram of HFA3824

Pin Description

NAME	PIN	TYPE I/O	DESCRIPTION
V_{DDA} (Analog)	10, 18, 20	Power	DC power supply 2.7V - 5.5V (Not Hardwire Together On Chip).
V_{DD} (Digital)	7, 21, 29, 42	Power	DC power supply 2.7V - 5.5V
GND (Analog)	11, 15, 19	Ground	DC power supply 2.7V - 5.5V, ground (Not Hardwire Together On Chip).
GND (Digital)	6, 22, 31, 41	Ground	DC power supply 2.7V - 5.5V, ground.
V_{REFN}	17	I	"Negative" voltage reference for ADC's (I and Q) [Relative to V_{REFP}]
V_{REFP}	16	I	"Positive" voltage reference for ADC's (I, Q and RSSI)
I_{IN}	12	I	Analog input to the internal 3-bit A/D of the In-phase received data.
Q_{IN}	13	I	Analog input to the internal 3-bit A/D of the Quadrature received data.
RSSI	14	I	Receive Signal Strength Indicator Analog input.
A/D_CAL	26	O	This signal is used internally as part of the I and Q ADC calibration circuit. When the ADC calibration circuit is active, the voltage references of the ADCs are adjusted to maintain the outputs of the ADCs in their optimum range. A logic 1 on this pin indicates that one or both of the ADC outputs are at their full scale value. This signal can be integrated externally as a control voltage for an external AGC.
TX_PE	2	I	When active, the transmitter is configured to be operational, otherwise the transmitter is in standby mode. TX_PE is an input from the external Media Access Controller (MAC) or network processor to the HFA3824. The rising edge of TX_PE will start the internal transmit state machine and the falling edge will inhibit the state machine. TX_PE envelopes the transmit data.
TXD	3	I	TXD is an input, used to transfer serial Data or Preamble/Header information bits from the MAC or network processor to the HFA3824. The data is received serially with the LSB first. The data is clocked in the HFA3824 at the falling edge of TXCLK.
TXCLK	4	O	TXCLK is a clock output used to receive the data on the TXD from the MAC or network processor to the HFA3824, synchronously. Transmit data on the TXD bus is clocked into the HFA3824 on the falling edge. The clocking edge is also programmable to be on either phase of the clock. The rate of the clock will be depending upon the modulation type and data rate that is programmed in the signalling field of the header.
TX_RDY	5	O	When the HFA3824 is configured to generate the preamble and Header information internally, TX_RDY is an output to the external network processor indicating that Preamble and Header information has been generated and that the HFA3824 is ready to receive the data packet from the network processor over the TXD serial bus. The TX_RDY returns to the inactive state when the TX_PE goes inactive indicating the end of the data transmission. TX_RDY is an active high signal. This signal is meaningful only when the HFA3824 generates its own preamble.
CCA	32	O	Clear Channel Assessment (CCA) is an output used to signal that the channel is clear to transmit. The CCA algorithm is user programmable and makes its decision as a function of RSSI, Energy detect (ED), Carrier Sense (CRS) and the CCA watch dog timer. The CCA algorithm and its programmable features are described in the data sheet. Logic 0 = Channel is clear to transmit. Logic 1 = Channel is NOT clear to transmit (busy). This polarity is programmable and can be inverted.
RXD	35	O	RXD is an output to the external network processor transferring demodulated Header information and data in a serial format. The data is sent serially with the LSB first. The data is frame aligned with MD_RDY.
RXCLK	36	O	RXCLK is the clock output bit clock. This clock is used to transfer Header information and data through the RXD serial bus to the network processor. This clock reflects the bit rate in use. RXCLK will be held to a logic "0" state during the acquisition process. RXCLK becomes active when the HFA3824 enters in the data mode. This occurs once bit sync is declared and a valid signal quality estimate is made, when comparing the programmed signal quality thresholds.

Table 3.1 Pin description of HFA3824

NAME	PIN	TYPE I/O	DESCRIPTION
MD_RDY	34	O	MD_RDY is an output signal to the network processor, indicating a data packet is ready to be transferred to the processor. MD_RDY is an active high signal and it envelopes the data transfer over the RXD serial bus. MD_RDY returns to its inactive state when there is no more receiver data, when the programmable data length counter reaches its value or when the link has been interrupted. MD_RDY remains inactive during preamble synchronization.
RX_PE	33	I	When active, receiver is configured to be operational, otherwise receiver is in standby mode. This is an active high input signal. In standby, all A/D converters are disabled.
ANTSEL	27	O	The antenna select signal changes state as the receiver switches from antenna to antenna during the acquisition process in the antenna diversity mode.
SD	25	I/O	SD is a serial bi-directional data bus which is used to transfer address and data to/from the internal registers. The bit ordering of an 8-bit word is MSB first. The first 8 bits during transfers indicate the register address immediately followed by 8 more bits representing the data that needs to be written or read at that register.
SCLK	24	I	SCLK is the clock for the SD serial bus. The data on SD is clocked at the rising edge. SCLK is an input clock and it is asynchronous to the internal master clock (MCLK) The maximum rate of this clock is 11MHz or one half the master clock frequency, whichever is lower.
AS	23	I	AS is an address strobe used to envelope the Address or the data on SD. Logic 1 = envelopes the address bits. Logic 0 = envelopes the data bits.
R/$\overline{\text{W}}$	8	I	R/$\overline{\text{W}}$ is an input to the HFA3824 used to change the direction of the SD bus when reading or writing data on the SD bus. R/$\overline{\text{W}}$ must be set up prior to the rising edge of SCLK. A high level indicates read while a low level is a write.
$\overline{\text{CS}}$	9	I	$\overline{\text{CS}}$ is a Chip select for the device to activate the serial control port. The $\overline{\text{CS}}$ doesn't impact any of the other interface ports and signals, i.e. the TX or RX ports and interface signals. This is an active low signal. When inactive SD, SCLK, AS and R/$\overline{\text{W}}$ become "don't care" signals.
TEST 0-7	37, 38, 39, 40, 43, 44, 45, 46	I/O	This is a data port that can be programmed to bring out internal signals or data for monitoring. These bits are primarily reserved by the manufacturer for testing. A further description of the test port is given at the appropriate section of this data sheet. The direction of these pins are not established until programming of test registers is complete.
TEST_CK	1	O	This is the clock that is used in conjunction with the data that is being output from the test bus (TEST 0-7).
$\overline{\text{RESET}}$	28	I	Master reset for device. When active TX and RX functions are disabled. If $\overline{\text{RESET}}$ is kept low the HFA3824 goes into the power standby mode. $\overline{\text{RESET}}$ does not alter any of the configuration register values nor it presets any of the registers into default values. Device requires programming upon power-up.
MCLK	30	I	Master Clock for device. The maximum frequency of this clock is 44MHz. This is used internally to generate all other internal necessary clocks and is divided by 1, 2, 4, or 8 for the transceiver clocks.
I_{OUT}	48	O	TX Spread baseband I digital output data. Data is output at the programmed chip rate.
Q_{OUT}	47	O	TX Spread baseband Q digital output data. Data is output at the programmed chip rate.

Table 3.1(Cont.). Pin description of HFA3824

3.4.2 Description

The HFA3824 has on-board ADC's for analog I and Q inputs. Differential phase shift keying modulation schemes DQPSK, with optional data scrambling capability, are combined with a programmable PN sequence of 11 bits. Built-in flexibility allows the HFA3824 to be configured through a general purpose control bus, for a wide range of applications.

3.4.3 External Interfaces description

There are three primary digital interface ports for the HFA3824 that are used for configuration and during normal operation of the device. These ports are:

- The *TX Port*, which is used to accept the data that needs to be transmitted from the network processor.

- The *RX Port*, which is used to output the received demodulated data to the network processor.

- The *Control Port*, which is used to configure, write and/or read the status of the internal HFA3824 registers.
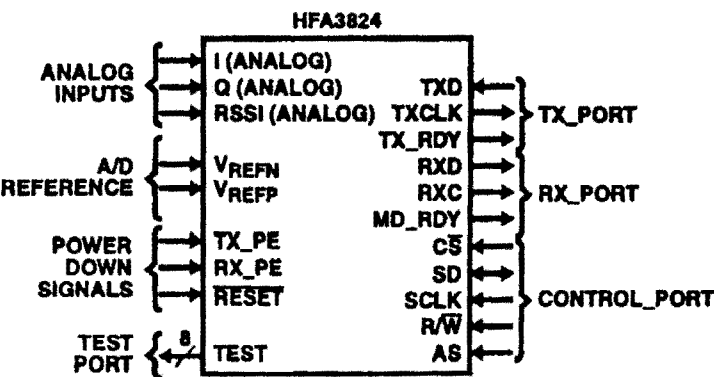

Figure 3.5 External interface

3.4.3.1 Control Port

The serial control port is used to serially write and read data to/from the device. This serial port can operate up to a 11MHz rate or the maximum master clock rate of the device, MCLK (whichever is lower). MCLK must be running and RESET must be inactive during programming. This port is used to program and to read all internal registers. The first 8 bits always represent the address followed immediately by the 8 data bits for that register. The two LSBs of address are don't care. The serial transfers are accomplished through the serial data pin (SD). SD is a bidirectional serial data bus. Address Strobe (AS), Chip Select (CS), and Read/Write (R/W) are also required as handshake signals for this port. The clock used in conjunction with the address and data on SD is SCLK. This clock is provided by the external source and it is an input to the HFA3824. The timing relationships of these signals are illustrated on figures 3.6 and 3.7. AS is active high during the clocking of the address bits. R/W is high when data is to be read, and low when it is to be written. CS must be sampled high to initialize state machine. CS must be active (low) during the entire data transfer cycle. CS selects the device. The serial control port operates asynchronously from the TX and RX ports and it can accomplish data transfers independent of the activity at the other digital or analog ports. CS does not effect the TX or RX operation of the device; impacting only the operation of the control port. The HFA3824 has 57 internal registers that can be configured through the control port.
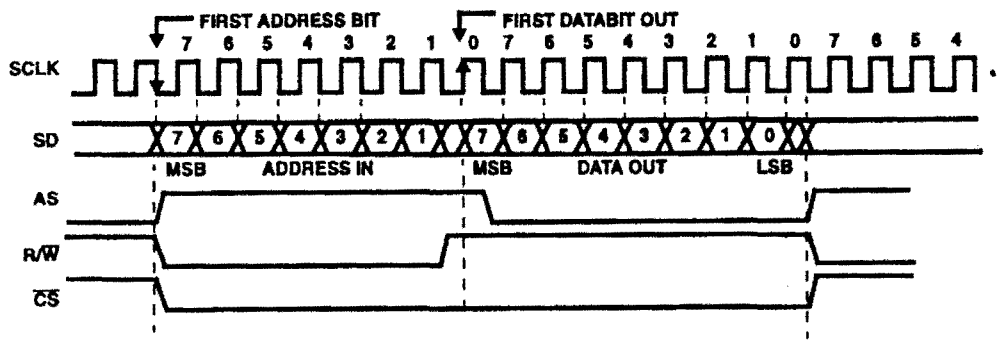
Figure 3.6 Control port read timing
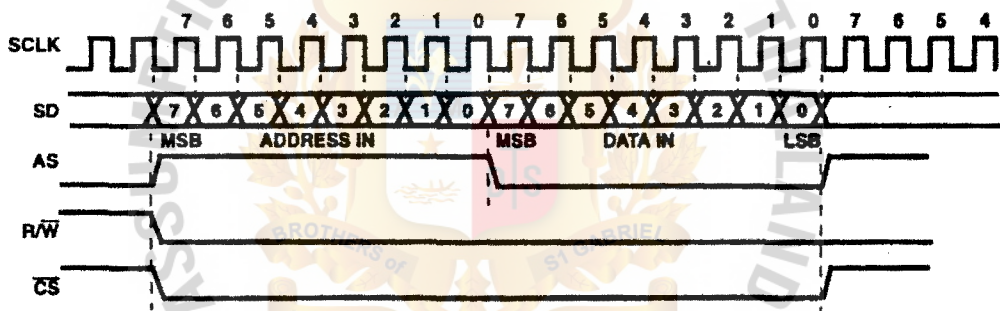
Figure 3.7 Control port write timing

3.4.3.2 TX Port

The transmit data port accepts the data that needs to be transmitted serially from an external data source. The data is modulated and transmitted as soon as it is received from the external data source. The serial data is input to the HFA3824 through TXD using the falling edge of TXCLK to clock it in the HFA3824. TXCLK is an output from the HFA3824. A timing scenario of the transmit signal handshakes and sequence is shown on timing diagram figures 3.8. The external processor initiates the transmit

sequence by asserting TX_PE. TX_PE envelopes the transmit data packet on TXD. The HFA3824 responds by generating TXCLK to input the serial data on TXD. TXCLK will run until TX_PE goes back to its inactive state indicating the end of the data packet.
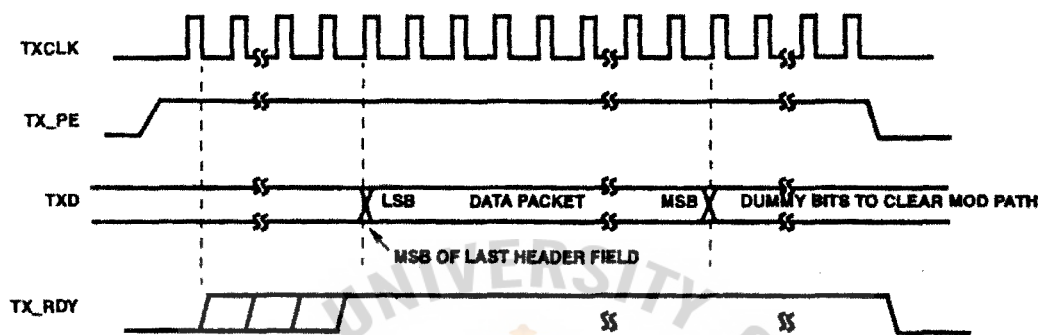

Figure 3.8 TX port timing

When the HFA3824 internally generates the preamble and header information. During this mode the external source needs to provide only the data portion of the packet. The timing diagram of this mode is illustrated on figure 3.8. When the HFA3824 generates the preamble internally, assertion of TX_PE will initialize the generation of the preamble and header. TX_RDY, which is an output from the HFA3824, is used to indicate to the external processor that the preamble has been generated and the device is ready to receive the data packet to be transmitted from the external processor. The TX_RDY timing is programmable in case the external processor needs several clocks of advanced notice before actual data transmission is begins.

The transmit port is completely independent from the operation of the other interface ports including the RX port, therefore supporting a full duplex mode.

3.4.3.3 RX Port

The timing diagram in figure 3.9 illustrates the relationships between the various signals of the RX port. The receive data port serially outputs the demodulated data from RXD. The data is output as soon as it is demodulated by the HFA3824. RX_PE must be at its active state throughout the receive operation. When RX_PE is inactive the device's receive functions, including acquisition, will be in a stand by mode.
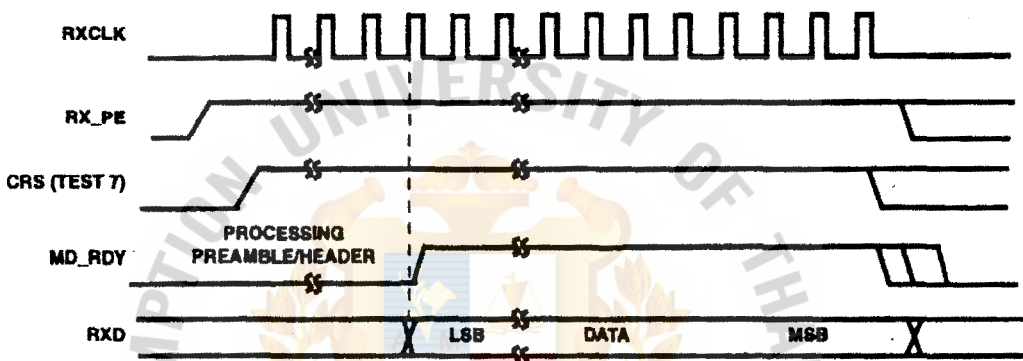
Figure 3.9 RX port timing

RXCLK is an output from the HFA3824 and is the clock for the serial demodulated data on RXD. MD_RDY is an output from the HFA3824 and it envelopes the valid data on RXD. The HFA3824 can be also programmed to ignore error detections during the CCITT-CRC 16 check of the header fields.

Note that RXCLK becomes active after acquisition, well before valid data begins to appear on RXD and MD_RDY is asserted. MD_RDY returns to its inactive state under the following conditions:

- The number of data symbols, as defined by the length field in the protocol, has been received and output through RXD in its entirety (normal condition).

- PN tracking is lost during demodulation.

- RX_PE is deactivated by the external controller.

The receive port is completely independent from the operation of the other interface ports including the TX port, supporting therefore a full duplex mode.

3.4.4 Transmitter Description

The HFA3824 transmitter is designed as a Direct Sequence Spread Spectrum DQPSK modulator. It can handle data rates up to 2 Mbps. The major functional blocks of the transmitter include a network processor interface, DQPSK modulator, a data scrambler and a PN generator, as shown in figure 3.10.
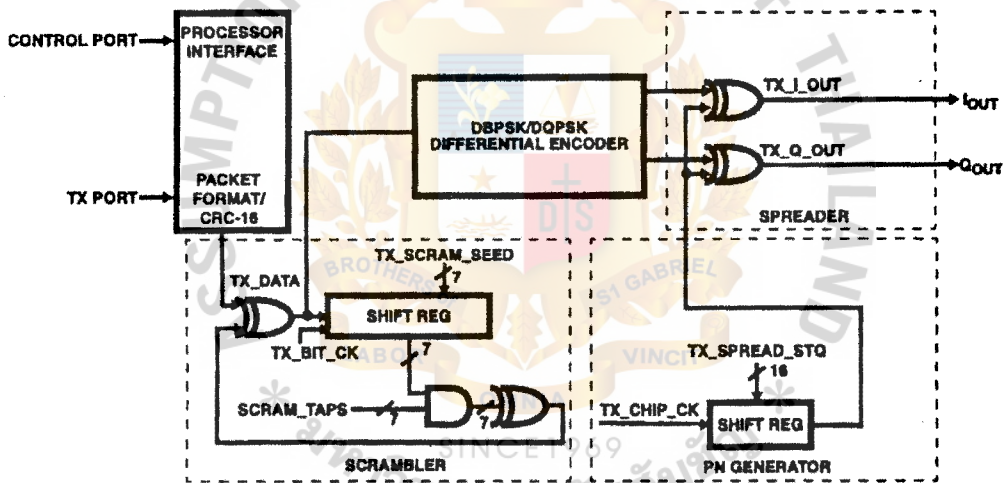

Figure 3.10 Modulator diagram

The transmitter has the capability to generate its own synchronization preamble and header, while data packet can be configured to be DQPSK modulation. The preamble is used by the receiver to achieve initial PN synchronization while the header includes the necessary data fields of the communications protocol to establish the physical layer link.

The transmitter accepts data from the external source, scrambles it, differentially encodes it as DQPSK, and mixes it with the PN spreading. The baseband digital signals are then output to the external IF modulator.

The transmitter includes a PN generator that we use 11 chip sequences. The transmitter also contains a programmable clock divider circuit that allows for various data rates. The master clock (MCLK) can be a maximum of 44 MHz.

The following equations show the symbol rate for both TX and RX as a function of MCLK, Chips per symbol and N.

Symbol Rate = MCLK/(N x Chips per symbol)

For this circuit, we use 24 MHz crystal oscillator to generate MCLK = 24 MHz and use value of N = 2 with Chips per symbol = 11.

Symbol Rate (DQPSK) = 2 x 24 / (2 x 11) = 2.18 Mbps

The modulator is complete independent from the demodulator, allowing the baseband processor to be used in full duplex operation.

3.4.5 Header/Packet Description

The HFA3824 is designed to handle continuous or packetized Direct Sequence Spread Spectrum (DSSS) data transmissions. The HFA3824 can generate its own preamble and header information or it can accept them from an external source.

When preamble and header are internally generated, the device supports a synchronization preamble up to 256 symbols, and a header that can include up to five fields. The preamble size and all of the fields are programmable. When internally generated the preamble is all 1's (before entering the scrambler). The actual transmitted pattern of the preamble will be randomized by the scrambler if the user chooses to utilize the data scrambling option.

The five available fields for the header are:

- *SFD Field (16 Bits)* - This field carries the ID to establish the link. This is a mandatory field for the HFA3824 to establish communications. The HFA3824 will not declare a valid data packet, even if PN acquires, unless it detects the specific SFD. The SFD field is required for both Internal preamble/header generation and External preamble/header generation. The HFA3824 receiver can be programmed to time out searching for the SFD. The timer starts counting the moment that initial PN synchronization has been established from the preamble.

- *Signal Field (8 Bits)* - This field indicates whether the data packet that follows the header is modulated as DBPSK or DQPSK.

- *Service Field (8 Bits)* - This field can be utilized as user requirement.

- *Length Field (16 Bits)* - This field indicates the number of data symbols contained in the data packet. The receiver can be programmed to check the length field in determining when it needs to de-assert the MD_RDY interface signal. MD_RDY envelopes the received data packet as it is being output to the external processor.

- *CCITT-CRC 16 Field (16 Bits)* - This field includes the 16-bit CCITT-CRC 16 calculation of the five header fields. This value is compared with the CCITT-CRC 16 code calculated at the receiver. The HFA3824 receiver can be programmed to drop the link upon a CCITT-CRC 16 error or it can be programmed to ignore the error and to continue with data demodulation.

The CRC or Cyclic Redundancy Check is a CCITT CRC-16 FCS (Frame Check Sequence). In packetize RF data transmissions systems, transmitted messages are susceptible to various types of bit errors due to noise, interference, data collisions. CRCs are very useful in detecting single bit errors, multiple bit errors, and burst errors in packetized messages. In theory CRCs could be thought of as simply taking a binary

message and dividing it by a fixed binary number, with the remainder being the checksum, or more commonly the CRC. The polynomial for the CRC calculation is a 16-bit function and is given as $G_x = X^{16} + X^{12} + X^5 + 1$. The mathematics performed on in calculating the CRC is binary modulo 2 arithmetic, and typically implemented with an XOR function.

3.4.6 Receiver Description

The receiver portion of the baseband processor performs ADC conversion and demodulation of the spread spectrum signal. It correlates the PN spread symbols, then demodulates the DQPSK symbols. The demodulator includes a frequency loop that tracks and removes the carrier frequency off-set. In addition it tracks the symbol timing, differentially decodes and descrambles the data. The data is output through the RX port to the external processor.

A common practice for burst mode communications systems is to differentially modulate the signal, so that a DPSK demodulator can be used for data recovery. This form of demodulator uses each symbol as a phase reference for the next one. It offers rapid acquisition and tolerance to rapid phase fluctuations at the expense of lower bit error rate (BER) performance.

The baseband processor, HFA3824, uses differential demodulation for the initial acquisition portion of the processing and then switches to coherent demodulation for the rest of the acquisition and data demodulation. The HFA3824 is designed to achieve rapid settling of the carrier tracking loop during acquisition. Coherent processing substantially improves the BER performance margin. Rapid phase fluctuations are handled with a relatively wide loop bandwidth.
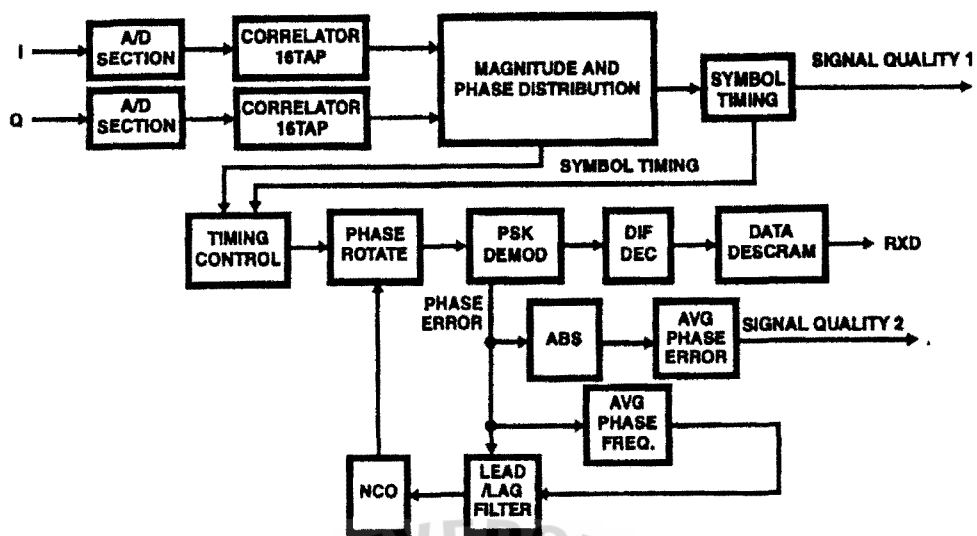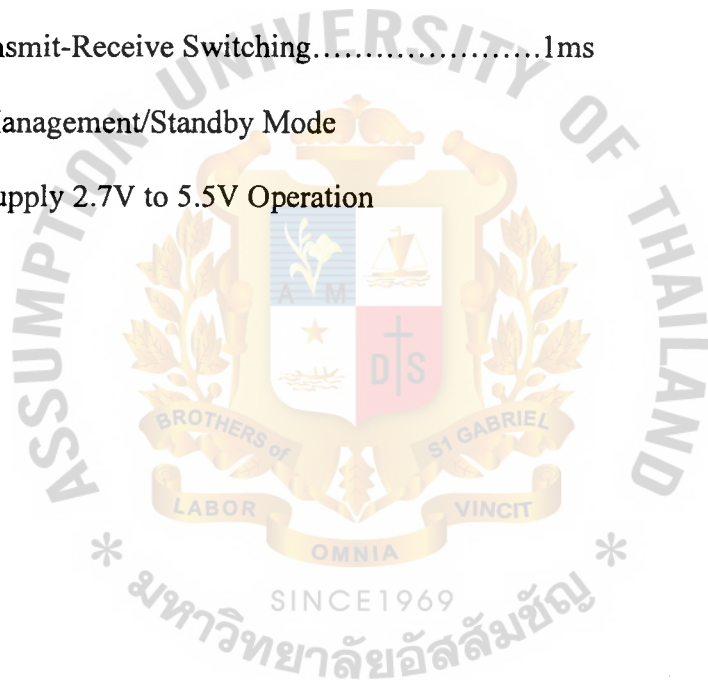
Figure 3.11 Demodulator diagram

The baseband processor uses time invariant correlation to strip the PN spreading and polar processing to demodulate the resulting signals. These operations are illustrated in figure 3.11 which is an overall block diagram of the receiver processor. Input samples from the I and Q ADC converters are correlated to remove the spreading sequence. The magnitude of the correlation pulse is used to determine the symbol timing. The sample stream is decimated to the symbol rate and the phase is corrected for frequency offset prior to PSK demodulation. Phase errors from the demodulator are fed to the NCO through a lead/lag filter to achieve phase lock. The variance of the phase errors is used to determine signal quality for acquisition and lock detection.

3.5 HFA3724 400MHz Quadrature IF Modulator/Demodulator

3.5.1 Features

- Integrates all IF Transmit and Receive Functions

- Broad Frequency Range ……………………………10MHz to 400MHz

- I/Q Amplitude and Phase Balance …………………0.2dB, 2°

- 400 MHz Limiting IF Gain Strip with RSSI ………84dB

- Low LO Drive Level ………………………………-15dBm

- Fast Transmit-Receive Switching…………………1ms

- Power Management/Standby Mode
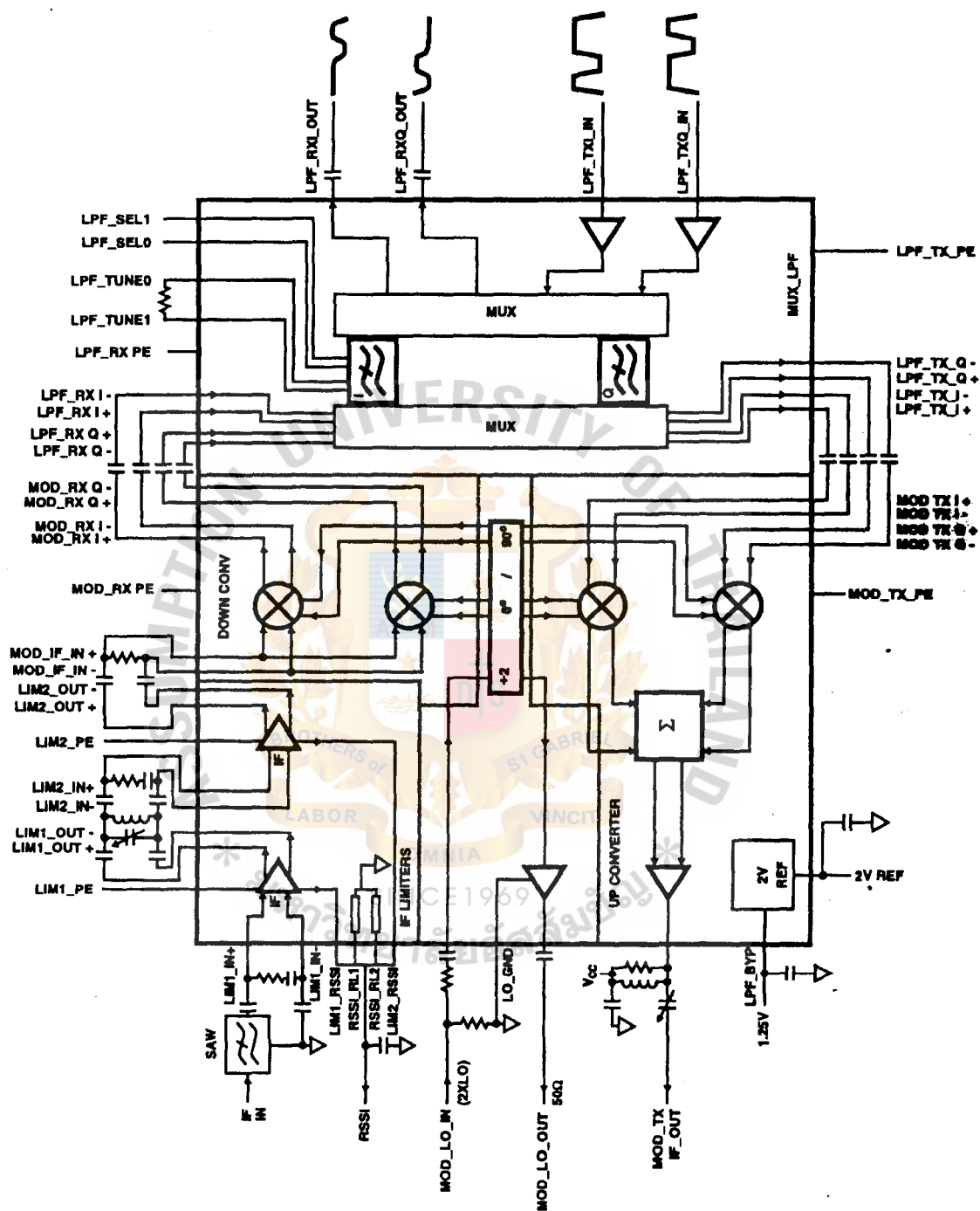
- Single Supply 2.7V to 5.5V Operation

Block Diagram

Figure 3.12 Block diagram of HFA3724

Pin Description

PIN	SYMBOL	DESCRIPTION
1	LIM1_BYP+	DC feedback pin for Limiter amplifier 1. Requires good decoupling and minimum wire length to a solid signal ground.
2	LIM1_In+	Non inverting analog input of Limiter amplifier 1.
3	LIM1_In-	Inverting input of Limiter amplifier 1.
4	LIM1_BYP-	DC feedback pin for Limiter amplifier 1. Requires good decoupling and minimum wire length to a solid signal ground.
5, 6, 7, 8	GND	Ground. Connect to a solid ground plane.
9	LPF_V_{CC}	Supply pin for the Low pass filter. Use high quality decoupling capacitors right at the pin.
10	2V REF	Stable 2V reference voltage output for external applications. Loading must be higher than 10kΩ. A bypass capacitor of at least 0.1µF is required.
11	LPF_BYP	Internal reference bypass pin. This is the common voltage (V_{CM}) used for the LPF digital thresholds. Requires 0.1µF decoupling capacitor.
12	LPF_TXI_In	Low pass filter in phase (I) channel transmit input. Conventional or attenuated direct coupling is required for digital inputs. (Note 7)
13	LPF_TXQ_In	Low pass filter quadrature (Q) channel transmit input. Conventional or attenuated direct coupling is required for digital inputs. (Note 7)
14	LPF_RXI_Out	Low pass filter in phase (I) channel receive output. Requires AC coupling. (Note 8)
15	LPF_RXQ_Out	Low pass filter quadrature (Q) channel receive output. Requires AC coupling. (Note 8)
16	LPF_Sel1	Digital control input pins. Selects four programed cut off frequencies for both receive and transmit channels. Tuning speed from one cutoff to another is less than 1µs. SEL1 SEL0 Cutoff Frequency SEL1 SEL0 Cutoff Frequency LO LO 2.2MHz HI LO 8.8MHz LO HI 4.4MHz HI HI 17.6MHz
17	LPF_Sel0	
18	LPF_Tune1	These two pins are used to fine tune the Low pass filter cutoff frequency. A resistor connected between the two pins (R_{TUNE}) will fine tune both transmit and receive filters. Refer to the tuning equation in the LPF AC specifications.
19	LPF_Tune0	
20	GND	Ground. Connect to a solid ground plane.
21	LPF_RX_PE	Digital input control pin to enable the LPF receive mode of operation. Enable logic level is High.
22	LPF_TX_PE	Digital input control pin to enable the LPF transmit mode of operation. Enable logic level is High.
23	LPF_TXQ-	Negative output of the transmit Low pass filter, quadrature channel. AC coupling is required. Normally connects to the inverting input of the quadrature Modulator (Mod_TXQ-), pin 40.
24	LPF_TXQ+	Positive output of the transmit Low pass filter, quadrature channel. AC coupling is required. Normally connects to the non inverting input of the quadrature Modulator (Mod_TXQ+), pin 39.
25	LPF_TXI-	Negative output of the transmit Low pass filter, in phase channel. AC coupling is required. Normally connects to the inverting input of the in phase Modulator (Mod_TXI-), pin 38.
26	LPF_TXI+	Positive output of the transmit Low pass filter, in phase channel. AC coupling is required. Normally connects to the non inverting input of the in phase Modulator (Mod_TXI+), pin 37.
27	LPF_RXQ-	Low pass filter inverting input of the receive quadrature channel. AC coupling is required. This input is normally coupled to the negative output of the quadrature demodulator (Mod_RXQ-), pin 36.
28	LPF_RXQ+	Low pass filter non inverting input of the receive quadrature channel. AC coupling is required. This input is normally coupled to the positive output of the quadrature demodulator (Mod_RXQ+), pin 35.
29	LPF_RXI-	Low pass filter inverting input of the receive in phase channel. AC coupling is required. This input is normally coupled to the negative output of the in phase demodulator (Mod_RXI-), pin 34.

Table 3.2 Pin description of HFA3724

PIN	SYMBOL	DESCRIPTION
30	LPF_RXI+	Low pass filter non inverting input of the receive in phase channel. AC coupling is required. This input is normally coupled to the positive output of the in phase demodulator (Mod_RXI-), pin 33.
31, 32	GND	Ground. Connect to a solid ground plane.
33	Mod_RXI+	In phase demodulator positive output. AC coupling is required. Normally connects to the non inverting input of the Low pass filter (LPF_RXI+), pin 30.
34	Mod_RXI-	In phase demodulator negative output. AC coupling is required. Normally connects to the inverting input of the Low pass filter (LPF_RXI-), pin 29.
35	Mod_RXQ+	Quadrature demodulator positive output. AC coupling is required. Normally connects to the non inverting input of the Low pass filter (LPF_RXQ+), pin 28.
36	Mod_RXQ-	Quadrature demodulator negative output. AC coupling is required. Normally connects to the inverting input of the Low pass filter (LPF_RXQ+), pin 27.
37	Mod_TXI+	In phase modulator non inverting input. AC coupling is required. This input is normally coupled to the Low pass filter positive output (LPF_TXI+), pin 26.
38	Mod_TXI-	In phase modulator inverting input. AC coupling is required. This input is normally coupled to the Low pass filter negative output (LPF_TXI-), pin 25.
39	Mod_TXQ+	Quadrature modulator non inverting input. AC coupling is required. This input is normally coupled to the Low pass filter positive output (LPF_TXQ+), pin 24.
40	Mod_TXQ-	Quadrature modulator inverting input. AC coupling is required. This input is normally coupled to the Low pass filter negative output (LPF_TXQ-), pin 23.
41	Mod_TX_PE	Digital input control to enable the Modulator section. Enable logic level is High for transmit.
42	Mod_TX_IF_Out	Modulator open collector output, single ended. Termination resistor to V_{CC} with a typical value of 316Ω.
43	Mod_RX_PE	Digital input control to enable the demodulator section. Enable logic level is High for receive.
44	Mod_LO_In (2XLO)	Single ended local oscillator current input. Frequency of input signal must be twice the required modulator carrier and demodulator LO frequency. Input current is optimum at 200µA$_{RMS}$. Input matching networks and filters can be designed for a wide range of power and impedances at this port. Typical input impedance is 130Ω. This pin requires AC coupling. (Note 9) NOTE: High second harmonic content input waveforms may degrade I/Q phase accuracy.
45	Mod_V$_{CC}$	Modulator/Demodulator supply pin. Use high quality decoupling capacitors right at the pin.
46	Mod_LO_Out	Divide by 2 buffered output reference from "Mod_LO_In" input. Used for external applications where the modulating and demodulating carrier reference frequency is required. 50Ω single end driving capability. This output can be disabled by use of pin 50. AC coupling is required, otherwise tie to pin 47 (V$_{CC}$).
47	Mod_V$_{CC}$	Modulator/Demodulator supply pin. Use high quality decoupling capacitors right at the pin.
48	Mod_IF_In+	Demodulator non inverting input. Requires AC coupling.
49	Mod_IF In-	Demodulator inverting input. Requires AC coupling.
50	LO_GND	When grounded, this pin enables the LO buffer (Mod_LO_Out). When open (NC) it disables the LO buffer.
51, 52, 53	GND	Ground. Connect to a solid ground plane.
54	LIM2_PE	Digital input control to enable the limiter amplifier 2. Enable logic level is High.
55	LIM2_V$_{CC}$	Limiter amplifier 2 supply pin. Use high quality decoupling capacitors right at the pin.
56	LIM2_Out-	Positive output of limiter amplifier 2. Requires AC coupling.
57	LIM2_Out+	Negative output of limiter amplifier 2. Requires AC coupling.
58	GND	Ground. Connect to a solid ground plane.

Table 3.2(Cont.) Pin description of HFA3724

Pin Description (Continued)

PIN	SYMBOL	DESCRIPTION
59	RSSI_RL2	Load resistor to ground. Nominal value is 6kΩ. This load is used to terminate the LIM RSSI current output and maintain temperature and process variation to a minimum.
60	LIM2_RSSI	Current output of RSSI for the limiter amplifier 2. Connect in parallel with the RSSI output of the amplifier limiter 1 for cascaded response.
61	LIM2_BYP+	DC feedback pin for Limiter amplifier 2. Requires good decoupling and minimum wire length to a solid signal ground.
62	LIM2_In+	Non inverting analog input of Limiter amplifier 2.
63	LIM2_In-	Inverting input of Limiter amplifier 2.
64	LIM2_BYP-	DC feedback pin for Limiter amplifier 2. Requires good decoupling and minimum wire length to a solid signal ground.
65, 66, 67, 68, 69, 70, 71, 72, 73	GND	Ground. Connect to a solid ground plane.
74	LIM1_PE	Digital input control to enable the limiter amplifier 1. Enable logic level is High.
75	LIM1_V_{CC}	Limiter amplifier 1 supply pin. Use high quality decoupling capacitors right at the pin.
76	LIM1_Out-	Negative output of limiter amplifier 1. Requires AC coupling.
77	LIM1_Out+	Positive output of limiter amplifier 1. Requires AC coupling.
78	GND	Ground. Connect to a solid ground plane.
79	RSSI_RL1	Load resistor to ground. Nominal value is 6kΩ. This load is used to terminate the LIM RSSI current output and maintain temperature and process variation to a minimum.
80	LIM1_RSSI	Current output of RSSI for the limiter amplifier 1. Connect in parallel with the RSSI output of the amplifier limiter 2 for cascaded response.

Table 3.2(Cont.) Pin description of HFA3724

3.5.2 Description

HFA3724 400MHz Quadrature IF Modulator/Demodulator is a highly integrated baseband converter for quadrature modulation applications. It features all the necessary blocks for baseband modulation and demodulation of I and Q signals. It has a two stage integrated limiting IF amplifier with 84db of gain with a built in Receive Signal Strength Indicator (RSSI). Baseband antialiasing and shaping filters are integrated in the design. Four filter bandwidths are programmable via a two bit digital control interface. In addition, these filters are continuously tunable over a ±20% frequency range via one external resistor. The modulator channel receives digital I and Q data for processing. To

achieve broadband operation, the Local Oscillator frequency input is required to be twice the desired frequency of modulation/demodulation.

3.5.3 Overall Device Description

The HFA3724 is a highly integrated baseband converter for half duplex wireless data applications. It features all the necessary blocks for baseband modulation and demodulation of "I" and "Q" quadrature multiplexing signals. It targets applications using all phase shift types of modulation (PSK) due to its hard limiting receiving front end. Four fully independent blocks adds flexibility for numerous applications covering a wide range of IF frequencies. A differential design architecture, device pin out and layout have been chosen to improve system RF properties like common mode signal immunity (noise, crosstalk), reduce relevant parasitics and settling times, and optimize dynamic range for low power requirements. Single power supply requirement from 2.7V DC to 5.5V DC makes the HFA3724 a good choice for portable transceiver designs.

The HFA3724 has a two stage integrated limiting IF amplifier with frequency response to 400MHz. These amplifiers exhibit a -84dbm, -3db cascaded limiting sensitivity with a built in Receive Signal Strength Indicator (RSSI) covering 60db of dynamic range with excellent linearity. An up conversion and down conversion pair of quadrature doubly balanced mixers are available for "I" and "Q" baseband IF processing. These converters are driven by an internal quadrature LO generator which exhibits a broadband response with excellent quadrature properties. To achieve broadband operation, the Local Oscillator frequency input is required to be twice the desired frequency for modulation/demodulation. Duty cycle and signal purity requirements for the 2X LO input using this type of quadrature architecture are less

restrictive for the HFA3724. Ground reference input signals as low as -15dBm and frequencies up to 900MHz (2XLO) can be used and tailored by the user. A buffered, divide by 2, LO single ended 50W selectable output is provided for convenience of PLL designs. The receive channel mixers "I" and "Q" quadrature outputs have a frequency response up to 30MHz for baseband signals and the transmit mixers are summed and amplified to a single ended open collector output with frequency response up to 400MHz.

Multiplexed or half duplex baseband 5th order Butterworth low pass filters are also included in the design. The "I" and "Q" filters address applications requiring low pass and antialiasing filtering for external baseband threshold comparison or simple analog to digital conversion in the receive channel. During transmission, the filter is used for pulse shaping or control of spectral mask.

Four filter bandwidths are programmable, (2.2MHz, 4.4MHz, 8.8MHz and 17.6MHz) via a two bit digital or hardwired control interface. These cut off frequencies are selected for optimization of spectrum output responses for 2.25M, 5.5M, 11M and 22M chips/sec respectively for spread spectrum applications (These rates can also be interpreted as symbol rates for conventional data transmission). External processing correlators in the receive channel as in the Harris HSP3824 baseband converter will bring the demodulation to lower effective data rates. As an example, the use of 11M chips/sec, 11 chip Barker code using the 8.8MHz low pass filter in a QPSK type of modulation scheme will bring a post processed effective data rate to 1M symbol/sec or 2M bits/sec. In addition, these filters are continuously tunable over a ±20% frequency range via one external resistor. This feature gives the user to reshape the spectrum of a transmitted signal at the antenna port which takes into account any spectral regrowth along the transmitter chain. The modulator "I" and "Q" filter inputs accept digital signal

levels data for modulation and their phase and gain characteristics, including I/Q matching and group delay are well suitable for reliable data transmission. In the receive mode and over the full input limiting dynamic range, both low pass filters outputs swing a 500mV P-P baseband signal.

Each block has its own independent power enable control for power management and half duplex transmit/receive operation. A stable 2V DC output and a buffered band gap reference voltage are also provided for an external analog to digital conversion reference.

CHAPTER 4. SIMULATION AND MEASUREMENT

4.1 Simulation

The purpose of simulation is to verify our circuit diagram and to predict the performance of the system. Simulation model based on Matlab programming and Ansoft software by using DQPSK modulation technique and direct sequence spread spectrum to spread the signal spectrum.

4.1.1 Matlab simulation

In matlab simulation, we use matlab program to plot the power spectral density of output spread spectrum signal with carrier frequency of 80 MHz by using equation Fourier transform of the auto-correlation function as we describe in our theory. That is

$$S_s(f) = \frac{t_1}{2}\left\{ \left[\frac{\sin \pi(f - f_0)t_1}{\pi(f - f_0)t_1} \right]^2 + \left[\frac{\sin \pi(f + f_0)t_1}{\pi(f + f_0)t_1} \right]^2 \right\}$$

by using $t_1 = 2t_m/11 = 2 \times 0.909 \times 10^{-7}$ and $f_0 = 80\text{MHz}$

Figure 4.1 is the power spectral density of output spread spectrum signal and figure 4.2 is power spectral density of spread spectrum signal in dBm. You can see in figure 4.2 that main lobe of output spread spectrum signal is around 11 MHz bandwidth start from 74.5 MHz to 85.5 MHz and side lobe is around 5.5 MHz bandwidth. Output power spectral density of output spread spectrum signal is around −27 dBm at center frequency 80 MHz.
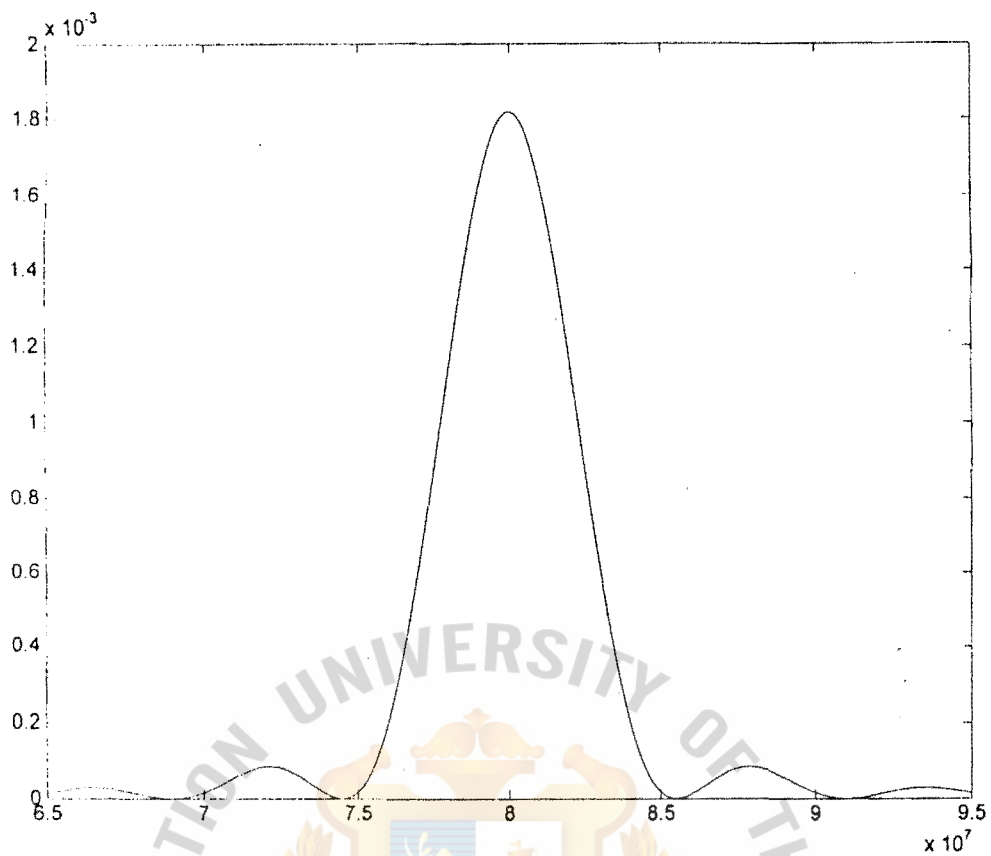
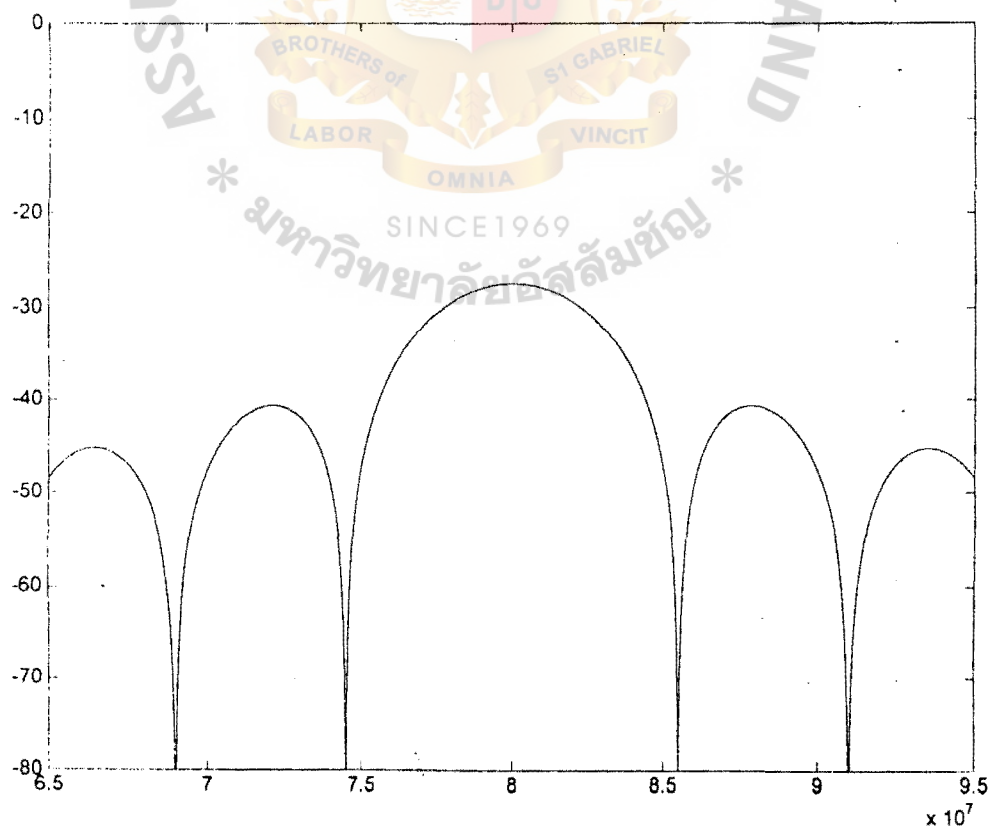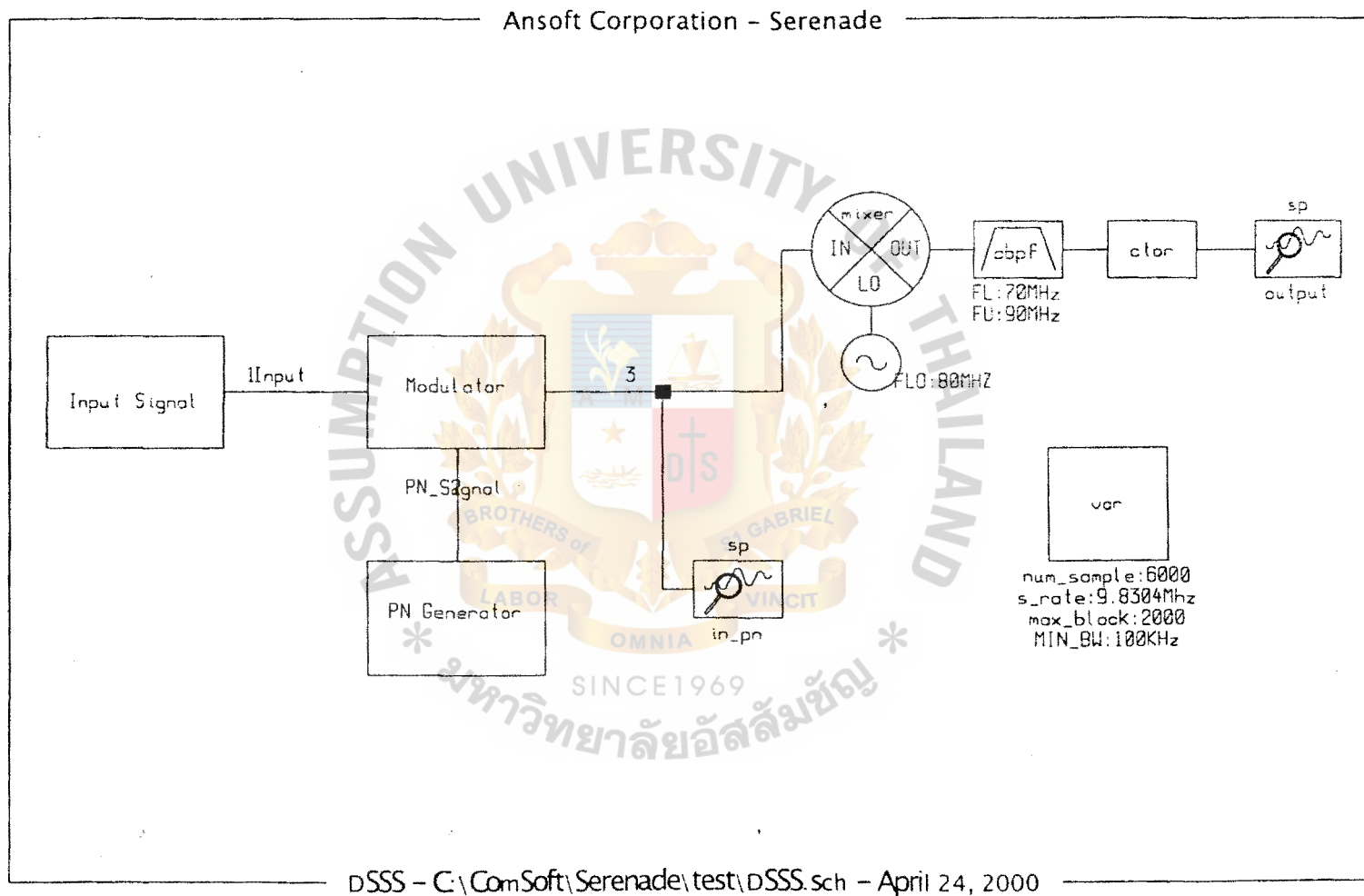Figure 4.1 Power spectral density of output spread spectrum signal

Figure 4.2 Power spectral density of output spread spectrum signal in dBm

4.1.2 Ansoft simulation

In Ansoft simulation, we use block diagram in Ansoft program to simulate the output spread spectrum signal by using 80 MHz carrier frequency. We use digital pulse signal as an input signal with sample rate about 10 MHz. A simulation model is shown in figure 4.3. Figure 4.4 is an input signal. The output of spread spectrum signal at the central frequency of 80 MHz shown in figure 4.5.

Figure 4.3 A simulation circuit

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DSSS   Y1
SP(DSSS.DSSS_IN.IN) Mag
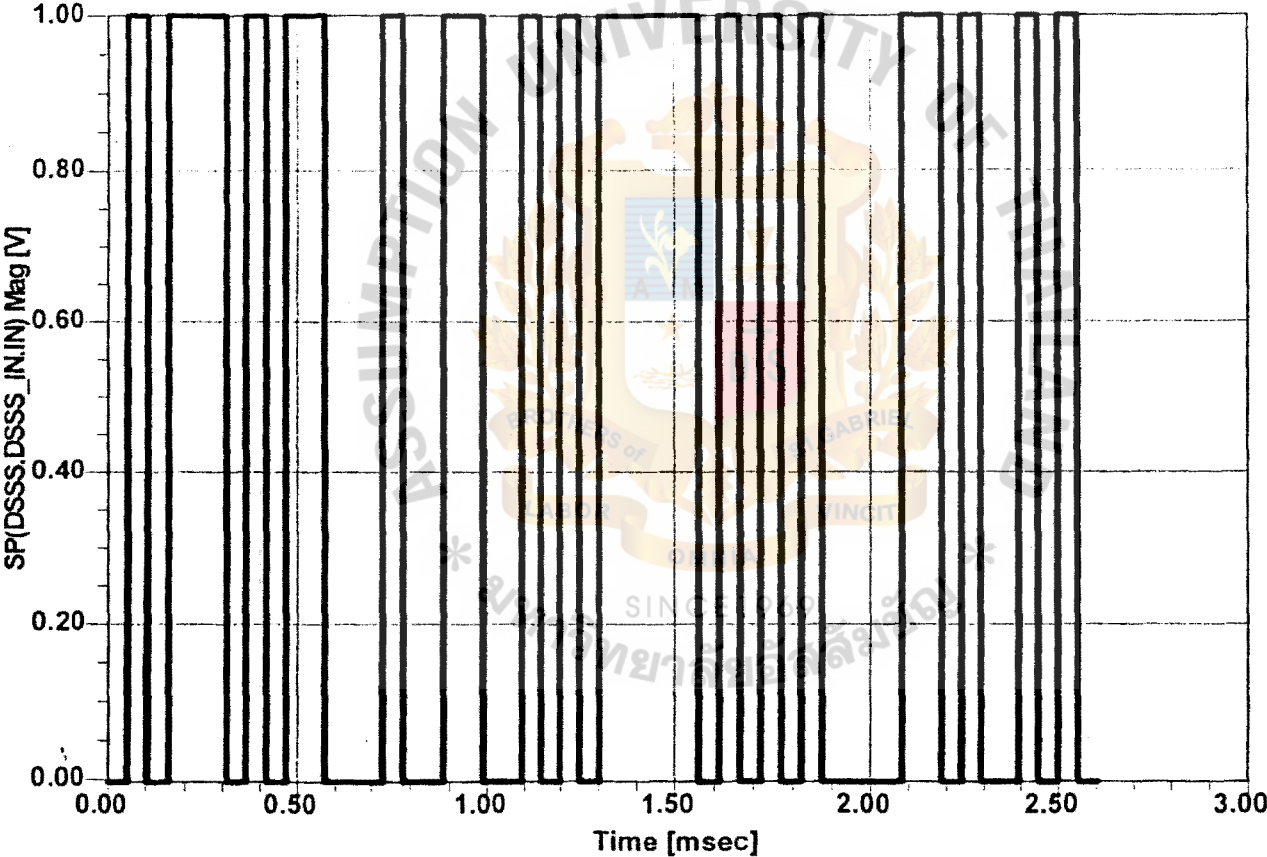
C:\ComSoft\Serenade\test\DSSS.sph
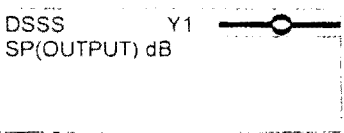## System: DSSS

Figure 4.4 Input signal

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Ansoft Corporation - Symphony ® v8.0

DSSS   Y1
SP(OUTPUT) dB
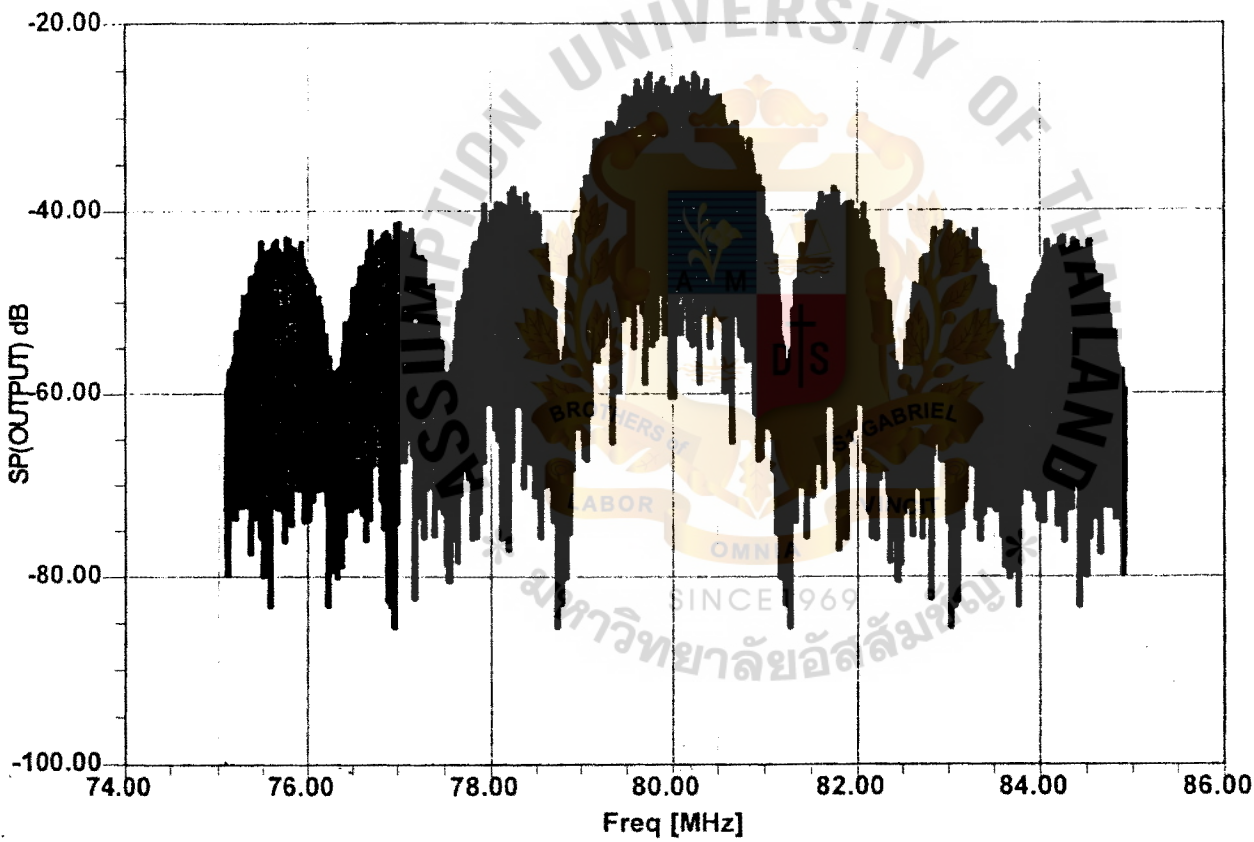
C:\ComSoft\Serenade\test\DSSS.sph
System: DSSS

Figure 4.5 Output signal spectrum at 80 MHz

4.2 Measurement

We measure the power spectral density by giving power to wireless LAN card 5Vcc and using spectrum analyzer to input carrier frequency to wireless LAN card. We active pin TXPE by connect to Vcc and inactive RXPE by connect to ground for testing transmit signal mode. At the output port, we connect to Spectrum Analyzer to observe the output signal.

We input data to card via TXD pin of HFA3824 Baseband Processor. Inside Baseband Processor chip HFA3824, adds preamble/header and uses CRC-16 cyclic redundancy check with data packet, then the data is scrambled and uses technique of DQPSK modulation to modulate signal into I and Q components. We use 11 bit Barker code sequence to spread the signal then output to the HFA3724 as CMOS logic signals. The HFA3724 receives I and Q signal, then mix with 80 MHz LO to shift the frequency to 80 MHz and outputs to the scope that we can see from figure 39 and 40.

Figure 4.6 is the figure of spectrum signal start frequency from 20 MHz to 1 GHz. We can see that it has a peak spectrum signal at 80 MHZ, 240 MHz, 400 MHz, 560 MHz, and so on. We can observe from the spectrum signals that these signals are odd harmonic of the spread spectrum signal at 80 MHz and these harmonics come from 160 MHz oscillator. Figure 4.7 is the figure of spread spectrum signal at central frequency of 80 MHz. We can see that the bandwidth of main lobe is around 11 MHz and side lobe is around 5.5 MHz bandwidth sane as in our Matlab simulation result and power is around –30 dBm. After that we add one amplifier at the output to increase the output power. We can see from figure 4.8 that after we add amplifier at the output stage, the output power is increased to -15 dBm.
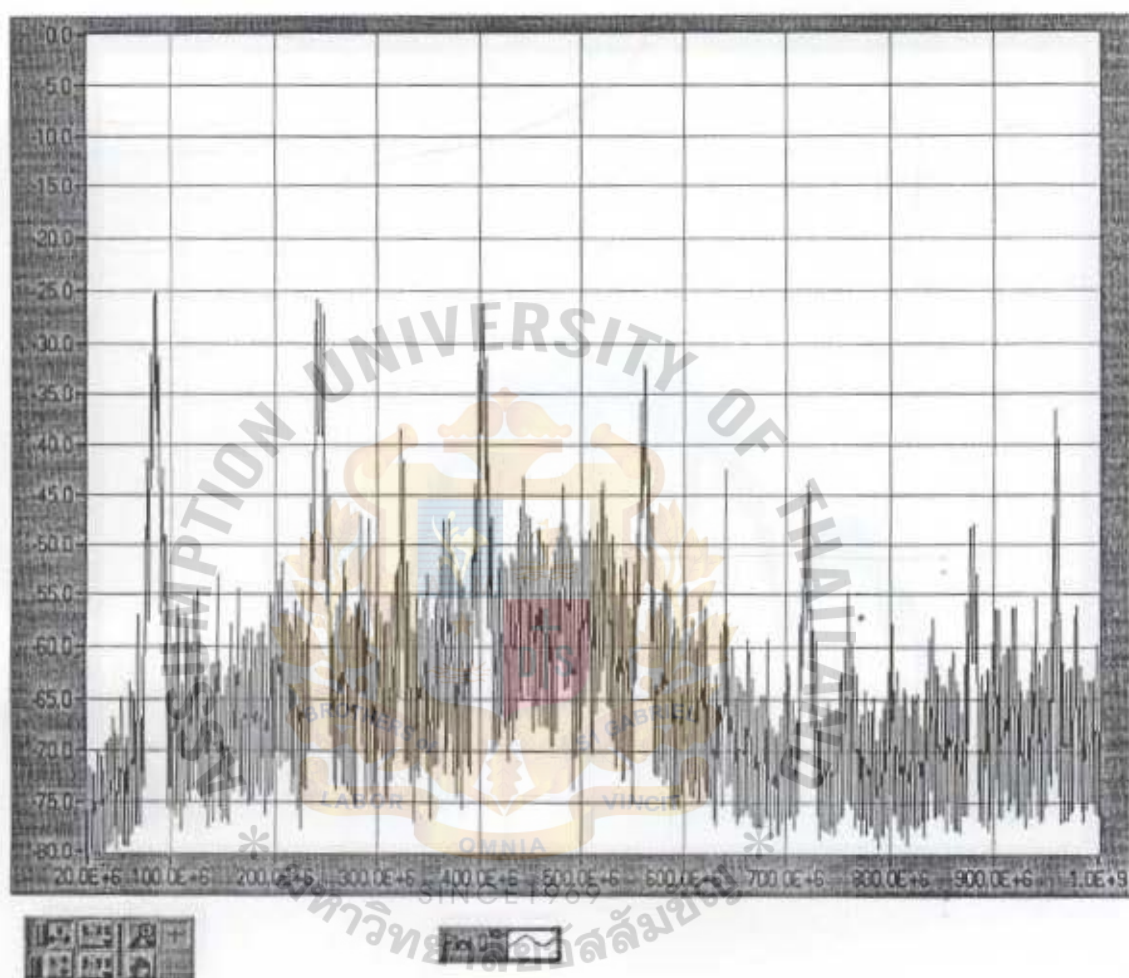
Start Freq. Hz 20.00E+6   Center Freq. Hz 510.00E+6   Span. Hz 980.00E+6   Stop Freq. Hz 1.00E+9

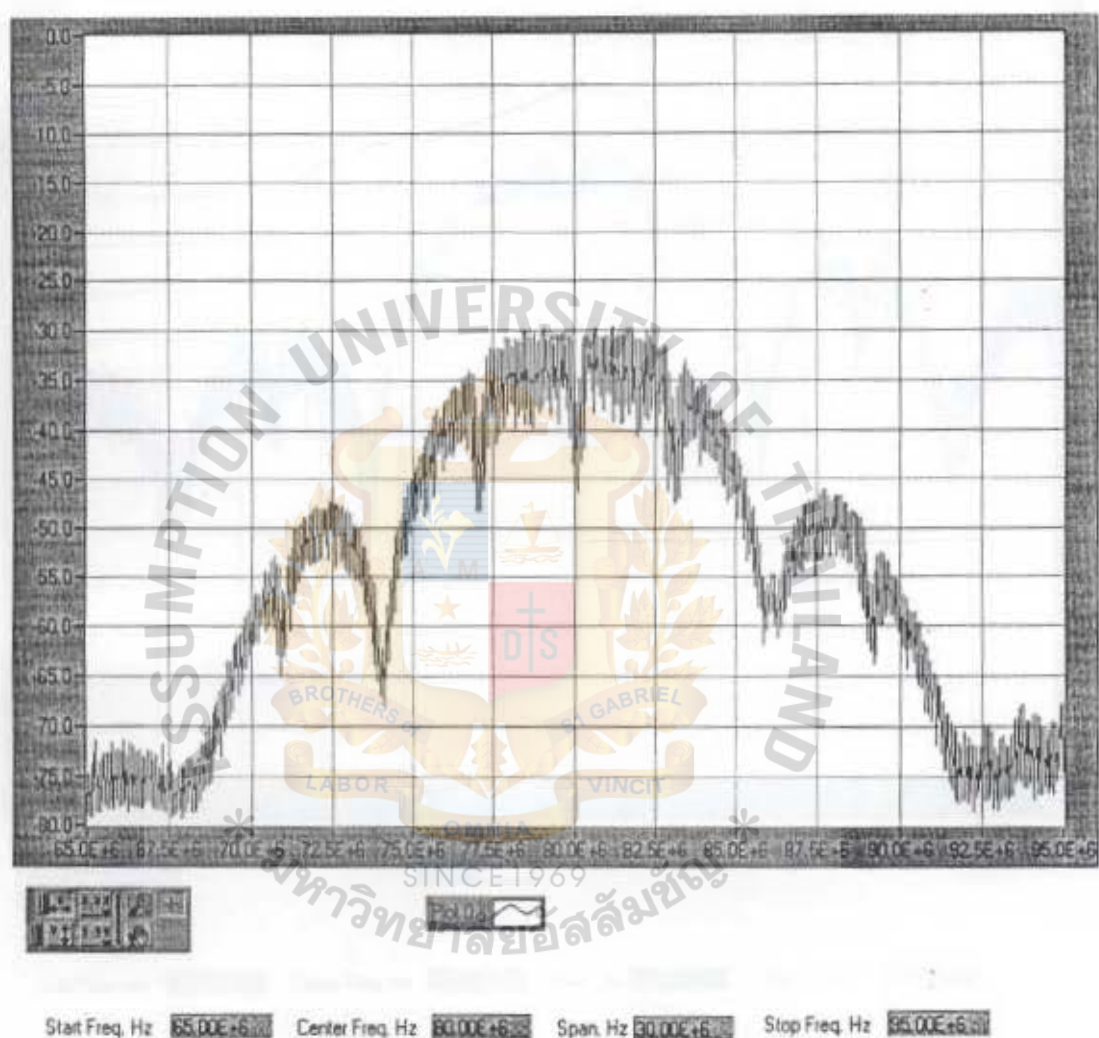Figure 4.6 Output spread spectrum signal with 1 GHz BW

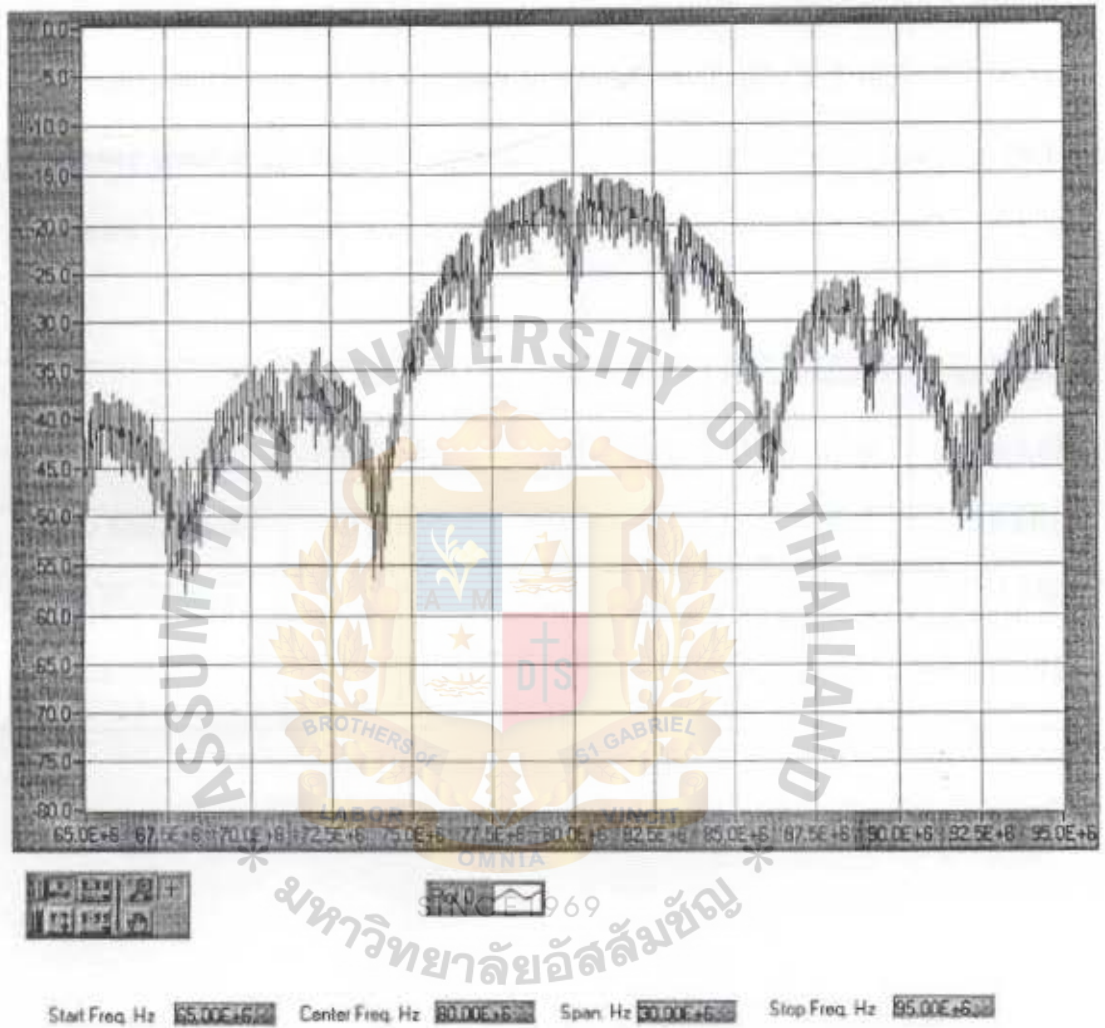Figure 4.7 Output Spread spectrum signal with 30 MHz BW

Figure 4.8 Output spread spectrum signal after amplify

4.3 Comparisons

In this part, we will compare the output signal spectrum of Matlab simulation, Ansoft simulation and measurement result. For both simulation and our measurement result we can get the output spread spectrum signal at the center frequency of 80 MHz. But in our Ansoft simulation we use 10 MHz clock for input signal, so we get the bandwidth of output spread spectrum signal less than in Matlab simulation and measurement result. The power spectral density and bandwidth of output spread spectral signal can be listed as follows.

	Center Frequency	Output Power Spectral Density	Bandwidth of Main Lobe	Bandwidth of Side Lobe
Matlab Simulation	80 MHz	-27 dBm	11 MHz	5.5 MHz
Ansoft Simulation	80 MHz	-27 dBm	2.5 MHz	1.25 MHz
Measurement Result	80 MHz	-30 dBm	11 MHz	5.5 MHz

Table 4.1 Comparison of Simulation and Measurement

Chapter 5. Conclusion

A physical layer design for a broadband part direct sequence spread spectrum wireless LAN is presented. This physical layer directly interfaces with the MAC layer. We receive data from MAC layer and transmit signal at the frequency of 80 MHz. In design, we use DSSS and DQPSK modulation technique.

In first section of this report, we introduce wireless systems. Several information of wireless network are discussed. We describe the concepts of the spread spectrum technology and modulation technology. The operations of two widely used spread spectrum systems, direct sequence spread spectrum and frequency hopping systems, and technique of QPSK modulation are briefly addressed.

For the hardware design, a transmitter has been designed and built to perform DQPSK modulation, direct sequence spread spectrum and moves the baseband spread spectrum to IF frequency at 80 MHz. In first period, that is collect data and component. We face to the problem of collecting component and chip. Almost all of component in this card, we use for surface mount component that is very hard to find in Thailand. In period of design circuit and set up PCB, we have some problems with PCB design. We use small cable to setup through hole for PCB. But these small cables and connections create some noise to the card. Another problem comes from transmission line that is not exactly 50 Ω. As we know that most of the components that used in high frequency needed to use 50 Ω transmission lines to have a good design. So these are the problems in this design and it makes we lost some power.

For testing period, we test by connecting output from our wireless LAN card to spectrum analyzer, and we can observe that we get the output spread spectrum signal at the IF frequency of 80 MHz as in our objective. The output spread spectrum signal has

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approximate 23 MHz bandwidth and power spectral density around -30 dBm. In matlab simulation, we can see that output power spectral density of spread spectrum signal and bandwidth of spread spectrum signal is nearly the same as in our measurement result but it has power spectral density a little bit higher than we measure from our circuit. This result maybe come from the design of circuit not so good, quality of PCB and noise. Although our output power of spreading signal is detected but it still quite low power and has some noise signals around some frequency that maybe from pager, mobile phone or others wireless system. So we try to increase output spread spectrum signal by using amplifier. Then we can get output power of spread spectrum signal increase to −15 dBm. We include some parts of hardware design, list of components and matlab program in appendix part.

In future, wireless network will become more popular and wireless LAN will become more usage with laptop and personal computer because of its mobility. In this thesis we have some idea concerning with wireless LAN design physical layer and in future we can develop wireless LAN card to have more efficiency and reliability.

APPENDIX A

A.1 Components List

The following table shows the components list used in wireless LAN broadband part (80MHz) design.

Table A.1 The Components List

Name	Type	Value	Company
U1	DSSS Baseband Processor	HFA3824	HARRIS
U2	Quad IF Modulator	HFA3724	HARRIS
U3	5 V Regulator	TH11235	TOKO
U4	Oscillator	24 MHz	.
U11	LNA	MAX2650	MAXIM
12, C73	Capacitor	4.7 u	MURATA
C1, C2, C3, C4, C5, C7, C8, C10, C29, C32, C35, C36, C37, C40, C42, C46, C55, C58, C66, C74, C80, C119, C125, C127, C130, C132	Capacitor	0.1u	MURATA
C147	Capacitor	0.01u	MURATA
C30, C31	Capacitor	1000p	MURATA
C6, C9, C11, C12, C13, C14, C15, C22, C43, C44, C47, C48, C49, C54, C61, C65, C72	Capacitor	100p	MURATA
C18, C28, C50	Capacitor	47p	MURATA
C62	Capacitor	20p	MURATA
L1	Inductor	10u	COIL CRAFT
L2, L4	Inductor	33n	TOKO
L3	Inductor	10n	COIL CRAFT
R1	Resistor	9.1k	ROHM
R22	Resistor	8.2k	ROHM
R63, R64	Resistor	4.3k	ROHM
R13	Resistor	3.9k	ROHM
R4	Resistor	1k	ROHM
R34	Resistor	909	ROHM
R58, R65	Resistor	680	ROHM
R9	Resistor	560	ROHM
R5	Resistor	261	ROHM
R2	Resistor	220	ROHM
R23	Resistor	56	ROHM

APPENDIX B

B.1 Matlab program

```
echo on

delta=1000;

F_min=-95000000;

F_max=-65000000;

f=F_min:delta:F_max;

z=65000000:1000:95000000;

Sy=10.*log10((0.1818.*10.^-2).*((sin(((80000000+f).*2).*3.14.*0.909.*10.^-7))./

(((80000000+f).*2).*3.14.*0.909.*10.^-7)).^2);

plot(z,Sy);

axis([65000000 95000000 -80 0]);
```

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