Movement Detector and Autodial

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MOVEMENT DETECTOR AND AUTODIAL

PRESENTED TO:

DR.WIN TIN

PRESENTED BY:

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2.MS. WON-JUNG CHAO ID.3916183

THIS PROJECT IS A PART OF THE REQUIREMENT OF THE COURSE EN 4902 ELECTRONICS ENGINEERING PROJECT II

DEPARTMINT OF ELECTRONICS

ABAC SCHOOL OF ENGINEERING

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ACKNOWLEDGEMENT

This project would never be completed without the help from many other people. We would first like to express our gratitude to our advisor, Dr. Win Tin, for the help and suggestions you never hesitate to provide to this project, as well as the patience and understanding you have with us inexperienced beginner. We would also like to say "thank you" to Dr. Kittiphan Techakittiroj for your advice and encouragement. Very special thanks to Mr. Suvir Kumar, who guides us all the way up to the present point, we really wouldn't be where we are without you.

Nothing is easy at the beginning and one shall not give up easily to the failures which must be there during the process. Mistakes made us learn.

ABSTRACT

It is very common in Thailand to have maids at home looking after the house while masters are away. Thus the security system is not very popular and important to many people. However, I personally experience a case when I have no maid at home for a month. I worried so much that thieves would break into the house while I am not home, and there came the idea of this project while I was expressing my worries to my partner. Therefore we decided to have "Movement Detector and Autodial" as the title and central idea of our senior project. Movement detector, as its name suggests, detects any movement within a limited range. Detected movement would signal or trigger the autodial circuit to call the stored telephone numbers and a recorded warning message is played to the receiver of the call through the telephone line. Microcontroller is used to interface all the hardware parts, such as movement detector, telephone speech network, tone decoder, DTMF generator, EEPROM, voice record/playback device, and keyboard encoder, with the software part, which is the program to be written in Assembly Language, in order to function according to the designed idea Each step wasa not easy, a lot of testings must be taken. However, we finally have achieved most goals and come to this final step.

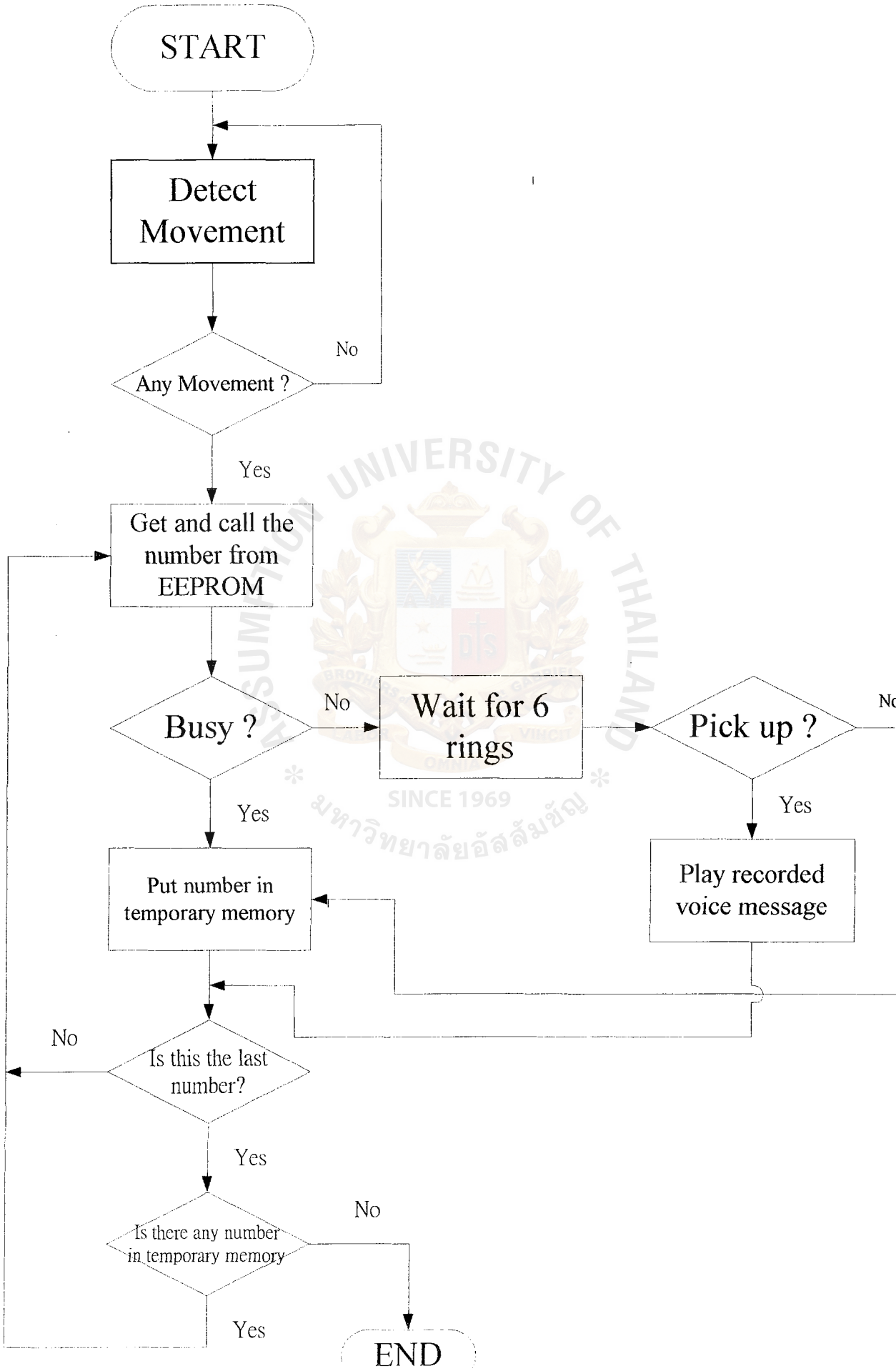
In this report one shall gain the knowledge background and theory for the design of this project. Discussion of the failures and errors we faced are also included. May this report be a worthy piece after all the hardworks and efforts we have put into.

CHAPTER 1 INTRODUCTION

Our objective for this project "Movement detector and Autodial" is to design a security system which will detect movement made by people and autodial the stored number to warn the call receiver about the intrusion with a recorded voice message. There are all together 8 ICs used in this project design as follows:

1. 8 bit Microcontroller with 4k Bytes Flash (AT89C51)
2. PIR Movement Detector (KC778B)
3. Telephone Speech Network with Dialer Interface (MC34114)
4. Tone Decoder (LM567)
5. DTMF (Touch – Tone) Generator (TP5089)
6. 2–wire serial EEPROM (AT24C01A)
7. Single–chip Voice Record / Playback device (ISP 2590)
8. 16–Key Encoder (MM74C922)

A flow chart for the working process of this project is shown in the next page. The detailed theories and ideas of design of each step with relevant IC will be presented in the next chapter. Assembly language is used for programming the AT89C51 microcontroller, which is the main chip for this whole project. Microcontroller brings all the hardware parts and the software programming together to work as we desired by programming it.


START
Detect Movement
Any Movement ?
No
Yes
Get and call the number from EEPROM
Busy ?
No
Wait for 6 rings
Pick up ?
No
Yes
Yes
Put number in temporary memory
Play recorded voice message
Is this the last number?
No
Yes
Is there any number in temporary memory
No
Yes
END

CHAPTER 2 THEORY AND DESIGN

Microcontroller

The microcontroller used in this project is a 8-bit microcontroller with 4K Bytes Flash and numbered as AT89C51, a product by ATMEL. The detailed descriptions and features can be found in the data sheets or at www.atmel.com. One advantage of the on-chip Flash is that it allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. It is actually a microcomputer and is very useful to many embedded control applications, as well as to this project. After correct programming, it shall act like a control center throughout the process of movement detection and autodialing, and one can discover its important role in the later parts of this report under "Movement Detection" and "Autodial". Assembly language, which we are more familiar with, is used to program the AT89C51 microcontroller for this project.

Movement Detection

PIR sensors are the most common movement detector used today for interior use. Ultrasonic is also another type of sensor used for similar purpose. The advantage of PIR over ultrasonic is that it needs no transmitter and receiver. So less space is taken. There are 3 main components to make movement detector in this project:

1) PIR(Passive Infra Red) movement sensor
2) PCB mounted fresnel lens
3) Movement detector IC (KC788B)

The most important chip in this movement detection part is the movement detector IC. Following are the Pin Descriptions and connections.

Vcc (pin1) – This is the regulated supply voltage to the chip (nominally 5V).

Sensitivity Adjust (pin2) – This pin is used to adjust the sensitivity threshold of the motion comparators. When the voltage on this pin equals the pyro drain reference voltage on pin7 the PIR sensitivity will be minimum (± 500 mV). When the voltage on this pin is Gnd the PIR sensitivity will be maximum (±125mV). Intermediate voltages will provide intermediate sensitivities.

Offset Filter (pin3) – This pin connects to an external capacitor of 10 μF and holds the average value of the switched capacitor bandpass filter output. Motion is

detected when the difference between this average and the actual filter output is greater than the sensitivity setting. The output of the switched capacitor bandpass filter can be seen directly on this pin if the external capacitor is disconnected, however, motion will not be detected under these conditions.

Anti–Alias (pin4) – This pin connects to an external capacitor of 0.1μF providing low pass filtering of the PIR input signal, blocking input signals at and above the switching frequency of the switched capacitor bandpass filter.

DC CAP (pin5) – This pin connects to an external capacitor of 10μF and holds the average pyro source voltage. The difference between this average and the actual pyro source voltage is amplified and coupled to the switched capacitor bandpass filter. The 10 μF capacitor must be a low leakage capacitor, such as a Tantalum capacitor.

Vreg (pin6) – This pin output a voltage that can be used to directly drive an external NPN/PNP voltage regulator, or the gate of an external depletion mode JFET voltage regulator pass element. This pin need not be connected if an external regulator, such as a three pins regulator, is used to generate Vcc for the chip.

Pyro (D) (pin7) – The pyro drain reference voltage is output on this pin. This voltage is power supply independent and is connected internally to special noise cancellation circuitry to improve the performance and reliability of the PIR interface. Externally, this pin is connected to the pyro drain and to a 0.1μF capacitor. This voltage can also be divided down by an external pot to supply the Sensitivity Adjust voltage to pin 2.

Pyro (S) (pin8) – This is the pyro source input pin that receives the PIR input signal. It is connected externally to the pyro source, a 200 pF capacitor and a 47 KΩ resistor to Gnd. This is a sensitive node and the length of the external interconnect to, this pin should be made as short as possible. There should be a ground plane on the PC board under the PIR sensor.

Gnd (A)(pin9) – This pin is the electrical ground for the internal analog circuitry of the chip.

Gnd (D)(pin10) – This pin is the electrical ground for the internal digital circuitry of the chip.

Daylight Adjust (pin11) – This pin is the output of the Daylight Sense amplifier and the input to the daylight comparator. When using a silicon photo diode daylight

sensor, this pin is connected to Daylight Sense (pin12) by a resistor or pot. The amount of resistance determines the gain of the Daylight Sense amplifier and hence the sensitivity of the daylight detector. When using a CdS daylight sensor, a pot is connected between this pin and Vcc, while the CdS sensor is connected across one side of the pot (two fixed resistors can be used instead of the pot). Daylight Sense (pin12) must be connected to Vcc when using a CdS sensor. To disable the daylight detector, Daylight Adjust (pin11) must be unconnected and Daylight Sense (pin12) must be connected to Vcc. To disable Auto–ON mode, Daylight Adjust (pin11) and Daylight Sense (pin12) must be connected to Vcc (the Daylight detector is not used when Auto–ON mode is disabled).

Daylight Sense (pin12) – This is the input to the Daylight Sense amplifier. When using a silicon photo diode daylight sensor, this pin is connected to the cathode of the silicon photo diode and to a feedback resistor (or pot) from Daylight Adjust (pin11). In all other cases, this pin is connected to Vcc.

Gain Select (pin13) – The Gain Select pin is a tri–state input used to select the gain of the PIR circuitry. When this pin is connected to Gnd, the PIR gain is set to 62 dB. When this pin is unconnected or connected to Vcc, the PIR gain is set to 68 dB. Normally this pin is unconnected except when less gain is required by a particular PIR sensor.

ON/AUTO/OFF (pin14) – This pin is a tri–state input used to determine the operation of the chip. Normally this pin is unconnected, allowing the chip to operate in its configured operating mode. If this pin is connected to Gnd, the load will turn off unconditionally and will remain off as long as this pin is connected to Gnd. If this pin is connected to Vcc, the load will turn on unconditionally and will remain on as long as this pin is connected to Vcc.

Toggle (pin15) – This pin is a toggle input used to determine the operation of the chip. Normally this pin is unconnected, allowing the chip to operate in its configured operating mode. If this pin is connected to Gnd, the load will change from on to off or from off to on and will remain in the new state unconditionally as long as this pin is connected to Gnd. If the ON/AUTO/OFF (pin14) and Toggle (pin15) switches are pressed such that one is trying to turn the load on unconditionally and the other is trying to turn the load odd unconditionally, the load will be turned off (off overrides on).

OUT (pin16) – The output from this pin is used to turn the external load on or off

through TRIAC, relay or opto–coupler. The impedance of this pin is less than 35Ω, enabling it to directly drive a small (100Ω DC coil resistance) relay, or drive pulse relay through a 150μF series capacitor. For proper operation, the load should come on when this pin goes high, the load should go off when this pin goes low.

LED (pin17) – The output from the motion comparator drives this pin through an internal 500Ω current limiting resistor, enabling it to directly drive an LED motion indicator. Whenever motion is detected this pin will go high and the LED will light. When there is no motion this pin will be low.

C (pin18) – This pin is the input to the OFF timer oscillator. It is connected externally to a pot (or resistor) from R (pin19) and to a capacitor. The OFF timer delay, in seconds, will be 5678*(40,000 + pot resistance in Ohms)*(capacitance in Farads). To disable Auto–OFF mode, this pin can be connected to Gnd or Vcc. For minimum time delay, C (pin18) and R (pin19) can be shorted together with no external resistor or capacitor. In this configuration, the output at OUT (pin16) should be the same as the output at LED (pin17).

R (pin19) – The output of the OFF timer oscillator drives this pin through an internal 40kΩ series resistor. This pin is connected externally to C (pin18) through a pot (or resistor). This pin can be connected directly to C (pin18) for the minimum OFF timer delay (maximum oscillator frequency).

Fref (pin20) – This is the 160 Hz reference frequency oscillator input. It is connected externally through a 60kΩ resistor to Vcc and a 0.1μF capacitor to Gnd. Other values of resistance and capacitance can be chosen, provided this input oscillates at 160 Hz. This frequency is used to drive the internal switched capacitor bandpass filter and the timing delays.

Other than just motion detector, KC788B also allows other functions such as Daylight adjust/sense, Gain select, ON/AUTO/OFF, and Toggle to be interfaced. However, after some tests of the circuit we can't efficiently use these extra functions, only the motion detection part worked well. Due to the high cost and difficulty in finding the IC, we decided to still use this IC since it satisfies our objective in movement detection alright. Sensitivity can be adjusted at pin 2. With the fresnel lens on the PIR movement sensor, the detecting area can be seen in the next page. There are 3 outputs from the movement sensor, those are Output , Vcc, and Ground. The output is high as 5V when there is no movement. It becomes low as 0V when

movement occurs. Therefore the output can be directly connected to microcontroller or other logic device. In this project we connect the movement detector output to AT89C51 microcontroller (P1.2) and a program is written so that any movement detected by the sensor, which causes the output to go low, would trigger the autodial unit, to start its work. The program can be referred to Appendix A.

The installation area is important because sensitivity would vary as the figure below. Sensors are more sensitive when they picking up movement travelling from left to right, or vice versa, instead to straight forward.

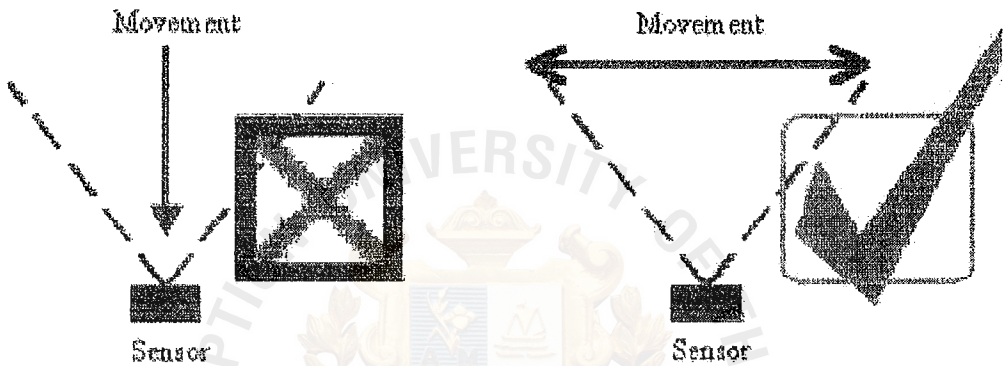


Figure 1.

Autodial

The purpose of autodial is to dial the stored telephone numbers automatically upon some trigger. In this project we do not want just to dial automatically but also to detect ringing and busy so that if the line is busy or nobody picks up, that specific number would be dialed again. The voice message being recorded in the voice IC would be played after the receiver of the call picks up the phone. Just a simple word "autodial" doesn't stand for a simple process and we divide this part further into some sub-parts for detailed discovery.

1) Speech network & tone decoder

Telephone Speech Network with Dialer Interface (MC34114) is the first chip we use to start the autodial part of this project and it's indeed a compulsory IC for autodial. How can we dial without a telephone in the first case? We want this autodial to be an individual piece so we do not interface with the telephone. Instead we use MC34114 which is actually a "telephone" in many ways. It already looks like a telephone in the block diagram (please refer to the datasheet in Appendix B) that one can see microphone and receiver. MC34114 is a speech network which interfaces with Tip and Ring and provides the 2-to-4 wire conversion. As shown in the block diagram in datasheet, the transmit gain 13 determined by the microphone amplifier (fixed gain of 30 dB), R_b, C5, the internal current gains of A1, A2, the AGC, and the line impedance in parallel with R1. The receive gain is determined by ZB, the internal current gains of A4 and the AGC, C8, and R8. Sidetone cancellation is determined by A3 and the ZB network. $\overline{\text{MUTE}}$ input at pin 17 disables the microphone amplifier and partially mute the receive amplifier while dialing when it is low. We can select to dial as pulse or tone and in this case we choose tone because of the DTMF dialer to be interfaced later. So pin 16 is low.

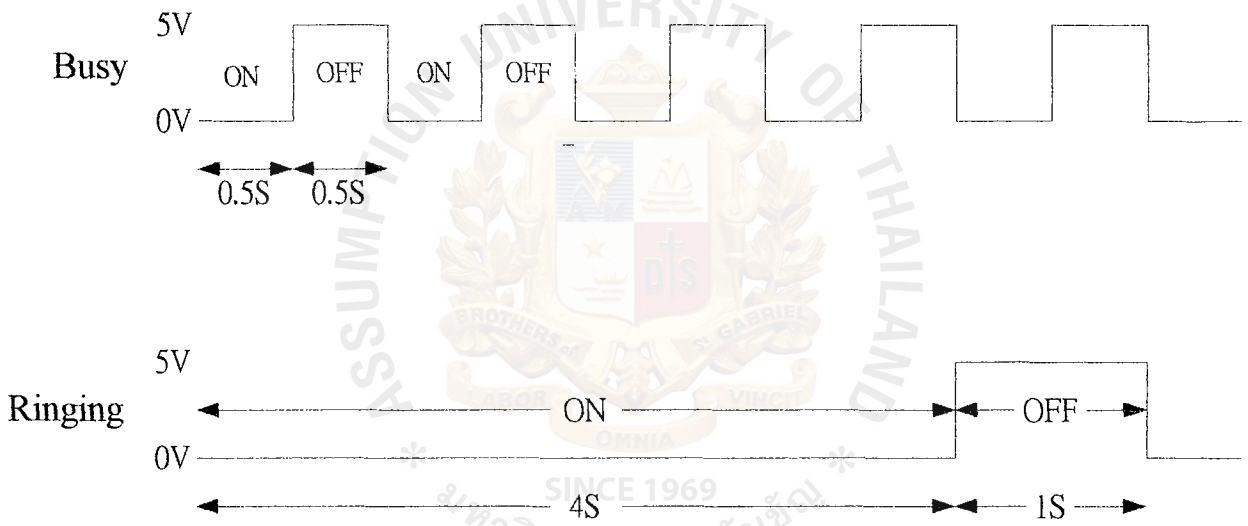
One question may come to one's mind. Who do the dialing? Well, we let 8 bit microcontroller to do the dialing with DTMF dialer, which will be described in later parts. After the dialing, a busy or ringing signal shall be heard at receiver output of MC34114(pin11). How can the microcontroller detect if the call is busy or ringing then? In this case we have to decode the incoming tone into binary signal so that microcontroller can understand. Tone decoder LM567 comes into the play, it is designed to provide a saturated transistor switch to ground when an input signal is present within the passband. It is found that the ringing and busy signal provided by the telephone central office is 400 Hz, so external components are set to adjust the passband which would pass and decode 400Hz as its center frequency, thus busy and

ringing signal would be decoded. When they are at the input of tone decoder. Resistor between pin5 and pin6 is calculated to be 22.7KΩ according to the design formula.

$$f_o = \frac{1}{1.1R_1C_1}$$

$$R_1 = \frac{1}{1.1f_oC_1} = \frac{1}{1.1 \times 400 \times 0.1 \times 10^{-6}} = 22.7K\Omega$$

Practically we choose 22KΩ because it works better than 22.7KHz after the testing. Now, whenever busy or ringing signal is fed into the LM567 at pin3, it decodes and output is low whenever the busy or ringing signal is present, which is 400Hz. Resulted busy and ringing signals are as follows:



This binary output from tone decoder thus can be used and understood by the microcontroller. We use pin 10 in AT89C51 microcontroller to accept the input from tone decoder to be used in the purpose of detecting line status (ringing or busy).

2) DTMF (Touch–tone) Generator

TP5089 DTMF Generator is commonly used with keypad to provide DTMF tones for dialing. It is also called a DTMF dialer. This chip is to be interfaced with MC34114 at pin10 to provide DTMF tones for dialing. As mentioned earlier, microcontroller will do the dialing thus we do not use keypad to provide DTMF tones, microcontroller itself can be programmed and interfaced with this chip to provide desired DTMF tones. As one can see from the datasheet (not the next figure), there are pins for the keypad input as columns and rows.

	COL1	COL2	COL3	COL4
ROW1	1	2	3	N1
ROW2	4	5	6	N2
ROW3	7	8	9	N3
ROW4	*	0	#	N4

Figure 2. Keypad

The pins corresponding to the column and row inputs in TP5089 are low-active. If we press 1, column 1 (pin 3) and row 1(pin14) would be low and that specific DTMF tone is generated.

With Port 0 of AT89C51 microcontroller connected to the corresponding pins of columns and rows (refer to chapter 3), we can program the microcontroller to dial the number we want referring to the table below.

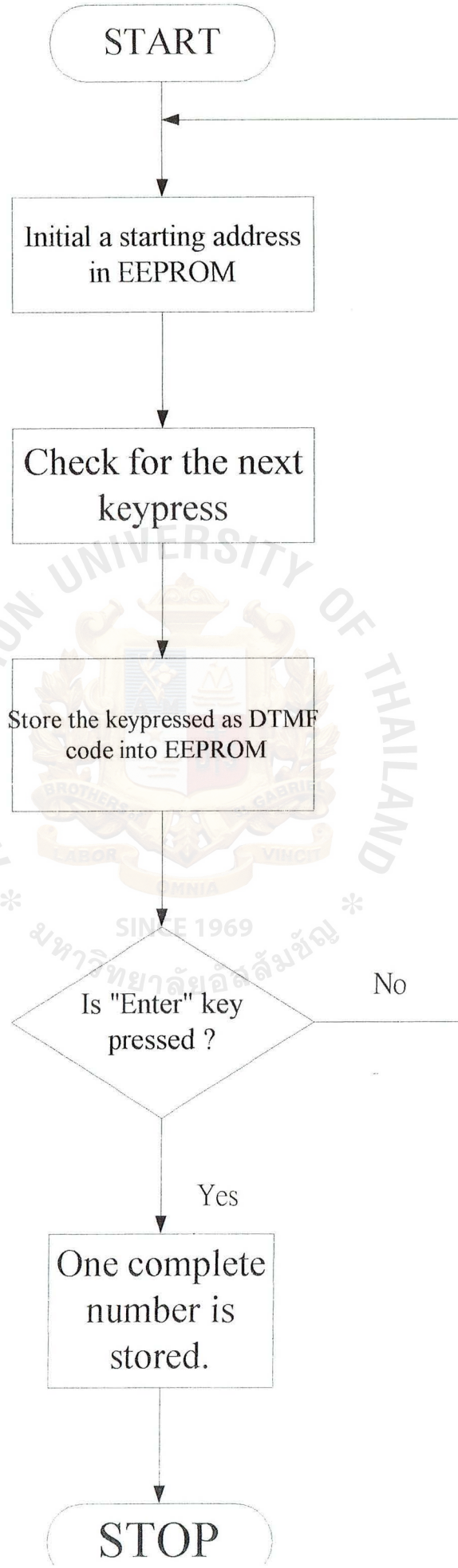
Number	**Column**	**Row**	**Bits assigned to Port 0 (binary)**	**Bits assigned to Port 0 (Hex)**
1	1	1	1110 1110	EE
2	2	1	1101 1110	DE
3	3	1	1011 1110	BE
4	1	2	1110 1101	ED
5	2	2	1101 1101	DD
6	3	2	1011 1101	BD
7	1	3	1110 1011	EB
8	2	3	1101 1011	DB
9	3	3	1011 1011	BB
*	1	4	1110 0111	E7
0	2	4	1101 0111	D7
#	3	4	1011 0111	B7

Table 1.

Thus, the generated DTMF tones from TP5089 used for dialing are not pressed from keypad but by microcontroller. We can now program any desired number to be dialed automatically by microcontroller.

3) Telephone number storage in EEPROM

The telephone numbers to be dialed to give the warning message should be stored in external memory and can be changed by the user anytime. In the design of this project we choose to store the numbers in 2-wire serial EEPROM AT24C01A. by microcontroller program. Program in Assembly language is written to write data into the EEPROM AT24C01A, one can refer to the Appendix A for the program. We programmed to give each number 25 digits, so that pager number can be stored and dialed as well, such as 1500 (pager station) – 760254 (pager number) – 12345678 (any number to be used as a "alarm number"). The numbers to be stored are pressed from the keypad which is interfaced with MM74C922 16 Key Encoder. Pin14~17 of MM74C922 are connected to Port1.4~1.7 of AT89C51 microcontroller. Whenever a number is pressed from keypad, there is a certain output at pin14~17 for that certain number pressed as shown in page 3 of the datasheet. Thus when keypad is pressed, a certain code would appear at pin14~17 and P1.4~1.7 of microcontroller, and microcontroller is programmed to differentiate what is the number being pressed and store that number in respective binary or hex form according to the Table 1 given previously in section "DTMF Generator". For example, when 5 is pressed, code at P.1.4-P.1.7 would be 0101 and microcontroller will store it as DDH in EEPROM for the use of DTMF dialing. Referring to the keypad shown in the Figure 2, N_1 to N_4 are the four keys to store the four telephone numbers. In order to store the 4 telephone numbers, N_1 is to be pressed and followed by the numbers to be stored as the 1st number, N_2 is for the 2nd number, and so on. The flow chart of the number storage process is as follows:

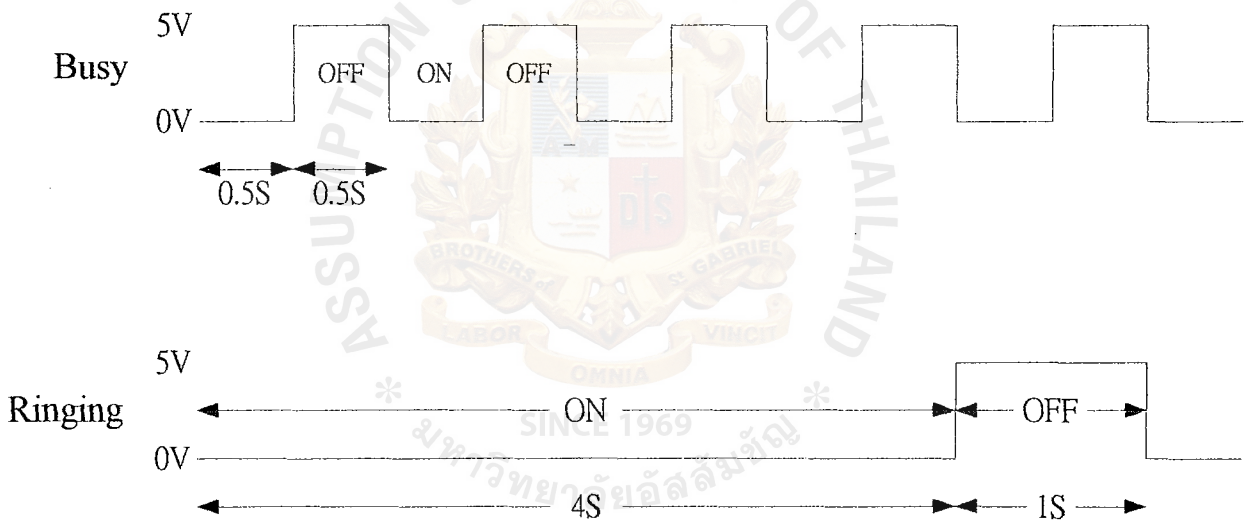


4) Taking out the stored numbers and dial

After the telephone numbers are stored into AT24C01 EEPROM, the next step is to read out each number correctly and dial. The program to read the data from EEPROM is written in Assembly language and can be referred to Appendix A section. The numbers stored in EEPROM are not in decimal form but in hex form according to the requirement of DTMF generator shown in the Table 1. So number 2 is stored as DEH or 11011110b. Thus, each number is read out from EEPROM and given to DTMF generator through P0 of microcontroller, DTMF generator will generate out the correct tone upon the data received, and dialing is done in this way.

5) Detection of busy signal and ringing signal

After the number is dialed, the microcontroller will get the busy or ringing signal from Tone Decoder (LM567) at P3.0 as shown below.



Whenever the signal is present (ON) about 400 Hz, tone decoder decodes it to be low. When no signal about 400HZ is available (OFF), tone decoder doesn't decode and output is high. 400Hz is the frequency given by the central office for both busy and ringing signal and we have designed the Tone Decoder so that 400Hz is within the passband for decoding. As one can observe from the timing diagram above the ON and OFF time for busy signal is the same and equal to 0.5 second whereas for ringing signal the ON time is 4 second and OFF time is 1 sec. Therefore, the program is written to compare the ON and OFF time of the input signal. If they are equal or about to be equal, microcontroller will understand it as busy signal as programmed. When busy signal is detected, microcontroller will cut or release the relay which will in turn off–hook the telephone line through the tip and ring interfaced with MC34114 Speech Network. Whenever the ON time and OFF time are not

equal, ON time is 4 seconds and OFF time is 1 second, the signal is to be taken as ringing signal when it is detected to be high at 4.5 second. When ringing signal is detected, microcontroller will count for 6 rings as programmed. If no one picks up, line is cut by release the relay. If the line is picked up, a recorded voice message will be played, this part will be further described in next section.

6) Display of the voice message

After phone calls are made and picked up, a warning message recorded in Single–Chip Voice Record/Playback Devices ISD2590 is played. Detailed description of this chip can be referred to the datasheet in Appendix B. There are many operational modes available in this chip and we choose Push–Button mode in this project. In Push–Button mode $\overline{CE}$ at pin 23 acts as a low going pulse–activated START/PAUSE signal. If no operation is currently in progress, a LOW-going pulse on this signal will initiate a playback or a record cycle according to the level on the P/R pin at pin 27. PD at Pin 24 acts as HIGH-going pulse-activated STOP/RESET signal. When a playback or record cycle is in progress and a HIGH-going pulse is observed on PD, the current cycle is terminated. The process of recording is as follows:

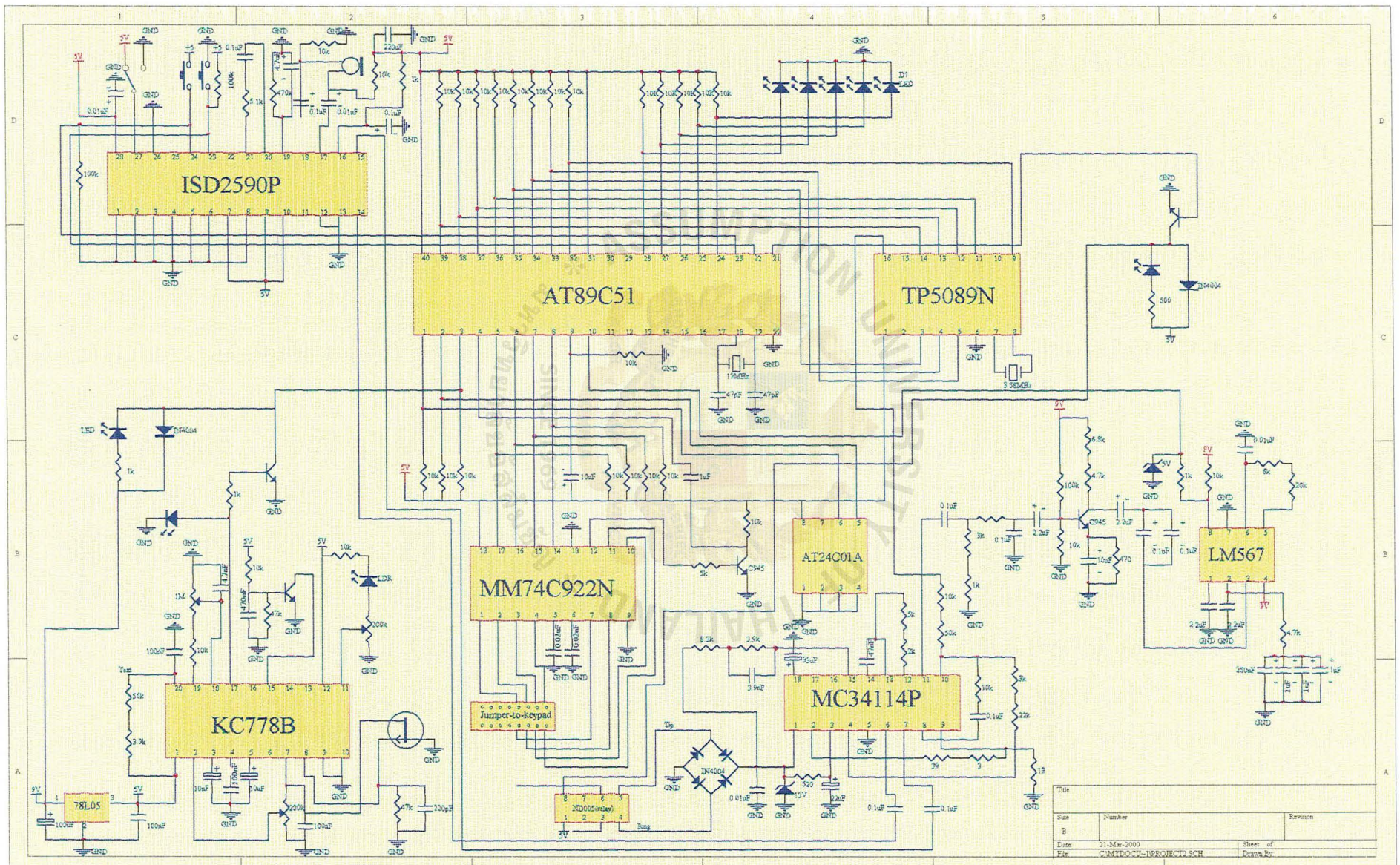
1) Switch to Record Mode (connect pin 27 P/R to ground)
2) Press and release START/PAUSE button (pin 23 $\overline{CE}$ is pulsed to ground)
3) Speak to the microphone
4) Press and release STOP/RESET button when message is finished (pin 24 PD is pulsed to Vcc) to stop the recording.
5) Voice is recorded

The process of playback is as follow:

1) Switch to Playback Mode (connect pin 27 P/R to Vcc)
2) Press START/PAUSE (pin 23 $\overline{CE}$ is pulsed to ground)
3) The message recorded is played out through the speaker
4) Press STOP/RESET (pin 24 PD is pulsed to Vcc) to stop the message anytime

Microcontroller is programmed to start the playback process which the call is picked up. However, record or playback mode has to be switched manually. It should be in the playback mode when working with autodial. Pin 23 and pin 24 from ISD2590 are connected directly to pin 22 (P2.1) and pin 23 (P2.2) of AT89C51 microcontroller, thus it is possible to assign the START and STOP of the playback by microcontroller.

CHAPTER 3 FABRICATION


ISD2590P
AT89C51
TP5089N
MM74C922N
AT24C01A
MC34114P
KC778B
LM567
78L05
Jumper-to-keypad
ND005(relay)
Title
Size
B
Number
Revision
Date: 21-Mar-2000
Sheet of
File: C:\MYDOCU~1\PROJECT2.SCH
Drawn By:

CHAPTER 4 TEST AND EQUIPMENT

Test 1 Test movement detector

Experiment Upon the completion of movement detector, it is to be tested for its sensitivity. LED should light whenever there is a movement detected.

Procedure Movement is made in front of the PIR sensor for different distance.

Problem 1 The movement detector does not work for the first 5 seconds.

Cause The movement detector needs a warm-up time when it is switched on.

Solution A warm-up period is to be allowed to the movement detector.

Problem 2 The LED1 at pin 16 does not work properly and there is no output from this pin after testing.

Cause The IC may be malfunctioning or broken in some way. Due to the difficulty in getting another one, we modified the circuit with the pins which are working properly.

Solution Connect all the components with pin 16 to pin 17 and leave pin 16 open because Pin 17 is working well and gives the output for sensing the movement. Thus both LED are now the output for movement detection.

Test 2 Tone Decoder LM567

Experiment Check to see if the tone decoder will decode 400Hz as desired and designed.

Procedure Use function generator to supply a 400Hz signal in square wave as the input to tone decoder. Observe the output of tone decoder with oscilloscope to see if it is low when 400Hz is at the input.

Test 3 Speech Network MC34114

Experiment Make sure the speech network IC is working properly like a telephone and dialing tone, busy tone, and ringing tone can be heard at pin 11 which is to be connected with a speaker.

Procedure Connect all necessary components and a telephone in parallel at tip and ring. For busy or ringing tone listen to the speaker and dial any number by the telephone in parallel.

Problem 1 The output from the speaker is very noise that the tone decoder won't decode anything when it is connected as input and tone decode.

Cause Unavoidable noise from the line, equipment, or environment is present.

Solution Connect a bandpass filter which filters out the frequencies below and above 400Hz. Resistor and capacitors are calculated so that 400Hz is within the passband range.

Problem 2 After the noise is filtered out, the clean output is connected to the tone decoder. However, the tone decoder still doesn't decode any signal.

Cause The input signal voltage is too small

Solution Amplify the signal from the filter by connecting a BJT amplifier circuit, then send the amplified signal to tone decoder.

Test 4 DTMF tone generator (TP 5089)

Experiment Check if the proper tone is produced at pin 16

Procedure 1 Connect keypad to the corresponding pins, connect pin 16 of DTMF tone generator to pin 10 of MC34114 speech network IC as a the DTMF dialer input.

Procedure 2 Interface the DTMF tone generator with microcontroller and write program which dial the number.

Problem 1 The output tone is too loud

Solution Connect a resistor before connecting to MC34114

Test 5 MC34114 Speech Network with TP5089 DTMF Generator

Experiment To dial phone number by DTMF generator TP5089

Procedure Connect the output from TP5089 to pin 10 of MC34114 which is used as input from DTMF dialer.

Problem 1 It decodes only first 2 column, not the third one.

Cause The speech network circuit was not connected completely.

Solution Connect as on the circuit diagram that pin 10 is to be connected to pin 4.

Test 6 16-Key Keypad

Experiment Check row and column of the keypad in order to know which are should be connected to the 16-key encoder MM 74C922 according to pin assignment.

Procedure Use the multimeter to check the shorting (while pressing the keypad) of each row and column then collect the result.

Test 7 16-Key Encoder (MM 74C922)

Experiment Check the output from the encoder

Procedure Press any key from the keypad and detect the output from the encoder by logic tester to see if the output is the same according to the key pressed by comparing the output with the table in page 3 of the datasheet.

Test 8 EEPROM AT24C01A

Experiment Check to see if correct numbers are stored.

Procedure Connect the EEPROM to microcontroller (as shown in chapter 3). Press the numbers by keypad. Load the data from the EEPROM by emulator.

Problem 1 The numbers are not the same as pressed.

Cause The rhythm in pressing the numbers may be too fast or keys are not pressed strongly enough to give an output.

Solution Rewrite the program and reduce the delay between detection of the number pressed and light up a LED after the EEPROM has successfully store one number. Thus, only when the LED lights up, the next number is pressed.

Test 9 Voice IC ISD2590

Experiment Check the working of recording and payback.

Procedure After all the components are set up, record and play the voice as instructed in Chapter 2 Theory and Design under "Display voice message".

Equipment	Quantity
AT89C51 Microcontroller	1
MM74C922 Keypad encoder	1
AT24C01 EEPROM	1
TP5089 DTMF generator	1
MC34114 Speech Network	1
LM 567 Tone Decoder	1
ISD 2590 Voice IC	1
KC 778B Movement detector	1
PIR sensor	1
Fresnel Lens	1
C945 BJT	5
Relay	1
Switch	4
Microphone	1
Speaker	1
LED	8
Crystal 3.579 MHz	1
Crystal 12 MHZ	1
Zener Diode	2
IN4004 Diode	6
16-Keypad	1
Resistors	71
Capacitors	50

CHAPTER 5 CONCLUSION AND RECOMMENDATION

After the completion of this project, we have learned a lot of things which we can't learn from the textbooks but only from experiences. Months of time have been spent in testing this project but the result is not very satisfactory. We took more than enough time because we were inexperienced in practical designing and programming. Although we may have connected the circuits as it appears in the data sheet, it will never just work right away. A lot of testing were always needed and many mistake were made by us which should be avoided, such as Vcc and GND which are compulsory in almost every IC. Or the plug of ETS 7000 must be 2 head instead of 3 when testing with MC34114. Due to the lack of experience we once spend week time testing a broken IC as well. However, these things made us learn so that we don't make this unforgivable mistakes outside.

Programming was difficult to begin because we weren't familiar with it. Flow chart was written before we write any program. It was not that difficult after we started writing and we did finished many parts such as storing data into EEPROM, dialing the stored numbers, and detecting busy and ringing. However, when we combined them together they do not work so well. Therefore the results are not very satisfactory. Many things need to be improved, both software and hardware. One major problem with our autodial circuit is the way get busy and ringing signals. We used LM 567 to decode the busy and ringing tones to be used by microcontroller. However, the tone is varying every time and so must the resistor too at pin5 and pin6. Once the signal can't be decoded nicely with the right timing, the microcontroller can't detect the busy and ringing as programmed. The program is okay but it has to work with a properly decoded signal. Another problem is that other than house phones, cellular phones can't be used due to the difference in ringing tones. Furthermore, different types of cellular phone (800, 900, 1800)has different ringing tone. Thus the tone decoding method is not very efficient after all. This autodial circuit should be improved with a modem chip, which can detect whatever busy and ringing signals from anywhere.

Although it was not a fully completed project, we are glad to have gained experiences and practical knowledges and found ourselves to be more interested in Engineering.

For the improvement of this project, one should find a method in replacement of the tone decoder method, such as to detect busy and ringing by modem chip. Password protection should also be included so that only the owner can store the autodialing numbers. Battery charger should be used instead of adapter so that it can

still work when electricity is off. Finally, the movement detector should be wireless when interfacing with autodial circuit so that installation is easier.

Appendix A Programming Operation

```
P0        DATA 080H
P1        DATA 090H
P2        DATA 0A0H
P3        DATA 0B0H
PSW       DATA 0D0H
ACC       DATA 0E0H
ERRFAG    BIT  027H
IPSCL     EQU  P1.0
IPSDA     EQU  P1.1
TRIG      EQU  P1.2
DATAEN    EQU  P1.3
RELAY     EQU  P2.0          ;
VSIG_ON   EQU  P2.1          ;Start button
VSIG_OFF  EQU  P2.2          ;Stop button
RSIG      EQU  P3.0          ;Ringing Signal

B         DATA 0F0H
TEST      DATA 020H
COUNTER   DATA 021H
CNTB      DATA 022H
MEM1      DATA 023H
MEM2      DATA 024H
MEM3      DATA 025H
MEM4      DATA 026H
MODEL     DATA 028H
AGAIN     DATA 029H
COUNTER1  DATA 02AH

;--------------------CHECK_SENSOR----------------------------------------


MOV P2,#00000110B
SETB TRIG
CALL DELAY1
CALL DELAY1
CALL DELAY1
CALL DELAY1
CALL DELAY1
```

```
SENSOR:
SETB    VSIG_OFF                ;press stop button for voice
nop
nop
nop
nop
nop
CLR     VSIG_OFF                ;release stop button for voice
CLR     A
SETB    DATAEN
SETB    TRIG
JNB     TRIG,PROCEDURE1
JNB     DATAEN,GOTO_CHECK1
SJMP    SENSOR

GOTO_CHECK1:
LJMP CHECK1

PROCEDURE1:
CLR     P2.7
CLR     P2.6
CLR     P2.5
CLR     P2.4
CLR     P2.3
SETB    VSIG_OFF                ;press stop button for voice
CALL    DELAY
CLR     VSIG_OFF                ;release stop button for voice
SETB    VSIG_ON                 ;unpress start button for voice
MOV     R6,#00H                 ;counter for low signal
MOV     R7,#00H                 ;counter for high signal
MOV     R5,#28H                 ;counter for pickup(high) signal
MOV     COUNTER,#01H            ;counter for calling next number
MOV     CNTB,#00H
MOV     MODEL,#00H
MOV     AGAIN,#00H
MOV     COUNTER1,#00H
```

```
ADD1:
MOV     R0,#04H             ;set start address for EEPROM (1st number)
SETB    RELAY               ;off-hook the phone
MOV     CNTB,#00H

CALL_N1:                    ;call the 1st stored number
CALL    DELAY               ;
CALL    DELAY               ;
INC     R0                  ;
CALL    IPR                 ;get the number from EEPROM with specified R0
MOV     P0,R1               ;output the number from EEPROM
CALL    DELAY
CALL    DELAY
MOV     P0,#00H             ;clear P0
INC     CNTB
LJMP    ENTER

ADD2:
CLR     A
MOV     R0,#1DH             ;set start address for EEPROM (2nd number)
SETB    RELAY               ;off-hook the telephone
MOV     CNTB,#00H
CALL    CALL_N1

ADD3:
CLR     A
MOV     R0,#36H             ;set start address for EEPROM (3rd number)
SETB    RELAY               ;off-hook the telephone
MOV     CNTB,#00H
CALL    CALL_N1

ADD4:
CLR     A
MOV     R0,#4FH             ;set start address for EEPROM (3rd number)
SETB    RELAY               ;off-hook the telephone
MOV     CNTB,#00H
CALL    CALL_N1
```

```
ENTER:                          ;check if the keypressed is ENTER
CJNE    R1,#22H,PAUSE
CLR     A
LJMP    CALL_ACK                ;if keypressed is ENTER go to CALL_ACK

PAUSE:                          ;check is the keypressed is PAUSE
CJNE    R1,#33H,CALL_N1
CALL    DELAY
CALL    DELAY
CALL    DELAY
CALL    DELAY
CALL    DELAY
CALL    DELAY
LJMP    CALL_N1

CALL_ACK:                       ;starting to check if line is busy or ringing
SETB    RSIG
SETB    P2.3
CALL    DELAY2
CLR     P2.3
INC     COUNTER1
MOV     A,COUNTER1
CJNE    A,#36H,CALL_ACK1
LJMP    VOICE

CALL_ACK1:
JB      RSIG,CALL_ACK           ;when signal is low go to RESET


RESET:                          ;counts how long low signal is
CALL    DELAY2                  ;0.125sec + 1 us
MOV     R3,#0FAH                ;1 us
MOV     R3,#0FAH                ;1 us
MOV     R3,#0FAH                ;1 us
MOV     R3,#0FAH                ;1 us
MOV     R3,#0FAH                ;1 us
INC     R6                      ;1 us
```

```
JNB     RSIG,RESET              ;go to SET1 when signal is high (2 us)

SET1:                           ;counts how long high signal is
CALL    DELAY2                  ;0.125s
DEC     R5
INC     R7
CJNE    R5,#00H,HIGH1           ;2 us
LJMP    VOICE                   ;if high signal is 5sec then go to VOICE

HIGH1:
JB      RSIG,SET1               ;whenever the signal is low again start to
SJMP    COMPARE                 ; compare, or else keep on counting

COMPARE:                        ;compare the low and high signal
MOV     A,R7
MOV     TEST,R6
SUBB    A,TEST                  ;subtract the duration of high and low
CJNE    A,#00H,COMPARE1         ;if they are not equal compare again
LJMP    BUSY                    ;if they are equal go to BUSY

COMPARE1:                       ;compare the low and high signal(2nd)
CJNE    A,#01H,COMPARE2         ;if they are not differed by 1 compare again
LJMP    BUSY                    ;if they are differed by 1 go to BUSY

COMPARE2:                       ;compare low and high signal (3rd)
CJNE    A,#02H,COMPARE3         ;if they are not differed by 2 compare again
LJMP    BUSY                    ;if they are differed by 2 go to BUSY

COMPARE3:                       ;compare low and high signal (4th)
CJNE    A,#03H,COMPARE4         ;if they are not differed by 3 compare again
LJMP    BUSY                    ;if they are differed by 3 go to BUSY

COMPARE4:                       ;compare low and high signal (5th)
CJNE    A,#04H,COMPARE5         ;if they are not differed by 4 compare again
LJMP    BUSY                    ;if they are differed by 4 go to BUSY

COMPARE5:                       ;compare low and high signal (last)
CJNE    A,#05H,RINGING          ;if they are differed more than 5 go RINGING
```

```
LJMP    BUSY                    ;if they are differed by 5 go to BUSY


BUSY:                           ;signal detected is busy
CLR     RELAY                   ;on-hook the telephone
CALL    DELAY1
CALL    DELAY1
CALL    DELAY1
CLR     A
LJMP    STORE


RINGING:                        ;signal detected is ringing
CLR     A
RINGING1:
JNB     RSIG,RINGING1
SETB    P2.7
CALL    DELAY1                  ;call
CALL    DELAY1                  ;     delay
CALL    DELAY1                  ;          for
CALL    DELAY1                  ;               4.5
CALL    DELAY1                  ;                    seconds
CALL    DELAY1                  ;                         check!
CLR     P2.7
JNB     RSIG,CHECK11            ;if low check again
LJMP    VOICE                   ;if high go to VOICE


INCREASE:
CLR     P2.6
SETB    P2.6
CALL    DELAY2
CLR     P2.6
INC     A
CJNE    A,#03H,RINGING1         ;count ringing for 6 times
LJMP    NOPICK                  ;go to NOPICK after 6 ringing

CHECK11:
```

```
CLR     P2.5
SETB    P2.5
CALL    DELAY2
CLR     P2.5
JNB     RSIG,CHECK22            ;check again if signal is low
SJMP    VOICE                   ;if not go to VOICE

CHECK22:
CLR     P2.4
SETB    P2.4
CALL    DELAY2
CLR     P2.4
JNB     RSIG,INCREASE           ;check if signal is still low
SJMP    VOICE                   ;if not go to VOICE

VOICE:
CALL    DELAY2
JNB     RSIG,INCREASE           ;check for if signal is low to make sure
CALL    DELAY2
JNB     RSIG,INCREASE           ;check for if signal is low to make sure
CALL    DELAY2
JNB     RSIG,INCREASE           ;check for if signal is low to make sure
CALL    DELAY2
JNB     RSIG,INCREASE           ;check for if signal is low to make sure
CALL    DELAY2
JNB     RSIG,INCREASE           ;check for if signal is low to make sure
CALL    DELAY2
JNB     RSIG,INCREASE           ;check for if signal is low to make sure
CALL    DELAY2
JNB     RSIG,INCREASE           ;check for if signal is low to make sure
CALL    DELAY2
JNB     RSIG,INCREASE           ;check for if signal is low to make sure
CALL    DELAY2
JNB     RSIG,INCREASE           ;check for if signal is low to make sure
CALL    DELAY2
JNB     RSIG,INCREASE           ;check for if signal is low to make sure
SETB    VSIG_OFF                ;press STOP for voice
CALL    DELAY
```

```
CLR     VSIG_OFF            ;release STOP for voice
CLR     VSIG_ON             ;press START for voice
CALL    DELAY
CALL    DELAY
SETB    VSIG_ON             ;release START for voice
CALL    DELAY               ;call
CALL    DELAY               ;     delay
CALL    DELAY               ;           to
CALL    DELAY               ;              play
CALL    DELAY               ;                  the
CALL    DELAY               ;                      recorded
CALL    DELAY               ;                              voice
CALL    DELAY               ;call
CALL    DELAY               ;     delay
SETB    VSIG_OFF            ;press STOP for voice
CALL    DELAY
CLR     VSIG_OFF            ;release STOP for voice
CLR     RELAY               ;on-hook the telephone
CLR     A
CALL    DELAY1
CALL    DELAY1
CALL    DELAY1
SJMP    CHK1                ;go to CHK1 to call next number


NOPICK:                     ;no one pick up the phone
CLR     RELAY               ;on-hook the telephone
CLR     A
CALL    DELAY1
CALL    DELAY1
CALL    DELAY1
LJMP    STORE               ;


CHK1:
MOV     A,MODEL
CJNE    A,#00H,CALL_LEFT1
INC     COUNTER
```

```
MOV     A,COUNTER
CJNE    A,#02H,CHK2             ;if counter counts 2 then call the-
LJMP    ADD2                    ;-2nd number

CHK2:
CJNE    A,#03H,CHK3             ;if counter counts 3 then call the-
LJMP    ADD3                    ;-3rd number

CHK3:
CJNE    A,#04H,CALL_LEFT1       ;if counter counts 4 then call the-
LJMP    ADD4                    ;number in temp memory

CALL_LEFT1:
MOV     MODEL,#01H
INC     AGAIN
MOV     A,MEM1
CJNE    A,#04H,CALL_LEFT2
LJMP    ADD1

CALL_LEFT2:
INC     AGAIN
MOV     A,MEM2
CJNE    A,#1DH,CALL_LEFT3
LJMP    ADD2

CALL_LEFT3:
INC     AGAIN
MOV     A,MEM3
CJNE    A,#36H,CALL_LEFT4
LJMP    ADD3

CALL_LEFT4:
INC     AGAIN
MOV     A,MEM4
CJNE    A,#4FH,OVER
LJMP    ADD4

SUBCHECK:
```

```
LJMP    CHK1

PRESET:
MOV     A,AGAIN
CJNE    A,#01H,PRESET1
LJMP    CALL_LEFT2

PRESET1:
CJNE    A,#02H,PRESET2
LJMP    CALL_LEFT3

PRESET2:
CJNE    A,#03H,OVER
LJMP    CALL_LEFT4

OVER:
SJMP    $

STORE:
MOV     A,MODEL
CJNE    A,#00H,PRESET
CLR     P2.7
SETB    P2.7
CALL    DELAY
CLR     P2.7
MOV     A,R0
SUBB    A,CNTB
CJNE    A,#04H,STORE1
MOV     MEM1,A
LJMP    SUBCHECK

STORE1:
CLR     P2.6
SETB    P2.6
CALL    DELAY
CLR     P2.6
CJNE    A,#1DH,STORE2
```

```
MOV     MEM2,A
LJMP    SUBCHECK

STORE2:
SETB    P2.5
CALL    DELAY
CLR     P2.5
CJNE    A,#36H,STORE3
MOV     MEM3,A
LJMP    SUBCHECK

STORE3:
SETB    P2.4
CALL    DELAY
CLR     P2.4
CJNE    A,#4FH,SUBCHECK
MOV     MEM4,A
LJMP    SUBCHECK


;-----------------------CHECK_KEYPRESSED-----------------------------------
MAIN:
MOV     P2,#00H
CLR     A
SETB    DATAEN
JB      DATAEN,SUB2
MOV     A,P1
ANL     A,#11110000B
LJMP    CHECK1

SUB2:
LJMP    SENSOR
;-------------------------------CHECK_N-----------------------------------
GET_N1:
MOV     R0,#04H
MOV     P2,#00H
MOV     P2,#10000000B
```

```
LJMP    GET_KEYPRESSED

GET_N2:
MOV     R0,#1DH
MOV     P2,#00H
MOV     P2,#01000000B
LJMP    GET_KEYPRESSED

GET_N3:
MOV     R0,#36H
MOV     P2,#00H
MOV     P2,#00100000B
LJMP    GET_KEYPRESSED

GET_N4:
MOV     R0,#4FH
MOV     P2,#00H
MOV     P2,#00010000B
LJMP    GET_KEYPRESSED
;-------------------------------CHECK_NUMBER-----------------------------
GET_KEYPRESSED:
CLR     A
SETB    DATAEN
CALL    SHORTDELAY
JB      DATAEN,GET_KEYPRESSED
CALL    DELAY
INC     R0
                                ;check if keypressed is "one"
MOV     A,P1                    ;get P1(keypressed) and copy into A
ANL     A,#11110000B            ;masK LOWER bits
CJNE    A,#00000000B,CHK_NUM0   ;if keypressed is not 1, check for "ZERO"
MOV     R1,#11101110B
CALL    IPW
SETB    P2.3
CALL    DELAY
CLR     P2.3
LJMP    GET_KEYPRESSED
```

```
CHK_NUM0:
MOV     A,P1                    ;get P1(keypressed) and copy into A
ANL     A,#11110000B            ;masK LOWER bits
CJNE    A,#11010000B,CHK_NUM2   ;if keypressed is not 0, check for "two"
MOV     R1,#11010111B
CALL    IPW
SETB    P2.3
CALL    DELAY
CLR     P2.3
LJMP    GET_KEYPRESSED


CHK_NUM2:                       ;check if keypressed is "two"
MOV     A,P1                    ;get P1(keypressed) and copy into A
ANL     A,#11110000B            ;masK LOWER bits
CJNE    A,#00010000B,CHK_NUM3   ;if keypressed is not 2, check for "three"
MOV     R1,#11011110B
CALL    IPW
SETB    P2.3
CALL    DELAY
CLR     P2.3
LJMP    GET_KEYPRESSED


CHK_NUM3:                       ;check if keypressed is "three"
MOV     A,P1                    ;get P1(keypressed) and copy into A
ANL     A,#11110000B            ;masK LOWER bits
CJNE    A,#00100000B,CHK_NUM4   ;if keypressed is not 3, check for "four"
MOV     R1,#10111110B
CALL    IPW
SETB    P2.3
CALL    DELAY
CLR     P2.3
LJMP    GET_KEYPRESSED
```

```
CHK_NUM4:                       ;check if keypressed is "four"
MOV     A,P1                    ;get P1(keypressed) and copy into A
ANL     A,#11110000B            ;mask LOWER bits
CJNE    A,#01000000B,CHK_NUM5   ;if keypressed is not 4, check for "five"
MOV     R1,#11101101B
CALL    IPW
SETB    P2.3
CALL    DELAY
CLR     P2.3
LJMP    GET_KEYPRESSED

CHK_NUM5:                       ;check if keypressed is "five"
MOV     A,P1                    ;get P1(keypressed) and copy into A
ANL     A,#11110000B            ;masK LOWER bits
CJNE    A,#01010000B,CHK_NUM6   ;if keypressed is not 5, check for "six"
MOV     R1,#11011101B
CALL    IPW
SETB    P2.3
CALL    DELAY
CLR     P2.3
LJMP    GET_KEYPRESSED

CHK_NUM6:                       ;check if keypressed is "six"
MOV     A,P1                    ;get P1(keypressed) and copy into A
ANL     A,#11110000B            ;masK LOWER bits
CJNE    A,#01100000B,CHK_NUM7   ;if keypressed is not 6, check for "seven"
MOV     R1,#10111101B
CALL    IPW
SETB    P2.3
CALL    DELAY
CLR     P2.3
LJMP    GET_KEYPRESSED

CHK_NUM7:                       ;check if keypressed is "seven"
MOV     A,P1                    ;get P1(keypressed) and copy into A
ANL     A,#11110000B            ;masK LOWER bits
CJNE    A,#10000000B,CHK_NUM8   ;if keypressed is not 7, check for "eight"
```

```
MOV     R1,#11101011B
CALL    IPW
SETB    P2.3
CALL    DELAY
CLR     P2.3
LJMP    GET_KEYPRESSED


CHK_NUM8:                       ;check if keypressed is "eight"
MOV     A,P1                    ;get P1(keypressed) and copy into A
ANL     A,#11110000B            ;masK LOWER bits
CJNE    A,#10010000B,CHK_NUM9   ;if keypressed is not 8, check for "nine"
MOV     R1,#11011011B
CALL    IPW
SETB    P2.3
CALL    DELAY
CLR     P2.3
LJMP    GET_KEYPRESSED

CHK_NUM9:                       ;check if keypressed is "nine"
MOV     A,P1                    ;get P1(keypressed) and copy into A
ANL     A,#11110000B            ;masK LOWER bits
CJNE    A,#10100000B,CHK_PAUSE
MOV     R1,#10111011B
CALL    IPW
SETB    P2.3
CALL    DELAY
CLR     P2.3
LJMP    GET_KEYPRESSED

CHK_PAUSE:                      ;check if keypressed is "pause"
MOV     A,P1                    ;get P1(keypressed) and copy into A
ANL     A,#11110000B            ;mask LOWER bits
CJNE    A,#11000000B,CHK_ENTER
MOV     R1,#33H
CALL    IPW
SETB    P2.3
CALL    DELAY
```

```
CLR     P2.3
LJMP    GET_KEYPRESSED


CHK_ENTER:                          ;check if keypressed is "enter"
MOV     A,P1                        ;get P1(keypressed) and copy into A
ANL     A,#11110000B                ;masK LOWER bits
CJNE    A,#11100000B,JMP_GETKEYPRESSED
MOV     R1,#22H
CALL    IPW
SETB    P2.3
CALL    DELAY
CLR     P2.3
LJMP    MAINLOOP

MAINLOOP:
LJMP MAIN

JMP_GETKEYPRESSED:
DEC     R0
LJMP    GET_KEYPRESSED


CHECK1:
MOV     A,P1
ANL     A,#11110000B
CJNE    A,#00110000B,CHECK2     ;if keypressed is not N1 go to CHECK2
LJMP    GET_N1                  ;if kepressed is N1 go to GET_N1
RET

CHECK2:
CJNE    A,#01110000B,CHECK3     ;if keypressed is not N2 go to CHECK3
LJMP    GET_N2                  ;if kepressed is N2 go to GET_N2
RET

CHECK3:
CJNE    A,#10110000B,CHECK4     ;if keypressed is not N3 go to CHECK4
LJMP    GET_N3                  ;if kepressed is N3 go to GET_N3
```

```
RET

CHECK4:
CJNE    A,#11110000B,CHECK1      ;if keypressed is not N4 go to CHECK1
LJMP    GET_N4                   ;if kepressed is N4 go to GET_N4
RET

;-------Procedure To Write Byte To Serial EEProm-----------------

IPW:

;-------Provide Signals For Start Condition AT24C01A-------------
SETB    IPSDA
SETB    IPSCL
CLR     IPSDA
CALL    CDEL
CLR     IPSCL
SETB    IPSDA

;-----Device Signal Id 1010 and (Hardwired Address (XXXD)--------

MOV A,#10100000B
CALL IPWRB
JB   ERRFAG,IPW9

;------Serial Transfer Of EEPROM Byte Address--------------------

MOV     A,R0
ANL     A,#01111111B
CALL    IPWRB
JB      ERRFAG,IPW9

;-----Serial Transfer Of Data To Write To EEPROM-----------------

MOV     A,R1
CALL    IPWRB

;-----Provide Signals For Stop Condition AT24C01A----------------
```

```
IPW9:
CLR     IPSDA
SETB    IPSCL
CALL    CDEL
SETB    IPSDA
RET

;------Sub-Procedure To Shift And Write Serial Data--------------

IPWRB:
CLR     ERRFAG
MOV     R2,#8

;-----------Sub-Procedure Called By IPWRB-----------------------

IPWRB1:
RLC     A
MOV     IPSDA,C
CALL    CHIGH
CALL    CLOW
DJNZ    R2,IPWRB1

;----------Wait For EEPROM To Acknowledge-----------------------

SETB    IPSDA
CALL    CHIGH
JNB     IPSDA,IPWRB2
SETB    ERRFAG
;-------------Sub-Procedure To Return----------------------------

IPWRB2:
CALL    CLOW
RET

;------------Serial Clock High And Delay------------------------
CHIGH:
SETB    IPSCL
```

```
NOP
NOP
NOP
NOP
NOP
RET

;------------Serial Clock Low And Delay-------------------------

CLOW:
CLR     IPSCL
NOP
NOP
NOP
NOP
NOP
RET

;-----------Procedure To Provide Delay---------------------------

CDEL:
NOP
NOP
NOP
NOP
NOP
RET

;-----------------Procedure To Read Byte From Serial EEProm------------

IPR:
;---------------Provide Signals For Start Condition AT24C01A------------

SETB    IPSDA
SETB    IPSCL
CLR     IPSDA
CALL    CDEL
CLR     IPSCL
```

```
;-----------Device Signal Id 1010 and (Hardwired Address (XXXD)--------

MOV A,#10100000B
CALL IPWRB
JB   ERRFAG,IPR9
;-------------Serial Transfer Of EEPROM Byte Address--------------------

MOV     A,R0
ANL     A,#01111111B
CALL    IPWRB
JB      ERRFAG,IPR9

;------------Provide Signals For Stop Condition AT24C01A----------------

CLR     IPSDA
SETB    IPSCL
CALL    CDEL
SETB    IPSDA

;------------Provide Signals For Start Condition AT24C01A---------------

SETB    IPSDA
SETB    IPSCL
CLR     IPSDA
CALL    CDEL
CLR     IPSCL

;-----------Device Signal Id 1010 and (Hardwired Address (XXXR)--------

MOV A,#10100001B
CALL IPWRB
JB   ERRFAG,IPR9
CALL IPRDB
JB ERRFAG,IPR9
MOV R1,A

;------------Provide Signals For Stop Condition AT24C01A----------------
```

```
;-----------Device Signal Id 1010 and (Hardwired Address (XXXD)--------

MOV A,#10100000B
CALL IPWRB
JB   ERRFAG,IPR9
;-------------Serial Transfer Of EEPROM Byte Address--------------------

MOV     A,R0
ANL     A,#01111111B
CALL    IPWRB
JB      ERRFAG,IPR9

;------------Provide Signals For Stop Condition AT24C01A----------------

CLR     IPSDA
SETB    IPSCL
CALL    CDEL
SETB    IPSDA

;------------Provide Signals For Start Condition AT24C01A---------------

SETB    IPSDA
SETB    IPSCL
CLR     IPSDA
CALL    CDEL
CLR     IPSCL

;-----------Device Signal Id 1010 and (Hardwired Address (XXXR)--------

MOV A,#10100001B
CALL IPWRB
JB   ERRFAG,IPR9
CALL IPRDB
JB ERRFAG,IPR9
MOV R1,A

;------------Provide Signals For Stop Condition AT24C01A----------------
```

```
DJNZ R4,$
DJNZ R3,TDLAY1
RET

;-------------------Procedure To Provide Delay--------------------------

DELAY:
MOV R3,#0FFH
TDLAY2:
MOV R4,#0FFH
DJNZ R4,$
MOV R4,#0FFH
DJNZ R4,$
MOV R4,#0FFH
DJNZ R4,$
MOV R4,#0FFH
DJNZ R3,TDLAY2
RET
;---------------------DELAY FOR BUSYTONE--------------------------------;
DELAY1:
MOV     R3,#0FAH      ;1 uS
WDH:
MOV     R4,#0FAH      ; 1us
DJNZ    R4,$          ; 2 + 2*250
MOV     R4,#0FAH      ; 1us
DJNZ    R4,$          ; 2 + 2*250
MOV     R4,#0FAH      ; 1us
DJNZ    R4,$          ; 2 + 2*250
MOV     R4,#0FAH      ; 1us
DJNZ    R4,$          ; 2 + 2*250
MOV     R4,#0FAH      ; 1us
DJNZ    R4,$          ; 2 + 2*250
MOV     R4,#0FAH      ; 1us
DJNZ    R4,$          ; 2 + 2*250
DJNZ    R3,WDH        ; 2us + 250(30us+3000us)
RET
```

```
DELAY2:
MOV     R3,#0FAH
DE1:
MOV     R4,#0FAH
DJNZ    R4,$
DJNZ    R3,DE1
RET



END
```

Appendix B IC Data Sheet

8-Bit Microcontroller with 4K Bytes Flash

AT89C51

'eatures

- Compatible with MCS-51™ Products
- 4K Bytes of In-System Reprogrammable Flash Memory
  - Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

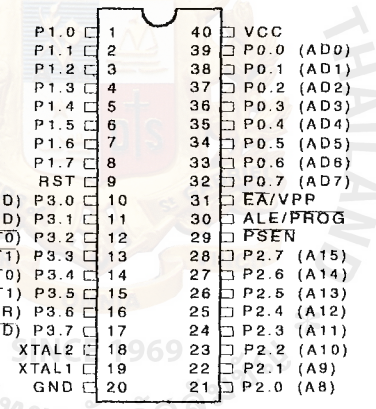
)escription

he AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K ytes of Flash Programmable and Erasable Read Only Memory (PEROM). The evice is manufactured using Atmel's high density nonvolatile memory technology nd is compatible with the industry standard MCS-51™ instruction set and pinout. The n-chip Flash allows the program memory to be reprogrammed in-system or by a conentional nonvolatile memory programmer. By combining a versatile 8-bit CPU with ash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which ovides a highly flexible and cost effective solution to many embedded control applitions.

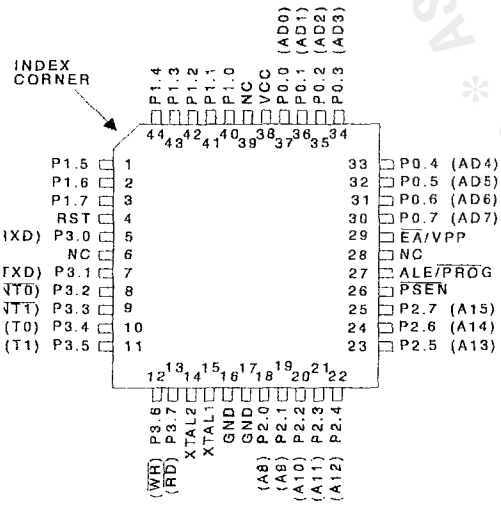
(continued)

'in Configurations

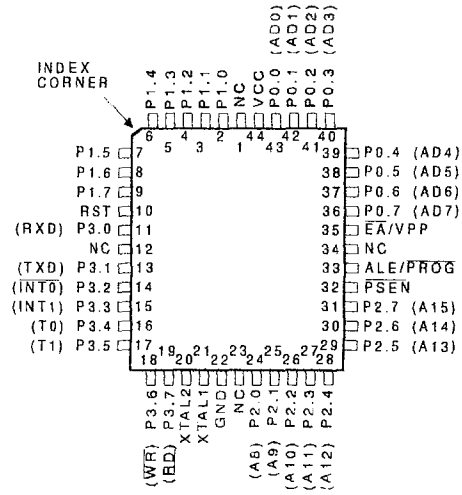
PDIP



PQFP/TQFP



PLCC



0265F-A-12/97

'eatures

- Low-Voltage and Standard-Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 2.5 (V_{CC} = 2.5V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 5.5V)
- Internally Organized 128 x 8 (1K), 256 x 8 (2K), 512 x 8 (4K), 1024 x 8 (8K) or 2048 x 8 (16K)
- 2-Wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 100 kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 8-Byte Page (1K, 2K), 16-Byte Page (4K, 8K, 16K) Write Modes
- Partial Page Writes Are Allowed
- Self-Timed Write Cycle (10 ms max)
- High Reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
  - ESD Protection: >3000V
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin and 14-Pin JEDEC SOIC, 8-Pin PDIP, 8-Pin MSOP, and 8-Pin TSSOP Packages

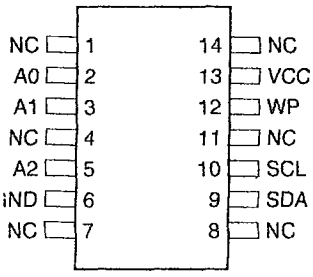
'escription

ıe AT24C01A/02/04/08/16 provides 1024/2048/4096/8192/16384 bits of serial elec-cally erasable and programmable read only memory (EEPROM) organized as 28/256/512/1024/2048 words of 8 bits each. The device is optimized for use in many dustrial and commercial applications where low power and low voltage operation are ssential. The AT24C01A/02/04/08/16 is available in space saving 8-pin PDIP, \T24C01A/02/04/08/16), 8-Pin MSOP (AT24C01A/02), 8-Pin TSSOP \T24C01A/02/04/08/16), and 8-Pin and 14-Pin JEDEC SOIC .T24C01A/02/04/08/16) packages and is accessed via a 2-wire serial interface. In ldition, the entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V), 2.5V .5V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

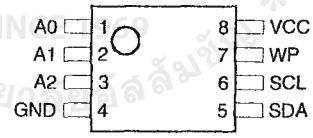
in Configurations

'in Name	Function
\0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
VP	Write Protect
IC	No Connect

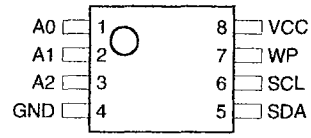
14-Pin SOIC



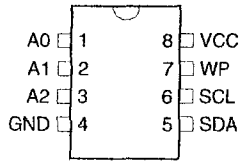
8-Pin TSSOP



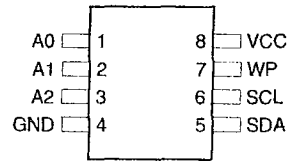
8-Pin MSOP



8-Pin PDIP



8-Pin SOIC



2-Wire Serial EEPROM

1K (128 x 8)

2K (256 x 8)

4K (512 x 8)

8K (1024 x 8)

16K (2048 x 8)

AT24C01A
AT24C02
AT24C04
AT24C08
AT24C16

Rev. 0180D–10/98

FAIRCHILD SEMICONDUCTOR™

October 1987
Revised January 1999

MM74C922 • MM74C923
16-Key Encoder • 20-Key Encoder

General Description

The MM74C922 and MM74C923 CMOS key encoders provide all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. These encoders also have on-chip pull-up devices which permit switches with up to 50 kΩ on resistance to be used. No diodes in the switch array are needed to eliminate ghost switches. The internal debounce circuit needs only a single external capacitor and can be defeated by omitting the capacitor. A Data Available output goes to a high level when a valid keyboard entry has been made. The Data Available output returns to a low level when the entered key is released, even if another key is depressed. The Data Available will return high to indicate acceptance of the new key after a normal debounce period; this two-key roll-over is provided between any two switches.

An internal register remembers the last key pressed even after the key is released. The 3-STATE outputs provide for easy expansion and bus operation and are LPTTL compatible.

Features

- 50 kΩ maximum switch on resistance
- On or off chip clock
- On-chip row pull-up devices
- 2 key roll-over
- Keybounce elimination with single capacitor
- Last key register at outputs
- 3-STATE output LPTTL compatible
- Wide supply range: 3V to 15V
- Low power consumption

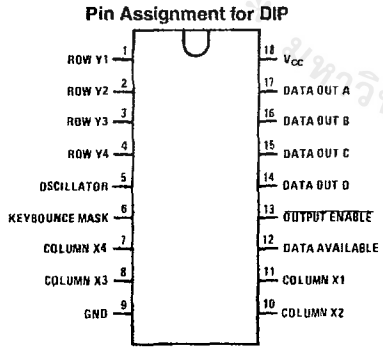
Ordering Code:

Order Number	Package Number	Package Description
MM74C922N	N18A	18-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74C922WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74C923WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74C923N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

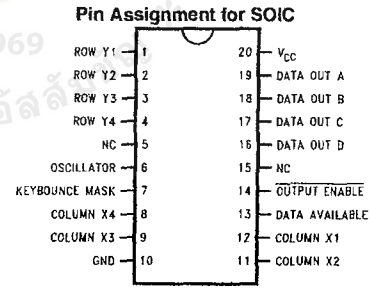
Connection Diagrams

Pin Assignment for DIP



Top View
MM94C922

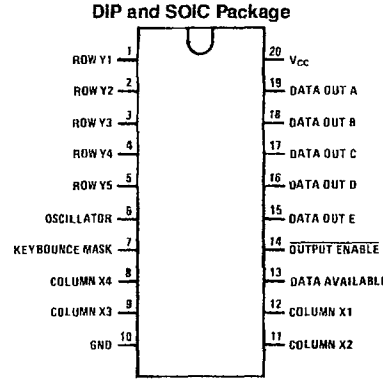
Pin Assignment for SOIC



Top View
MM74C922

Connection Diagrams (Continued)

Pin Assignment for DIP and SOIC Package



Top View
MM74C923

Truth Tables

(Pins 0 through 11)

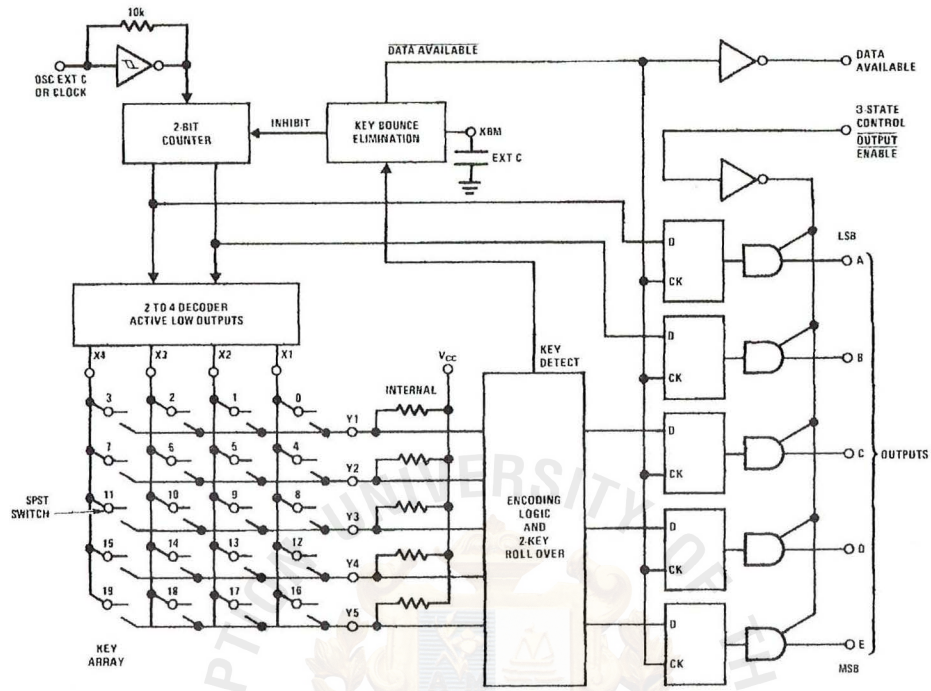
Switch Position		0 Y1,X1	1 Y1,X2	2 Y1,X3	3 Y1,X4	4 Y2,X1	5 Y2,X2	6 Y2,X3	7 Y2,X4	8 Y3,X1	9 Y3,X2	10 Y3,X3	11 Y3,X4
D													
A	A	0	1	0	1	0	1	0	1	0	1	0	1
T	B	0	0	1	1	0	0	1	1	0	0	1	1
A	C	0	0	0	0	1	1	1	1	0	0	0	0
O	D	0	0	0	0	0	0	0	0	1	1	1	1
U	E (Note 1)	0	0	0	0	0	0	0	0	0	0	0	0
T													

(Pins 12 through 19)

Switch Position		12 Y4,X1	13 Y4,X2	14 Y4,X3	15 Y4,X4	16 Y5(Note 1), X1	17 Y5 (Note 1), X2	18 Y5 (Note 1), X3	19 Y5 (Note 1), X4
D									
A	A	0	1	0	1	0	1	0	1
T	B	0	0	1	1	0	0	1	1
A	C	1	1	1	1	0	0	0	0
O	D	1	1	1	1	0	0	0	0
U	E (Note 1)	0	0	0	0	1	1	1	1
T									

Note 1: Omit for MM74C922

Block Diagram



Absolute Maximum Ratings (Note 2)

Voltage at Any Pin	V_{CC} − 0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM74C922, MM74C923	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
V_{CC}	18V
Lead Temperature	
(Soldering, 10 seconds)	260°C

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
V_{T+}	Positive-Going Threshold Voltage at Osc and KBM Inputs	V_{CC} = 5V, I_{IN} ≥ 0.7 mA	3.0	3.6	4.3	V
		V_{CC} = 10V, I_{IN} ≥ 1.4 mA	6.0	6.8	8.6	V
		V_{CC} = 15V, I_{IN} ≥ 2.1 mA	9.0	10	12.9	V
V_{T-}	Negative-Going Threshold Voltage at Osc and KBM Inputs	V_{CC} = 5V, I_{IN} ≥ 0.7 mA	0.7	1.4	2.0	V
		V_{CC} = 10V, I_{IN} ≥ 1.4 mA	1.4	3.2	4.0	V
		V_{CC} = 15V, I_{IN} ≥ 2.1 mA	2.1	5	6.0	V
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	V_{CC} = 5V	3.5	4.5		V
		V_{CC} = 10V	8.0	9		V
		V_{CC} = 15V	12.5	13.5		V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	V_{CC} = 5V		0.5	1.5	V
		V_{CC} = 10V		1	2	V
		V_{CC} = 15V		1.5	2.5	V
I_{rp}	Row Pull-Up Current at Y1, Y2, Y3, Y4 and Y5 Inputs	V_{CC} = 5V, V_{IN} = 0.1 V_{CC}		−2	−5	μA
		V_{CC} = 10V		−10	−20	μA
		V_{CC} = 15V		−22	−45	μA
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = −10 μA	4.5			V
		V_{CC} = 10V, I_O = −10 μA	9			V
		V_{CC} = 15V, I_O = −10 μA	13.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = 10 μA			0.5	V
		V_{CC} = 10V, I_O = 10 μA			1	V
		V_{CC} = 15V, I_O = 10 μA			1.5	V
R_{on}	Column "ON" Resistance at X1, X2, X3 and X4 Outputs	V_{CC} = 5V, V_O = 0.5V		500	1400	Ω
		V_{CC} = 10V, V_O = 1V		300	700	Ω
		V_{CC} = 15V, V_O = 1.5V		200	500	Ω
I_{CC}	Supply Current Osc at 0V, (one Y low)	V_{CC} = 5V		0.55	1.1	mA
		V_{CC} = 10V		1.1	1.9	mA
		V_{CC} = 15V		1.7	2.6	mA
$I_{IN(1)}$	Logical "1" Input Current at $\overline{\text{Output Enable}}$	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current at $\overline{\text{Output Enable}}$	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Except Osc and KBM Inputs	V_{CC} = 4.75V	V_{CC} − 1.5			V
$V_{IN(0)}$	Except Osc and KBM Inputs	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O = −360 μA, V_{CC} = 4.75V, I_O = −360 μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = −360 μA, V_{CC} = 4.75V, I_O = −360 μA			0.4	V

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8	16		mA

AC Electrical Characteristics (Note 3)

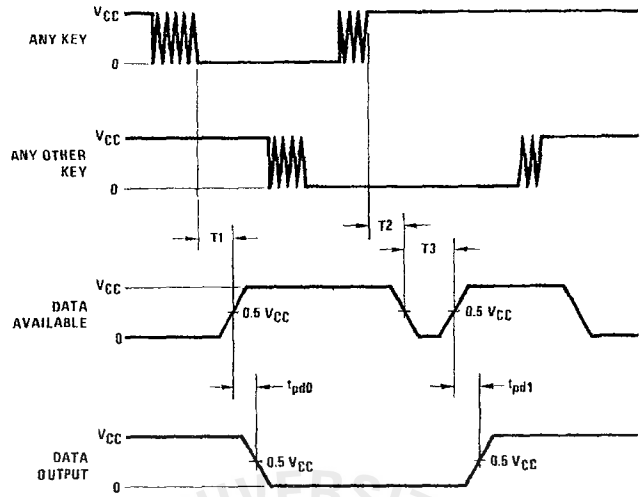
T_A = 25°C, C_L = 50 pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "0" or Logical "1" from D.A.	C_L = 50 pF (Figure 1)				
		V_{CC} = 5V		60	150	ns
		V_{CC} = 10V		35	80	ns
		V_{CC} = 15V		25	60	ns
t_{0H}, t_{1H}	Propagation Delay Time from Logical "0" or Logical "1" into High Impedance State	R_L = 10k, C_L = 10 pF (Figure 2)				
		V_{CC} = 5V, R_L = 10k		80	200	ns
		V_{CC} = 10V, C_L = 10 pF		65	150	ns
		V_{CC} = 15V		50	110	ns
t_{H0}, t_{H1}	Propagation Delay Time from High Impedance State to a Logical "0" or Logical "1"	R_L = 10k, C_L = 50 pF (Figure 2)				
		V_{CC} = 5V, R_L = 10k		100	250	ns
		V_{CC} = 10V, C_L = 50 pF		55	125	ns
		V_{CC} = 15V		40	90	ns
C_{IN}	Input Capacitance	Any Input (Note 4)		5	7.5	pF
C_{OUT}	3-STATE Output Capacitance	Any Output (Note 4)		10		pF

Note 3: AC Parameters are guaranteed by DC correlated testing.

Note 4: Capacitance is guaranteed by periodic testing.

Switching Time Waveforms



T1 = T2 = RC, T3 = 0.7 RC, where R = 10k and C is external capacitor at KBM input.

FIGURE 1.

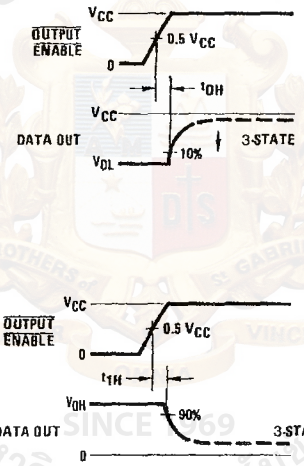
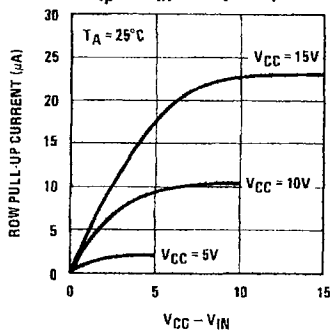


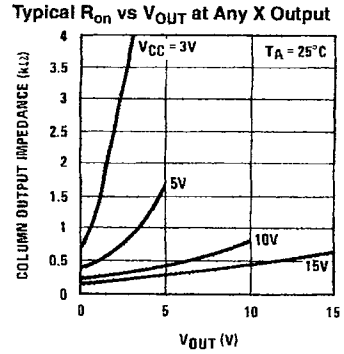
FIGURE 2.

Typical Performance Characteristics

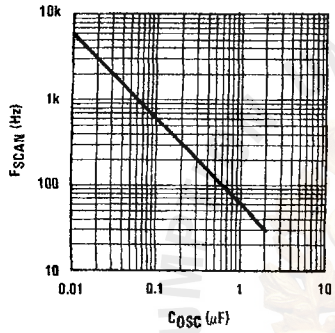
Typical I_{rp} vs V_{IN} at Any Y Input



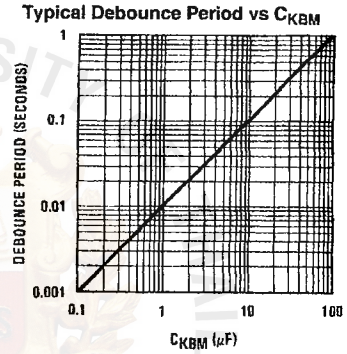
Typical R_{on} vs V_{OUT} at Any X Output



Typical F_{SCAN} vs C_{OSC}

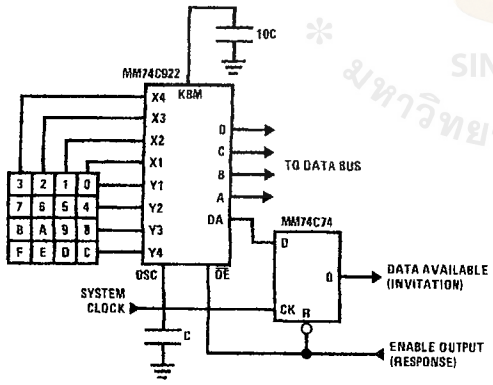


Typical Debounce Period vs C_{KBM}



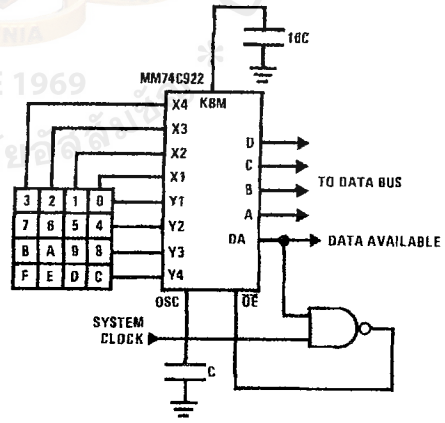
Typical Applications

Synchronous Handshake (MM74C922)



The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz

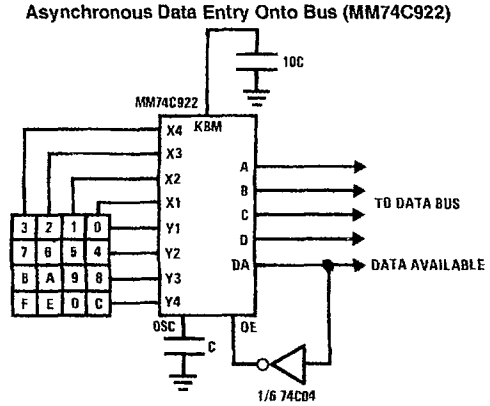
Synchronous Data Entry Onto Bus (MM74C922)



Outputs are enabled when valid entry is made and go into 3-STATE when key is released.

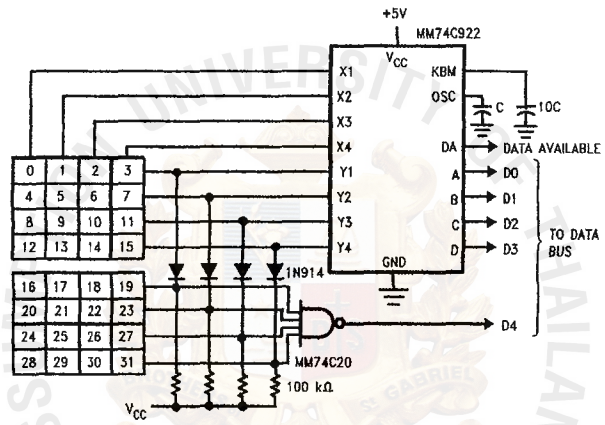
The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz

Asynchronous Data Entry Onto Bus (MM74C922)



Outputs are in 3-STATE until key is pressed, then data is placed on bus. When key is released, outputs return to 3-STATE.

Expansion to 32 Key Encoder (MM74C922)



Theory of Operation

The MM74C922/MM74C923 Keyboard Encoders implement all the logic necessary to interface a 16 or 20 SPST key switch matrix to a digital system. The encoder will convert a key switch closer to a 4(MM74C922) or 5(MM74C923) bit nibble. The designer can control both the keyboard scan rate and the key debounce period by altering the oscillator capacitor, C_{OSE}, and the key bounce mask capacitor, C_{MSK}. Thus, the MM74C922/MM74C923's performance can be optimized for many keyboards.

The keyboard encoders connect to a switch matrix that is 4 rows by 4 columns (MM74C922) or 5 rows by 4 columns (MM74C923). When no keys are depressed, the row inputs are pulled high by internal pull-ups and the column outputs sequentially output a logic "0". These outputs are open drain and are therefore low for 25% of the time and otherwise off. The column scan rate is controlled by the oscillator input, which consists of a Schmitt trigger oscillator, a 2-bit counter, and a 2–4-bit decoder.

When a key is depressed, key 0, for example, nothing will happen when the X1 input is off, since Y1 will remain high. When the X1 column is scanned, X1 goes low and Y1 will go low. This disables the counter and keeps X1 low. Y1 going low also initiates the key bounce circuit timing and locks out the other Y inputs. The key code to be output is a combination of the frozen counter value and the decoded Y inputs. Once the key bounce circuit times out, the data is latched, and the Data Available (DAV) output goes high.

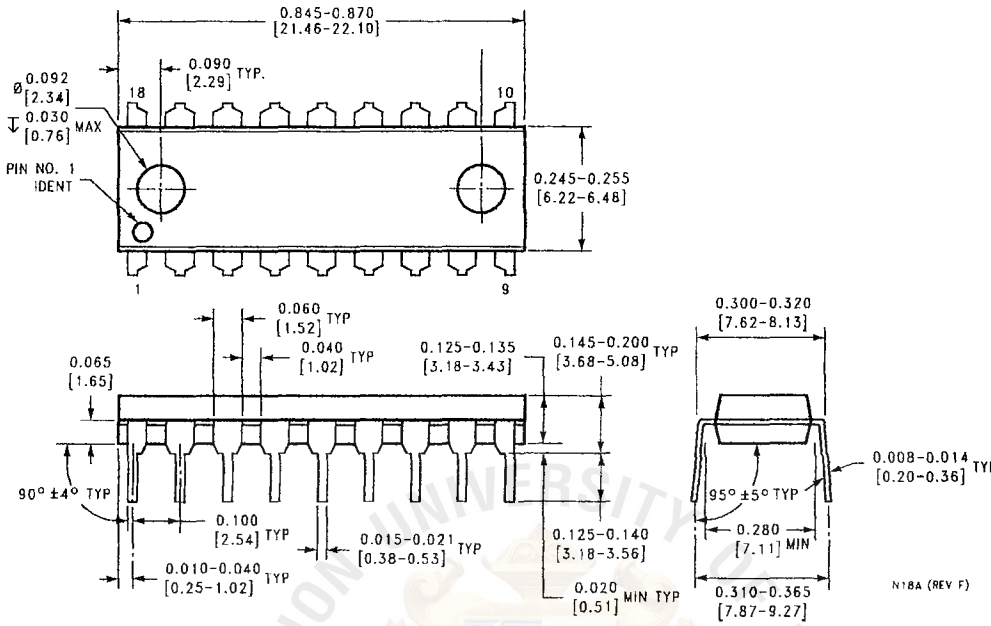
If, during the key closure the switch bounces, Y1 input will go high again, restarting the scan and resetting the key bounce circuitry. The key may bounce several times, but as soon as the switch stays low for a debounce period, the closure is assumed valid and the data is latched.

A key may also bounce when it is released. To ensure that the encoder does not recognize this bounce as another key closure, the debounce circuit must time out before another closure is recognized.

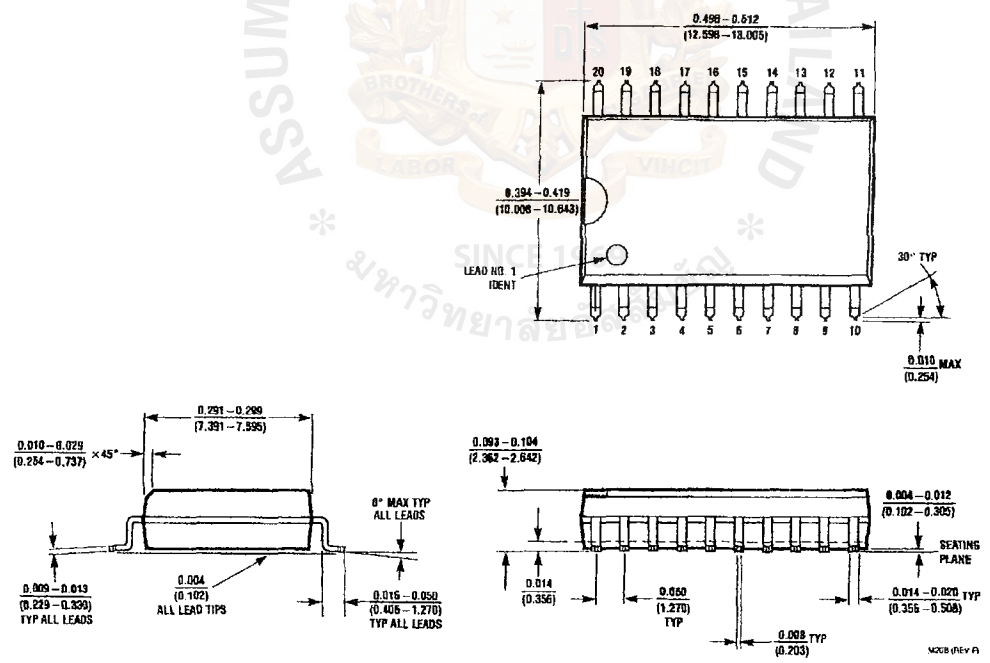
The two-key roll-over feature can be illustrated by assuming a key is depressed, and then a second key is depressed. Since all scanning has stopped, and all other Y inputs are disabled, the second key is not recognized until the first key is lifted and the key bounce circuitry has reset.

The output latches feed 3-STATE, which is enabled when the Output Enable ($\overline{OE}$) input is taken low.

Physical Dimensions inches (millimeters) unless otherwise noted

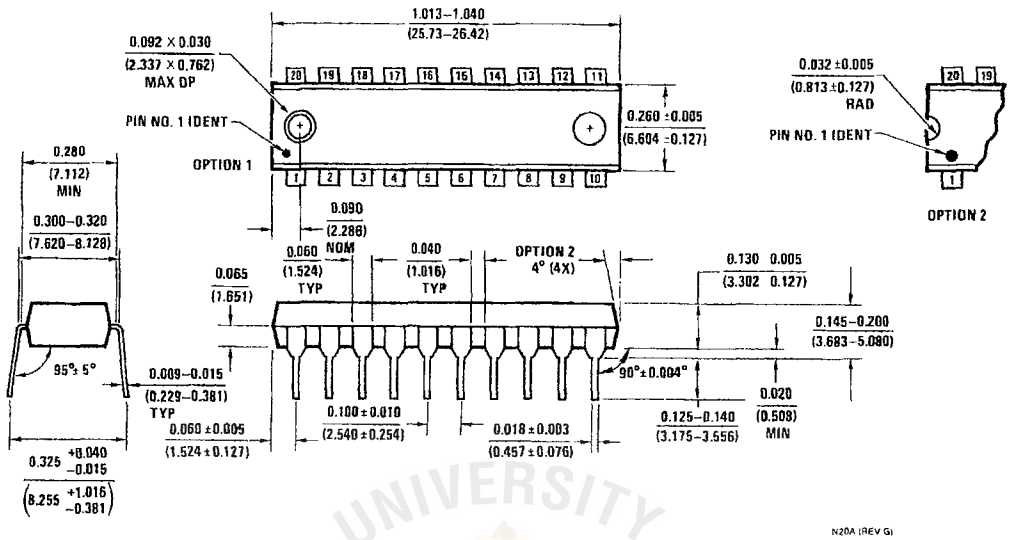


18-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N18A



20-Lead Plastic Small Outline I.C. Package (M)
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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MC34114

Specifications and Applications Information

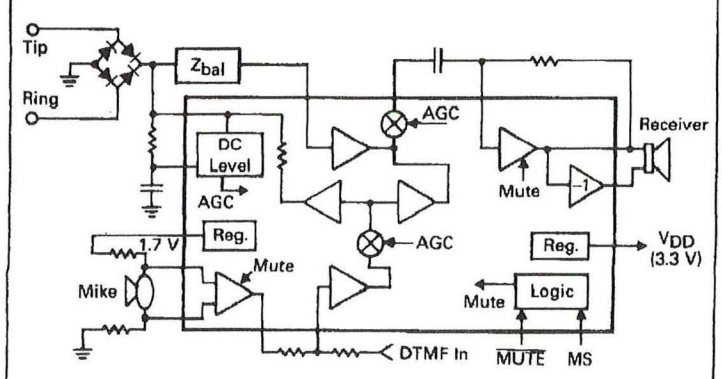
TELEPHONE SPEECH NETWORK WITH DIALER INTERFACE

The MC34114 is a monolithic integrated telephone speech network designed to replace the bulky magnetic hybrid circuit of a telephone set. The MC34114 incorporates the necessary functions of transmit amplification, receive amplification, and sidetone control, each with externally adjustable gain. Loop length equalization varies the gains based on loop current. The microphone amplifier has a balanced, differential input stage designed to reduce RFI problems. A $\overline{\text{MUTE}}$ input mutes the microphone and receive amplifiers during dialing. A regulated output voltage is provided for biasing of the microphone, and a separate output voltage powers an external dialer, microprocessor, or other circuitry. The MC34114 is designed to operate at a minimum of 1.2 volts, making party line operation possible.

A circuit using the MC34114 can be made to comply with Bell Telephone, British Telecom (BT), and NTT (Nippon Telegraph & Telephone) standards. It is available in a standard 18-pin DIP, and a 20-pin SOIC (surface mount) package.

- Operation Down to 1.2 Volts
- Externally Adjustable Transmit, Receive, and Sidetone Gains
- Differential Microphone Amplifier Input Minimizes RFI Susceptibility
- Transmit, Receive, and Sidetone Equalization on Both Voice and DTMF Signals
- Regulated 1.7 Volts Output for Biasing Microphone
- Regulated 3.3 Volts Output for Powering External Dialer or MPU
- Microphone and Receive Amplifiers Muted During Dialing
- Differential Receive Amplifier Output Eliminates Coupling Capacitor
- Operates with Receiver Impedances of 50 Ohms and Higher
- Complies with NTT, Bell Telephone and BT Standards

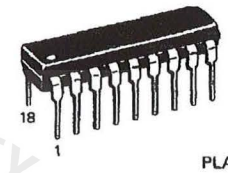
SIMPLIFIED BLOCK DIAGRAM



TELEPHONE SPEECH NETWORK WITH DIALER INTERFACE

SILICON MONOLITHIC INTEGRATED CIRCUIT

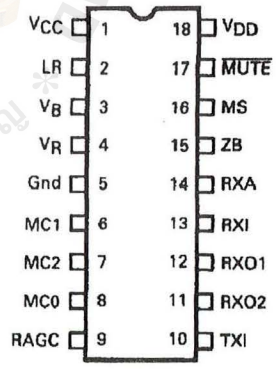
2



P SUFFIX
PLASTIC PACKAGE
CASE 707

DW SUFFIX
PLASTIC PACKAGE
CASE 751D

PIN CONNECTIONS
(Top View)
(DIP Package)



ORDERING INFORMATION

Package	Part No.
18-Pin Plastic DIP	MC34114P
20-Pin Surface Mount	MC34114DW

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Units
V_{CC} Supply Voltage	−1.0, +12	Vdc
Voltage at V_{DD} (Externally Applied, V_{CC} = 0)	−1.0, +6.0	Vdc
Voltage at $\overline{MUTE}$, MS (V_{CC} > 1.5 Volts)	−1.0, V_{DD}+0.5	Vdc
Voltage at $\overline{MUTE}$, MS (V_{CC} = 0)	−1.0, +6.0	Vdc
Voltage at RAGC (0 < V_{CC} < 12 Volts)	−1.0, +6.0	Vdc
Current through V_{CC}, LR	130	mA
Current into Z_B (Pin 15)	3.0	mA
Storage Temperature	−65, +150	°C

"Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices can be operated at these limits. The "Recommended Operating Conditions" provides conditions for actual device operation.

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RECOMMENDED OPERATING LIMITS

Parameter	Min	Typ	Max	Units
V_{CC} Voltage (Speech, Pulse Mode)	+1.2	—	+10.5	Vdc
(Tone Dialing Mode)	+3.3	—	+10.5	
Loop Current (into V_{CC}) (Speech, Pulse Mode)	4.0	—	120	mA
(Tone Dialing Mode)	15	—	120	
Receiver Impedance	50	—	—	Ω
Voltage at $\overline{MUTE}$, MS (V_{CC} > 1.5 Volts)	0	—	V_{DD}	Vdc
R1 (Resistor from V_{CC} to V_B)	100	—	1800	Ω
Ambient Temperature	−20	—	+70	°C

All limits are not necessarily functional concurrently.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, See Figure 1)

Parameter	Symbol	Min	Typ	Max	Units
SUPPLY CURRENT					
Supply Current into V_{CC} (Pin 2 open, R12 = 25 k, V_{DD} unloaded)					mA
Speech Mode (Figure 2) V_{CC} = 1.2 Volts	I_{ccsp}	4.0	5.0	5.5	
V_{CC} = 3.5 Volts		9.0	11	12	
V_{CC} = 8.0 Volts		10	12	14	
V_{CC} = 10.5 Volts		—	13	—	
Tone Mode (Figure 4) V_{CC} = 3.3 Volts	I_{cct}	—	14	—	
V_{CC} = 8.0 Volts		—	16	—	
V_{CC} = 10 Volts		—	18	—	
VOLTAGE REGULATORS					
V_R Voltage (I_R = 65 μA, V_{CC} = 2.5 V, Figure 5)	V_R	1.6	1.7	1.85	Vdc
Load Regulation (0 < I_R < 300 μA, V_{CC} = 2.5 V)		—	0.2	0.5	Vdc
Line Regulation (I_R = 65 μA, 2.5 < V_{CC} < 10.5 V)		−70	±20	+70	mVdc
V_{DD} Voltage (V_{CC} ≥ 3.8 V, I_{DD} = 0, Figure 6)	V_{DD}	3.1	3.3	3.7	Vdc
Line Regulation (I_{DD} = 0, 5.0 V < V_{CC} < 10.5 V)		−70	±30	+70	mVdc
Maximum Output Current (V_{CC} = 3.8 V, V_{DD} ≥ 3.0 V)	I_{DDMAX}				mA
Speech Mode		0.8	1.0	—	
Pulse, Tone Mode		2.2	2.5	—	
Input Leakage Current (V_{CC} = 0, 3.3 Volts applied to V_{DD})	I_{lkg}				μA
$\overline{Mute}$ open or at V_{DD}		—	0.02	0.5	
$\overline{Mute}$ = 0 Volts		—	180	—	

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C, See Figure 1)

Parameter	Symbol	Min	Typ	Max	Units
MICROPHONE AMPLIFIER					
Gain ($\overline{Mute}$ = V_{DD})	G_{MIC}	28	30	32	dB
Input Common Mode Rejection Ratio (1.0 kHz)	CMRR	20	26	—	dB
Input Impedance (Each Input)	R_{INMIC}	14	20	27	kΩ
MCO DC Bias Voltage (V_{CC} > 3.4 V, $\overline{Mute}$ = Hi) (V_{CC} = 1.2 V, $\overline{Mute}$ = Hi) ($\overline{Mute}$ = 0 V)	V_{MCODC}	0.85 0.6 —	1.1 0.71 0.08	1.25 0.93 —	Vdc
MCO Max Voltage Swing (THD = 5%, V_{CC} > 2.7 V) (THD = 5%, V_{CC} = 1.2 V)	V_{MCOAC}	— —	2.0 500	— —	Vp-p mVp-p
MCO Output Impedance	Z_{MCO}	—	270	—	Ω
MCO Output Current Capability (THD = 5%)	I_{MCO}	—	160	—	μA
Gain Reduction when Muted ($\overline{Mute}$ = 0 Volts, f = 1.0 kHz)	G_{MUT}	55	70	—	dB
RECEIVE AMPLIFIER					
RXI Bias Current (Mute = Hi)	I_{IBR}	—	50	—	nA
RXO1, RXO2 Bias Voltage (V_{CC} = 1.2 V) (V_{CC} > 3.0. V)	R_{XDC}	580 585	630 650	695 720	mVdc
RXO1–RXO2 Offset Voltage (V_{CC} > 3.0 V)	R_{XVOS}	−35	0	+35	mVdc
RXO1–RXO2 Max Voltage Swing (Figure 9) (THD = 5%, Receiver = ∞) (THD = 5%, Receiver = 150 Ω)	V_{RXAC}	— —	2.2 800	— —	Vp-p mVp-p
Internal Feedback Resistor (for muting)	R_{FINT}	—	1.0	—	kΩ
RXO1 & RXO2 Source Current	I_{RX}	2.6	3.2	3.5	mA
INTERNAL CURRENT AMPLIFIERS					
TXI Input Impedance	R_{TXI}	0.85	1.0	1.15	kΩ
ZB Input Impedance	R_{ZB}	—	500	—	Ω
RXA Output Impedance	R_{RXA}	—	10	—	kΩ
AC Current Gain					A/A
TXI to V_{CC} (V_{RAGC} = 0 V) TXI to V_{CC} (V_{RAGC} = 1.3 V)	G_{TX}	— —	100 50	— —	
ZB to RXA (V_{RAGC} = 0 V, RXA = AC Gnd) ZB to RXA (V_{RAGC} = 1.3 V, RXA = AC Gnd)	G_{ZB}	— —	0.5 0.25	— —	
TXI to RXA (V_{RAGC} = 0 V, RXA = AC Gnd) TXI to RXA (V_{RAGC} = 1.3 V, RXA = AC Gnd)	G_{STA}	— —	1.22 0.61	— —	
DC INTERFACE					
LR Level Shift (V_{CC}–V_{LR})					Vdc
(I_{LOOP} = 20 mA, $\overline{Mute}$ = V_{DD}) (I_{LOOP} = 80 mA, $\overline{Mute}$ = V_{DD})	ΔV_{LRS}	— —	2.8 3.5	— —	
(I_{LOOP} = 20 mA, $\overline{Mute}$ & MS = 0 V) (I_{LOOP} = 80 mA, $\overline{Mute}$ & MS = 0 V)	ΔV_{LRT}	— —	3.8 5.0	— —	
V_{CC} Boost (I_{LOOP} = 20 mA, $\overline{Mute}$ & MS switched from Hi to Lo, R1 = 620 Ω)	ΔV_{LRB}	0.7	1.0	1.2	Vdc
RAGC Current (V_{RAGC} = 0 V) (V_{RAGC} = 1.0 V)	I_{RAGC}	— —	−40 −12	— —	μA

2

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C, See Figure 1)

Parameter	Symbol	Min	Typ	Max	Units
LOGIC INPUTS					
$\overline{MUTE}$ Input Impedance (V_{CC} > 1.2 V)	R_{MUT}	—	60	—	kΩ
(V_{CC} = 0 V, 0 < $\overline{Mute}$ < 6.0 V)		—	>60	—	MΩ
Input Low Voltage	V_{ILMT}	0	—	1.0	Vdc
Input High Voltage	V_{IHMT}	V_{DD} − 0.5	—	V_{DD}	Vdc
Holdover (Delay for Receive amplifier to return to full gain after Pin 17 switches from 0 to V_{DD})	T_{MUT}	8.0	11	25	mSec
MS Input Impedance (V_{CC} > 1.2 V)	R_{MS}	—	60	—	kΩ
(V_{CC} = 0 V, $\overline{Mute}$ = open or V_{DD})		—	>50	—	MΩ
(V_{CC} = 0, $\overline{Mute}$ = 0)		—	4.0	—	kΩ
Input Low Voltage	V_{ILMS}	0	—	0.3	Vdc
Input High Voltage	V_{IHMS}	2.0	—	V_{DD}	Vdc

SYSTEM SPECIFICATIONS (f = 1.0 kHz unless noted, T_A = 25°C, Refer to Figure 1)

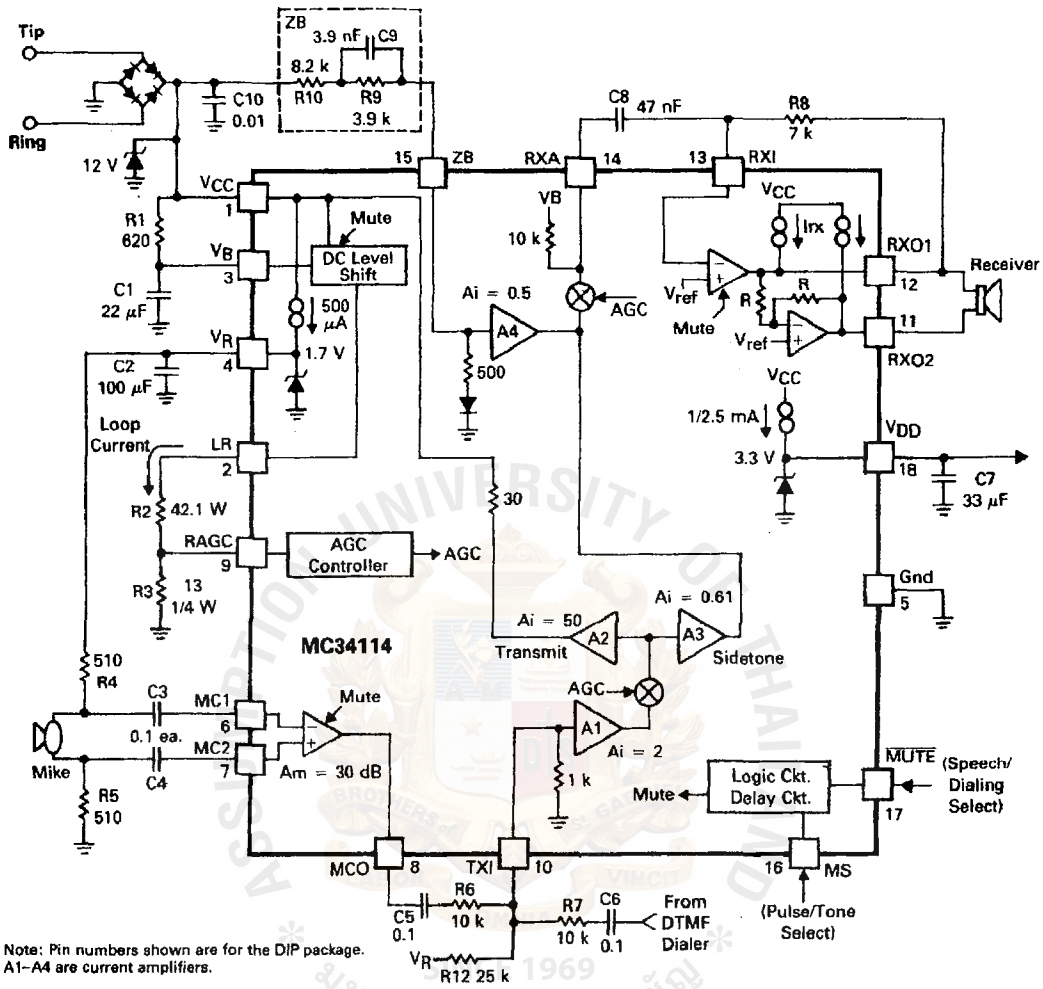
Parameter	Symbol	Min	Typ	Max	Units
LINE INTERFACE					
V_{CC} DC Voltage (Pin 1)	V_{CC}				Vdc
Bell Telephone Standard and NTT Specs. (R2 = 43 Ω, R3 = 13 Ω)					
Speech Mode I_{LOOP} = 10 mA		1.7	2.0	2.3	
I_{LOOP} = 20 mA		3.0	3.4	3.7	
I_{LOOP} = 30 mA		3.5	4.1	4.5	
I_{LOOP} = 120 mA		8.5	9.9	10.5	
Tone Mode I_{LOOP} = 20 mA		3.9	4.1	4.3	
I_{LOOP} = 30 mA		4.5	5.1	5.5	
British Telecom Standard (R2 = 43 Ω + 2.5 V Zener, R3 = 13 Ω)					
Speech Mode I_{LOOP} = 10 mA		—	4.3	—	
I_{LOOP} = 20 mA		—	5.9	—	
I_{LOOP} = 30 mA		—	6.9	—	
I_{LOOP} = 70 mA		—	10	—	
AC Terminating Impedance (I_{LOOP} = 20 mA, Figure 11)	Z_{AC}	500	600	700	Ω
RECEIVE PATH					
Gain (V_{CC} to RXO1–RXO2, Figures 14, 15)	G_{RX}				dB
I_{LOOP} = 20 mA		−7.2	−6.1	−5.0	
I_{LOOP} = 100 mA		−13.5	−11	−9.5	
ΔGain (G_{RX} @ 100 mA versus 20 mA)	ΔG_{RX}	−7.5	−6.0	−4.5	dB
Muted Gain ($\overline{Mute}$ = Logic 0, I_{LOOP} = 20 mA)	G_{RXM}	—	−22	−20	dB
Distortion (at RXO1–RXO2, V_{CC} = 250 mVrms)	THD_R				%
f = 300 Hz		—	0.3	—	
f = 1.0 kHz		—	0.2	2.0	
f = 3.4 kHz		—	0.02	—	
Output Noise Across RXO1–RXO2 (@ 1.0 kHz)	N_{RXO}	—	4.0	—	μVrms
TRANSMIT PATH					
Gain (MC1–MC2 to V_{CC}, Figures 12, 13)	G_{TX}				dB
I_{LOOP} = 20 mA		36	38.5	40.5	
I_{LOOP} = 100 mA		29	32.5	35.5	
ΔGain (G_{TX} @ 100 mA versus 20 mA)	ΔG_{TX}	−7.5	−6.0	−4.5	dB
Max V_{CC} Voltage Swing (THD = 5%, Figure 8)	VTX_{MAX}				Vp-p
I_{LOOP} = 20 mA		—	3.0	—	
I_{LOOP} = 100 mA		—	2.3	—	
Gain Reduction when muted (MC1–MC2 to V_{CC}, $\overline{Mute}$ = 0 V)	G_{TXM}	—	68	—	dB
Distortion (0 dBm @ V_{CC})	THD_T				%
f = 300 Hz		—	0.5	—	
f = 1.0 kHz		—	1.5	3.0	
f = 3.4 kHz		—	1.3	—	
Output Noise at V_{CC} (@ 1.0 kHz)	N_{TXO}	—	17	—	μVrms
SIDETONE					
Sidetone Gain (Gain from V_{CC} to RXO1–RXO2 with signal applied to MC1/MC2, I_{LOOP} = 20 mA)	G_{ST}	—	−27	−22	dB

PIN DESCRIPTIONS

Symbol	Pin Number (SOIC)	Pin Number (DIP)	Description
V_{CC}	1	1	Power supply pin for the IC. Supply voltage is derived from loop current. Transmit amp output operates on this pin.
LR	2	2	Resistors R2+R3 at this pin set the DC characteristics of the circuit. The majority of the loop current flows through these resistors. Other components may be used to produce required DC characteristics for individual regulatory agencies.
V_B	3	3	A resistor or appropriate network (R1) connected from this pin to V_{CC} sets the AC terminating impedance (return loss spec).
V_R	4	4	A 1.7 volt regulated output which can be used to bias the microphone. Additionally, this voltage powers a portion of the internal circuitry. Can nominally supply 300–500 μA.
GND	5	5	Ground pin for the entire IC. Normally this is not connected to, nor to be confused with earth ground.
MC1	6	6	Inverting differential input to the microphone amplifier. Input impedance is typically 20 kΩ.
MC2	7	7	Non-inverting differential input to the microphone amplifier. Input impedance is typically 20 kΩ.
MCO	8	8	Microphone amplifier output. Amplifier's gain is fixed at 30 dB.
RAGC	10	9	Loop current sensing input. The voltage at this pin, determined by the loop current and R3, operates the loop length equalization circuit.
TXI	11	10	Input to the transmit amplifier from the microphone amplifier, DTMF source, and other sources. Input impedance ≈ 1.0 kΩ.
RXO2	12	11	Receive amplifier non-inverting differential output. Current capability to the receiver is typically set at ±3.0 mA peak.
RXO1	14	12	Receive amplifier inverting differential output. Current capability to the receiver is typically ±3.0 mA peak. Gain is set by R8.
RXI	15	13	Summing input to the receive amplifier. This pin is an AC virtual ground.
RXA	16	14	Summed outputs of the receive current amplifier, sidetone amplifier, and an AGC point. Normally connected to the receive amplifier input (RXI) through a coupling capacitor.
ZB	17	15	Input to the receive current amplifier. A balance network (ZB) is connected between this pin and V_{CC}. The network affects the receive level and sidetone performance. Input impedance is ≈500 Ω in series with a diode.
MS	18	16	Mode Select Input. A logic "1" sets the IC for pulse dialing. A logic "0" sets the IC for tone (DTMF) dialing. Effective only if $\overline{MUTE}$ is at a logic "0". Input impedance is ≈ 60 kΩ.
$\overline{MUTE}$	19	17	Mute input. A logic "1" sets normal speech mode. A logic "0" mutes the microphone and receive amplifiers and allows MS to be functional. Input impedance is ≈60 kΩ referenced to V_{DD}. An internal fixed delay of 11 mSec minimizes clicks in the receiver when returning to the speech mode.
V_{DD}	20	18	A regulated 3.3 volt output for an external dialer. Output source current capability is 1.0 mA in speech mode, 2.5 mA in tone dialing mode.

2

FIGURE 1 — BLOCK DIAGRAM AND TEST CIRCUIT



Note: Pin numbers shown are for the DIP package.
A1–A4 are current amplifiers.

FIGURE 2 — I_{CC} versus V_{CC} (SPEECH MODE)

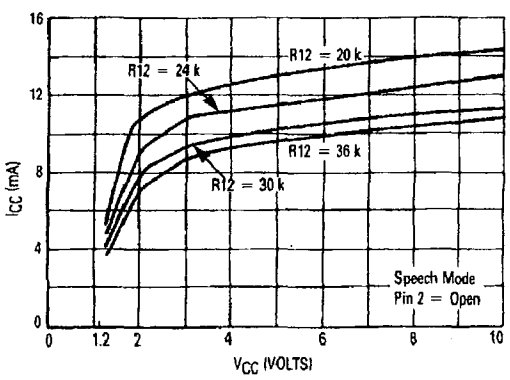
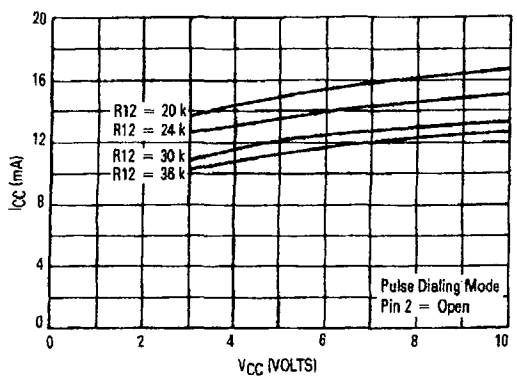


FIGURE 3 — I_{CC} versus V_{CC} (PULSE DIALING MODE)



May 1999

LM567/LM567C Tone Decoder

General Description

The LM567 and LM567C are general purpose tone decoders designed to provide a saturated transistor switch to ground when an input signal is present within the passband. The circuit consists of an I and Q detector driven by a voltage controlled oscillator which determines the center frequency of the decoder. External components are used to independently set center frequency, bandwidth and output delay.

Features

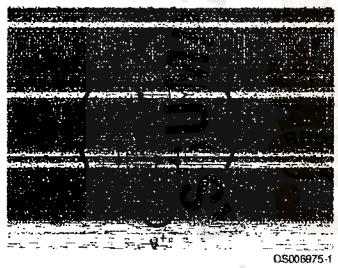
- 20 to 1 frequency range with an external resistor
- Logic compatible output with 100 mA current sinking capability
- Bandwidth adjustable from 0 to 14%
- High rejection of out of band signals and noise
- Immunity to false signals
- Highly stable center frequency
- Center frequency adjustable from 0.01 Hz to 500 kHz

Applications

- Touch tone decoding
- Precision oscillator
- Frequency monitoring and control
- Wide band FSK demodulation
- Ultrasonic controls
- Carrier current remote controls
- Communications paging decoders

Connection Diagrams

Metal Can Package



Top View
Order Number LM567H or LM567CH
See NS Package Number H08C

Dual-In-Line and Small Outline Packages

Top View
Order Number LM567CM
See NS Package Number M08A
Order Number LM567CN
See NS Package Number N08E

National Semiconductor

December 1991

TP5089 DTMF (TOUCH-TONE) Generator

General Description

The TP5089 is a low threshold voltage, field-implanted, metal gate CMOS integrated circuit. It interfaces directly to a standard telephone keypad and generates all dual tone multi-frequency pairs required in tone-dialing systems. The tone synthesizers are locked to an on-chip reference oscillator using an inexpensive 3.579545 MHz crystal for high tone accuracy. The crystal and an output load resistor are the only external components required for tone generation. A $\overline{\text{MUTE}}$ OUT logic signal, which changes state when any key is depressed, is also provided.

Features

- 3.5V–10V operation when generating tones
- 2V operation of keyscan and $\overline{\text{MUTE}}$ logic
- Static sensing of key closures or logic inputs
- On-chip 3.579545 MHz crystal-controlled oscillator
- Output amplitudes proportional to supply voltage
- High group pre-emphasis
- Low harmonic distortion
- Open emitter-follower low-impedance output
- $\overline{\text{SINGLE TONE INHIBIT}}$ pin

Block Diagram

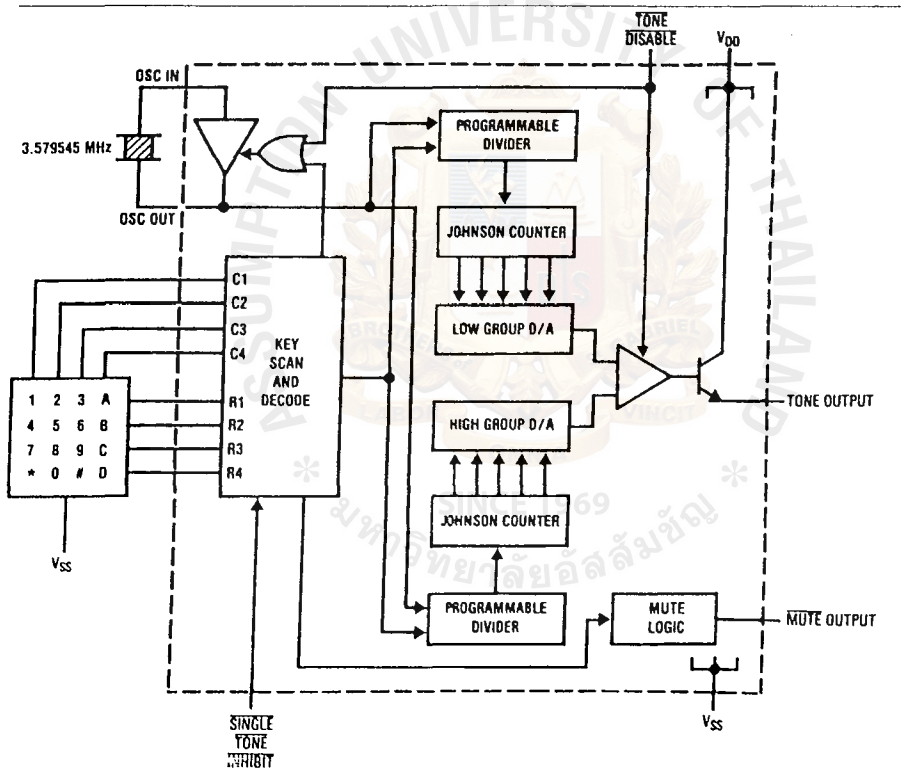


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FIGURE 1

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V_{DD} - V_{SS}$)	15V
Maximum Voltage at Any Pin	V_{DD} + 0.3V to V_{SS} − 0.3V
Operating Temperature	−30°C to +60°C
Storage Temperature	−55°C to + 150°C
Maximum Power Dissipation	500 mW

Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{DD} = 3.5V to 10V, T_A = 0°C to +60°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization.

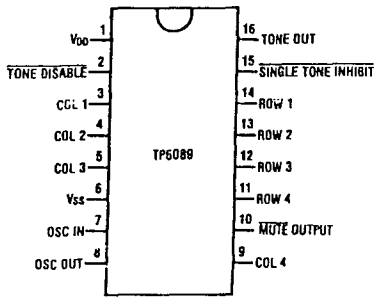
Parameter	Conditions	Min	Typ	Max	Units
Minimum Supply Voltage for Keysense and $\overline{\text{MUTE}}$ Logic Functions		2			V
Minimum Operating Voltage for generating tones		**3.5**			V
Operating Current Idle Generating Tones	Mute open $R_L = \infty$ V_{DD} = 3.5V		2 1.1	**25** **2.5**	μA mA
Input Resistors COLUMN and ROW (Pull-Up) $\overline{\text{SINGLE TONE INHIBIT}}$ (Pull-Down) $\overline{\text{TONE DISABLE}}$ (Pull-Up)		25 120	50		kΩ kΩ
Input Low Level				**0.2 V_{DD}**	V
Input High Level		**0.8 V_{DD}**			V
$\overline{\text{MUTE}}$ OUT Sink Current (COLUMN and ROW Active)	V_{DD} = 3.5V V_o = 0.5V	**0.4**			mA
$\overline{\text{MUTE}}$ Out Leakage Current	$V_o = V_{DD}$		1		μA
Output Amplitude Low Group	R_L = 240 Ω V_{DD} = 3.5V	**190**	250	**340**	mVrms
	R_L = 240Ω V_{DD} = 10V	**510**	700	**880**	mVrms
Output Amplitude High Group	R_L = 240Ω V_{DD} = 3.5V	**270**	340	**470**	mVrms
	R_L = 240Ω V_{DD} = 10V	**735**	955	**1265**	mVrms
Mean Output DC Offset	V_{DD} = 3.5V V_{DD} = 10V		1.3 4.6		V V
High Group Pre-Emphasis		**2.2**	2.7	**3.2**	dB
Dual Tone/Total Harmonic Distortion Ratio	V_{DD} = 4V, R_L = 240Ω 1 MHz Bandwidth		−23	**−22**	dB
Start-Up Time (to 90% Amplitude)			3	5	mS

Note 1: R_L is the external load resistor connected from TONE OUT to V_{SS}.

Note 2: Crystal specification: Parallel resonant 3.579545 MHz, $R_S \leq 150\ \Omega$, L = 100 mH, C_O = 5 pF, C_I = 0.02 pF.

Connection Diagram

Dual-In-Line Package



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Top View

Order Number TP5089N
See NS Package N16A

Pin Descriptions

Symbol	Description
V_{DD}	This is the positive voltage supply to the device, referenced to V_{SS}. The collector of the TONE OUT transistor is connected to this pin.
V_{SS}	This is the negative voltage supply. All voltages are referenced to this pin.
OSC IN, OSC OUT	All tone generation timing is derived from the on-chip oscillator circuit. A low cost 3.579545 MHz A-cut crystal (NTSC TV color-burst) is needed between pins 7 and 8. Load capacitors and a feedback resistor are included on-chip for good start-up and stability. The oscillator stops when column inputs are sensed with no valid input having been detected. The oscillator is also stopped when the $\overline{\text{TONE DISABLE}}$ input is pulled to logic low.
Row and Column Inputs	When no key is pushed, pull-up resistors are active on row and column inputs. A key closure is recognized when a single row and a single column are connected to V_{SS}, which starts the oscillator and initiates tone generation. Negative-true logic signals simulating key closures can also be used.
$\overline{\text{TONE DISABLE}}$ Input	The $\overline{\text{TONE DISABLE}}$ input has an internal pull-up resistor. When this input is open or at logic high, the normal tone output mode will occur. When $\overline{\text{TONE DISABLE}}$ input is at logic low, the device will be in the inactive mode, TONE OUT will be at an open circuit state.
$\overline{\text{MUTE}}$ Output	The $\overline{\text{MUTE}}$ output is an open-drain N-channel device that sinks current to V_{SS} with any key input and is open when no key input is sensed. The $\overline{\text{MUTE}}$ output will switch regardless of the state of the $\overline{\text{SINGLE TONE INHIBIT}}$ input.
$\overline{\text{SINGLE TONE INHIBIT}}$ Input	The $\overline{\text{SINGLE TONE INHIBIT}}$ input is used to inhibit the generation of other than valid tone pairs due to multiple row-column closures. It has a pull-down resistor to V_{SS}, and when left open or tied to V_{SS} any input condition that would normally result in a single tone will now result in no tone, with all other functions operating normally. When tied to V_{DD}, single or dual tones may be generated, see Table II.
TONE OUT	This output is the open emitter of an NPN transistor, the collector of which is connected to V_{DD}. When an external load resistor is connected from TONE OUT to V_{SS}, the output voltage on this pin is the sum of the high and low group sine-waves superimposed on a DC offset. When not generating tones, this output transistor is turned OFF to minimize the device idle current. Adjustment of the emitter load resistor results in variation of the mean DC current during tone generation, the sinewave signal current through the output transistor, and the output distortion. Increasing values of load resistance decrease both the signal current and distortion.

Functional Description

With no key inputs to the device the oscillator is inhibited, the output transistor is pulled OFF and device current consumption is reduced to a minimum. Key closures are sensed statically. Any key closure activates the $\overline{\text{MUTE}}$ output, starts the oscillator and sets the high group and low group programmable counters to the appropriate divide ratio. These counters sequence two ratioed-capacitor D/A converters through a series of 28 equal duration steps per sine-wave cycle. The two tones are summed by a mixer amplifier, with pre-emphasis applied to the high group tone. The output is an NPN emitter-follower requiring the addition of an external load resistor to V_{SS}. This resistor facilitates adjustment of the signal current flowing from V_{DD} through the output transistor.

The amplitude of the output tones is directly proportional to the device supply voltage.

Functional Description (Continued)

TABLE I. Output Frequency Accuracy

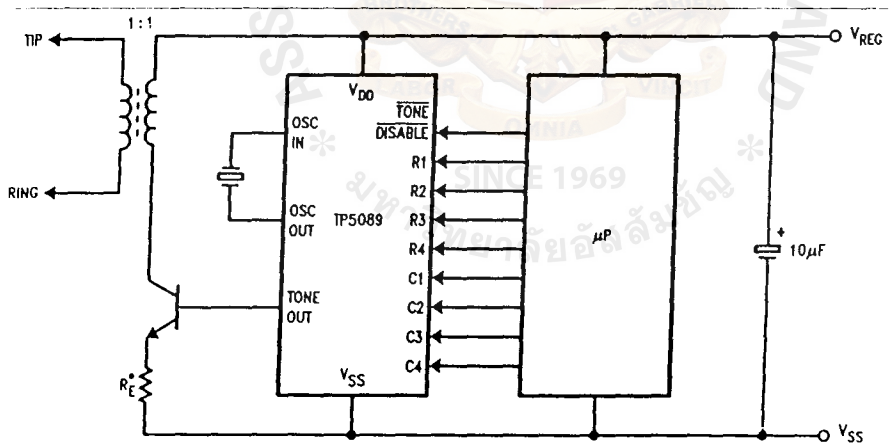
Tone Group	Valid Input	Standard DTMF (Hz)	Tone Output Frequency	% Deviation from Standard
Low Group f_L	R1	697	694.8	−0.32
	R2	770	770.1	+0.02
	R3	852	852.4	+0.03
	R4	941	940.0	−0.11
High Group f_H	C1	1209	1206.0	−0.24
	C2	1336	1331.7	−0.32
	C3	1477	1486.5	+0.64
	C4	1633	1639.0	+0.37

TABLE II. Functional Truth Table

$\overline{\text{SINGLE TONE INHIBIT}}$	$\overline{\text{TONE DISABLE}}$	ROW	COLUMN	TONE OUT		MUTE
				Low	High	
X	0	O/C	O/C	0V	0V	O/C
X	X	O/C	O/C	0V	0V	O/C
X	0	One	One	V_{OS}	V_{OS}	O
X	1	One	One	f_L	f_H	O
1	1	2 or More	One	—	f_H	O
1	1	One	2 or More	f_L	—	O
1	1	2 or More	2 or More	V_{OS}	V_{OS}	O
0	1	2 or More	One	V_{OS}	V_{OS}	O
0	1	One	2 or More	V_{OS}	V_{OS}	O
0	1	2 or More	2 or More	V_{OS}	V_{OS}	O

Note 1: X is don't care state.

Note 2: V_{OS} is the output offset voltage.



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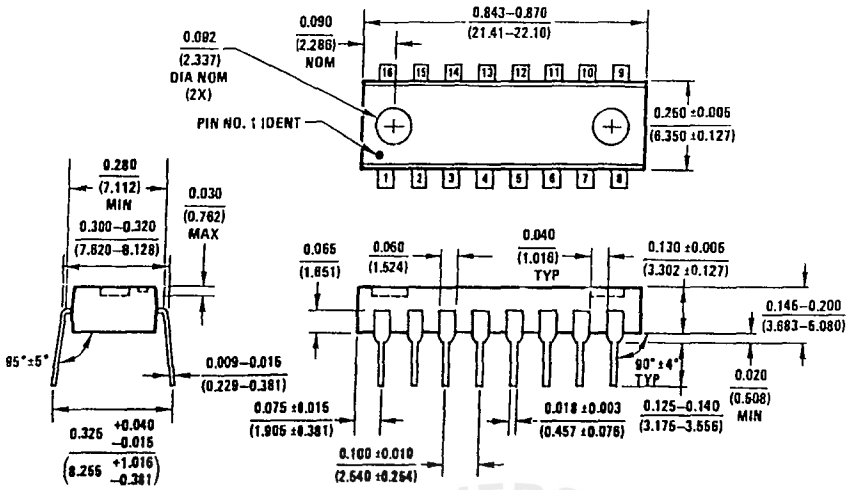
*Adjust R_E for desired tone amplitude.

FIGURE 2. Typical Application

Physical Dimensions inches (millimeters)

Lit. # 113986



Molded Dual-In-Line Package (N)
Order Number TP5089N
NS Package N16A

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ISD2500 Series

Single-Chip Voice Record/Playback Devices
32-, 40-*, 48-*, 64-*,* 60-, 75-, 90-, and 120-Second Durations

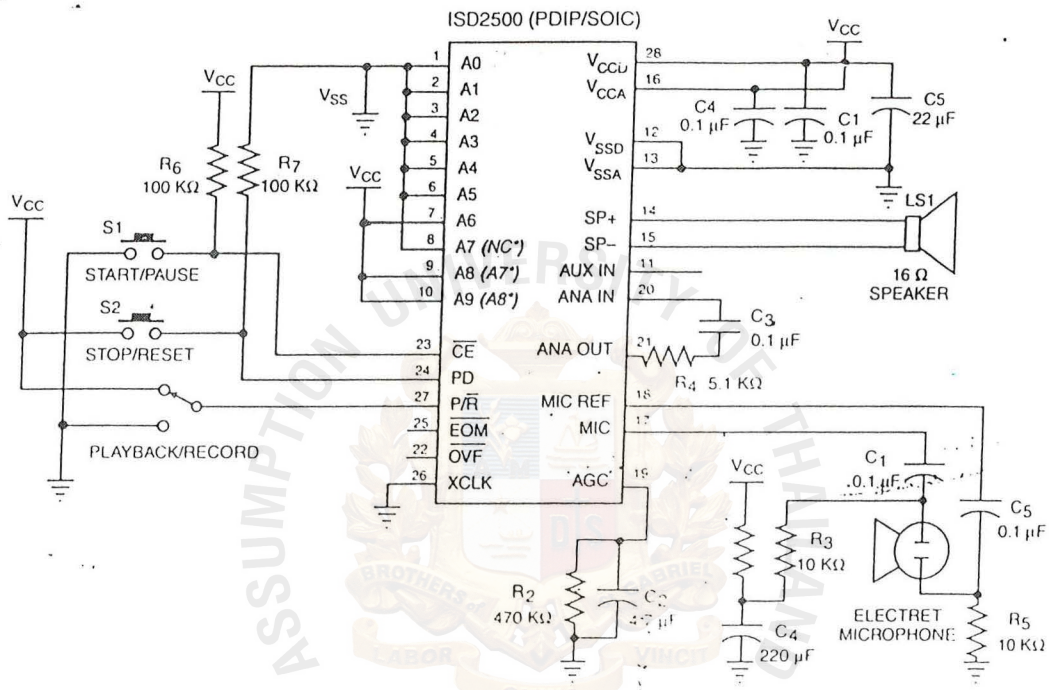
FEATURES

- Easy-to-use single-chip voice Record/Playback solution
- High-quality, natural voice/audio reproduction
- Manual switch or microcontroller compatible Playback can be edge- or level-activated
- Single-chip durations of *32*, 40*, 48*, 64*,* 60, 75, 90, and 120 seconds
- Directly cascadable for longer durations
- Automatic Power-Down (Push-Button Mode)
  - Standby current 1 µA (typical)
- Zero-power message storage
  - Eliminates battery backup circuits
- Fully addressable to handle multiple messages
- 100-year message retention (typical)
- 100,000 record cycles (typical)
- On-chip clock source
- No algorithm development required
- Single +5 volt power supply
- Available in die form, DIP, SOIC, and TSOP packaging
- Industrial temperature (-40°C to +85°C) versions available

ISD2500 SERIES SUMMARY

Part Number	Duration (Seconds)	Input Sample Rate (KHz)	Typical Filter Pass Band (KHz)
ISD2560	60	8.0	3.4
ISD2575	75	6.4	2.7
ISD2590	90	5.3	2.3
ISD25120	120	4.0	1.7
*ISD2532**	*32*	*8.0*	*3.4*
*ISD2540**	*40*	*6.4*	*2.7*
*ISD2548**	*48*	*5.3*	*2.3*
*ISD2564**	*64*	*4.0*	*1.7*

ISD2500 APPLICATION EXAMPLE – PUSH-BUTTON



NOTES: * Pin identifications for the ISD2532/40/48/64 devices which differ from those of the ISD2560/75/90/120 devices are indicated.

** For more details, please refer to the ISD Application Notes and Design Manual.

APPLICATION EXAMPLE – PUSH-BUTTON CONTROL

Control Step	Function	Action
1	Select Record/Playback mode	P/$\overline{R}$ = As desired
2A	Begin Playback	P/$\overline{R}$ = HIGH $\overline{CE}$ = Pulsed LOW
2B	Begin Record	P/$\overline{R}$ = LOW $\overline{CE}$ = Pulsed LOW
3	Pause Record or Playback	$\overline{CE}$ = Pulsed LOW
4A	End Payback	Automatic at EOM marker or PD = Pulsed HIGH
4B	End Record	PD = Pulsed HIGH